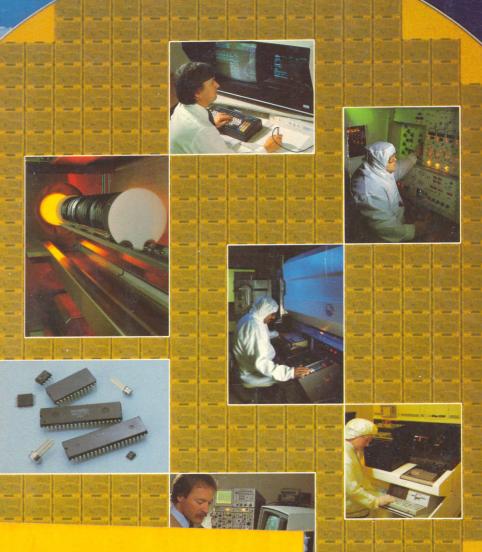


## Component Data Catalog 1986 Excellence in Signal Processing and Control Integrated Circuits





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2N4867 2N4867A 2N4868 2N4868A 2N4869	2N4867 2N4867A 2N4868 2N4868A 2N4869	2N5395 2N5396 2N5397 2N5398 2N5432	2N4869A 2N4869A 2N5397 2N5398 2N5432	2N5950 2N5951 2N5952 2N5953 2N6085	2N5486 2N5486 2N5484 2N5484 IT122	3N156 3N156A 3N157 3N157 3N157A 3N158	3N163 3N163 3N163 3N163 3N163
2N4869A 2N4878 2N4879 2N4880 2N4937	2N4869A 2N4878 2N4879 2N4880 IT131	2N5433 2N5434 2N5452 2N5453 2N5454	2N5433 2N5434 2N5452 2N5453 2N5454	2N6086 2N6087 2N6088 2N6089 2N6090	IT122 IT121 IT121 IT121 IT122 IT121	3N158A 3N160 3N161 3N163 3N164	3N163 3N161 3N161 3N163 3N164
2N4938 2N4939 2N4940 2N4941 2N4942	ITI32 IT132 IT132 IT131 IT132	2N5457 2N5458 2N5459 2N5460 2N5461	2N5457 2N5458 2N5459 2N5460 2N5461	2N6091 2N6092 2N6441 2N6442 2N6443	IT121 IT121 IT122 IT122 IT122	3N165 3N166 3N167 3N168 3N169	3N165 3N166 3N161 3N161 3N170
2N4955 2N4956 2N4977 2N4978 2N4979	IT122 IT122 2N5433 2N5433 2N4859	2N5462 2N5463 2N5464 2N5465 2N5471	2N5462 2N5463 2N5464 2N5465 2N5265	2N6444 2N6445 2N6446 2N6447 2N6448	IT122 IT121 IT121 IT121 IT121 IT121	3N170 3N171 3N172 3N173 3N174	3N170 3N171 3N172 3N173 3N163
2N5018 2N5019 2N5020 2N5021 2N5033	2N5018 2N5019 2N2843 2N2607 2N5460	2N5472 2N5473 2N5474 2N5475 2N5476	2N5265 2N5265 2N5265 2N5265 2N5265 2N5266	2N6451 2N6452 2N6453 2N6454 2N6483	U310 U310 U310 U310 U310 2N6483	3N175 3N176 3N177 3N177 3N178 3N179	3N170 3N170 3N171 3N171 3N172 3N172

3N180	3N172	AD7520KD	AD7520KD	AH0139D/883	DG139AK/883B	BF801	2N4867
3N181	3N161	AD7520KN	AD7520KN	AH0140CD	DG140BK	BF802	2N4338
3N182	3N161	AD7520LD	AD7520LD	AH0140D	DG140AK	BF804	2N4338
3N183	3N161	AD7520LN	AD7520LN	AH0140D/883	DG140AK/883B	BF805	2N4869
3N188	3N188	AD7520SD	AD7520SD	AH0141CD	DG141BK	BF806	2N4869
3N189	3N189	AD7520TD	AD7520TD	AH0141D	DG141AK	BF808	2N4868
3N190	3N190	AD7520UD	AD7520UD	AH0141D/883	DG141AK/883B	BF810	2N4858
3N191	3N191	AD7521JD	AD7521JD	AH0142CD	DG142BK	BF811	2N4858
3N207	3N190	AD7521JN	AD7521JN	AH0142D	DG142AK	BF815	2N4858
3N208	3N188	AD7521KD	AD7521KD	AH0142D/883	DG142AK/883B	BF816	2N4858
35K22	2N5486	AD7521KN	AD7521KN	AH0143CD	DG143BK	BF817	2N4858
35K23	2N5397	AD7521LD	AD7521LD	AH0143D	DG143AK	BF818	2N4858
35K28	2N5397	AD7521LN	AD7521LN	AH0143D/883	DG143AK/883B	BFQ10	U401
42T	2N4392	AD7521SD	AD7521SD	AH0144CD	DG144BK	BFQ11	U401
4360TP	2N5462	AD7521TD	AD7521TD	AH0144D	DG144AK	BFQ12	U402
5033TP	2N5460	AD7521UD	AD7521UD	AH0144D/883	DG144AK/883B	BFQ13	U403
588U	2N4416	AD7523AD	AD7523AD	AH0145CD	DG145BK	BFQ14	U404
58T	2N5457	AD7523BD	AD7523BD	AH0145D	DG145AK	BFQ15	U405
59T	2N4416	AD7523CD	AD7523CD	AH0145D/883	DG145AK/883B	BFQ16	U406
703U	2N4220	AD7523JN	AD7523JN	AH0146CD	DG145BK	BFQ23	IT5912
704U	2N4220	AD7523KN	AD7523KN	AH0146D	DG146AK	BFQ26	U403
705U	2N4224	AD7523LN	AD7523LN	AH0146D/883	DG146AK/883B	BFQ44	IT5912
707U	2N4860	AD7523SD	AD7523SD	AH0151CD	DG151BK	BFQ45	IT5912
714U	2N3822	AD7523TD	AD7523TD	AH0151D/883	DG151AK/883B	BFQ49A	2N3055
734EU	2N4416	AD7523UD	AD7523UD	AH0152CD	DG152BK	BFQ49B	2N3958
734U	2N5516	AD7530JD	AD7530JD	AH0152D	DG152AK	BFQ49C	2N3958
751U	2N4340	AD7530JN	AD7530JN	AH0152D/883	DG152AK/883B	BFS21	2N5199
752U	2N4340	AD7530KD	AD7530KD	AH0153CD	DG153BK	BFS21A	2N5199
753U	2N4341	AD7530KN	AD7530KN	AH0153D	DG153AK	BFS67	2N3821
754U	2N4340	AD7530LD	AD7530LD	AH0153D/883	DG153AK/883B	BFS67P	2N5459
755U	2N4341	AD7530LN	AD7530LN	AH0154CD	DG154BK	BFS68	2N3823
756U	2N4340	AD7531JD	AD7531JD	AH0154D	DG154AK	BFS68P	2N4416
A190	ITE4416	AD7531JN	AD7531JN	AH0154D/883	DG143AK/883B	BFS70	2N3821
A191	ITE4416	AD7531KD	AD7531KD	AH0155D	DG151AK	BFS71	2N3822
A192	2N4416	AD7531KN	AD7531KN	AH0161CD	DG161BK	BFS72	2N3823
A193	2N5484	AD7531LD	AD7531LD	AH0161D	DG161AK	BFS73	2N3821
A194	2N5484	AD7531LN	AD7531LN	AH0161D/883	DG161AK/883B	BFS74	2N4856
A195	2N5484	AD7533AD	AD7533AD	AH0162CD	DG162BK	BFS75	2N4857
A196	ITE4416	AD7533BD	AD7533BD	AH0162D	DG162AK	BFS76	2N4858
A197	ITE4391	AD7533CD	AD7533CD	AH0162D/883B	DG162AK/883B	BFS77	2N4859
A198	ITE4392	AD7533JN	AD7533JN	AH0163CD	DG163BK	BFS78	2N4860
A199	ITE4393	AD7533KN	AD7533KN	AH0163D	DG163AK	BFS79	2N4861
A5T3821	2N5484	AD7533LN	AD7533LN	AH0163D/883	DG163AK/883B	BFS80	2N4416A
A5T3822	2N5484	AD7533SD	AD7533SD	AH0164CD	DG164BK	BFT10	2N5397
A5T3823	2N4416	AD7533TD	AD7533TD	AH0164D	DG164AK	BFT11	2N5019
A5T3824	2N4341	AD7533UD	AD7533UD	AH0164D/883	DG164AK/883B	BFW10	2N3823
A5T5460	2N5460	AD7541AD	AD7541AD	AH5009CN	IH5009CPD	BFW11	2N3822
A5T5461	2N5461	AD7541BD	AD7541BD	AH5010CN	IH5010CPD	BFW12	2N4416
A5T5462	2N5462	AD7541JN	AD7541JN	AH5012CN	IH5012CPE	BFW13	2N4867
AD108	LM108	AD7541KN	AD7541KN	AH5013CN	IH5013CPD	BFW39	IT129
AD308	LM308	AD7541SD	AD7541SD	AH5014CN	IH5014CPD	BFW39A	IT120
AD3954	2N3954	AD7541TD	AD7541TD	AH5015CN	IH5015CPE	BFW54	2N3822
AD3954A	2N3954A	AD810	2N4878	AH5016CN	IH5016CPE	BFW55	2N3822
AD3955	2N3955	AD811	2N4878	AM5011CN	IH5011CPE	BFW56	2N4860
AD3956	2N3956	AD812	2N4878	BC264	2N5458	BFW61	2N4224
AD3958	2N3958	AD813	2N4878	BC264A	2N5457	BFX11	IT132
AD503	AD503	AD814	IT124	BC264B	2N5458	BFX15	IT122
AD589	ICL8069	AD815	IT124	BC264C	2N5458	BFX36	IT131
AD590	AD590	AD816	IT120A	BC264D	2N4416	BFX70	IT122
AD5905	2N5905	AD818	IT140	BCY87	IT121	BFX71	IT122
AD5906	2N5906	AD820	IT132	BCY88	IT122	BFX72	IT122
AD5907	2N5907	AD821	IT130A	BCY89	IT122	BFX78	2N5397
AD5908	2N5908	AD822	IT130A	BF244	2N5486	BFX82	2N5019
AD5909	2N5909	AD830	2N5520	BF244A	2N5484	BFX83	2N5019
AD7506/COM/CHIPS	IH6116C/D	AD831	2N5521	BF244B	2N5485	BFX99	IT120A
AD7506/MIL/CHIPS AD7506JD AD7506JD/883B AD7506JN AD7506KD	IH6116M/D IH6116CJI IH6116CJI/883B IH6116CPI IH6116CJI	AD832 AD833 AD833A AD835 AD836	2N5522 2N5523 2N5524 2N3954 2N3955	BF244C BF245 BF245A BF245B BF245C	2N5486 2N5486 2N4416 2N4416 2N4416	BFY20 BFY81 BFY82 BFY83 BFY84	IT122 IT122 IT122 IT122 IT122 IT122
AD7506KD/883B AD7506KN AD7506SD AD7506SD/883B AD7506TD	IH6116CJI/883B IH6116CPI IH6116MJI IH6116MJI/883B IH6116MJI	AD837 AD838 AD839 AD840 AD841	2N3955 2N3956 2N3957 2N5520 2N5521	BF246 BF246A BF246B BF246C BF247	2N5485 2N5639 2N5638 2N5638 2N4091	BFY85 BFY86 BFY91 BFY92 BN209	IT122 IT122 IT122 IT122 IT122 IT122
AD7506TD/883B	IH6116MJI/883B	AD842	2N5523	BF247A	2N4091	BSV22	2N4416
AD7507/COM/CHIPS	IH6216C/D	AH0126CD	DG126BK	BF247B	2N4091	BSV78	2N4856A
AD7507/MIL/CHIPS	IH6216M/D	AH0126D	DG126AK	BF247C	2N4091	BSV79	2N4857A
AD7507JD	IH6216CJI	AH0126D/883	DG126AK/883B	BF256	2N5484	BSV80	2N4858A
AD7507JD/883B	IH6216CJI/883B	AH0129CD	DG129BK	BF256A	2N5484	BSX82	2N3822
AD7507JN	IH6216CPI	AH0129D	DG129AK	BF256B	2N4416	C21	2N3821
AD7507KD	IH6216CJI	AH0129D/883	DG129AK/883B	BF256C	2N4416	C2306	2N5196
AD7507KD/883B	IH6216CJI/883B	AH0133CD	DG133BK	BF320	2N5461	C38	2N4338
AD7507KN	IH6216CPI	AH0133D	DG133AK	BF320A	2N5460	C413N	2N5434
AD7507SD	IH6216M/D	AH0133D/883	DG133AK/883B	BF320B	2N5461	C610	2N4392
AD7507SD/883B	IH6216MJI/883B	AH0134CD	DG134BK	BF320C	2N5462	C611	2N4221
AD7507TD	IH6216MJI	AH0134D	DG134AK	BF346	ITE4392	C612	2N4221
AD7507TD/883B	IH6216MJI/883B	AH0134D/883	DG134AK/883B	BF347	J201	C613	2N4221
AD7520JD	AD7520JD	AH0139CD	DG139BK	BF348	J310	C614	2N4220
AD7520JN	AD7520JN	AH0139D	DG139AK	BF800	2N4867	C615	2N4221

C620 C621 C622 C623 C624	2N4220 2N4220 2N4220 2N4220 2N4220 2N4220	D1202 D1203 D123AL D123AP D123BP	2N3821 2N4220 D123AL D123AK D123BK	DG151BP DG152AL DG152AP DG152BP DG153AL	DG151BK DG152AL DG152AK DG152BK DG153AL	DG188BP DG189AL DG189AP DG189BP DG190AL	DG188BK DG189AL DG189AK DG189BK DGM190AL
C625 C650 C651 C652 C653	2N4220 2N4220 2N4220 2N4220 2N4220 2N4220	D123BP D125AL D125AP D125BP D129AL	D123BJ D125AL D125AP D125BK D129AL	DG153AP DG153BP DG154AL DG154AP DG154BP	DG153AK DG153BK DG154AL DG154AK DG154BK	DG190AL DG190AP DG190AP DG190BP DG190BP	DG190AL DGM190AK DG190AK DGM190CJ DGM190BK
C6690	2N4341	D129AP	D129AK	DG161AL	DG161AL	DG190BP	DG190BK
C6691	2N4341	D129BP	D129BK	DG161AP	DG161AK	DG191AL	DGM191AL
C6692	2N4339	D1301	2N4222	DG161BP	DG161BK	DG191AL	DG191AL
C673	2N4341	D1302	2N4220	DG162AL	DG162AL	DG191AP	DGM191AK
C674	2N4341	D1303	2N4220	DG162AP	DG162AK	DG191AP	DG191AK
C680 C680A C681 C681A C682	2N4338 2N4338 2N4338 2N4338 2N4338 2N4339	D1420 D1421 D1422 D2T2218 D2T2218A	2N4868 2N3822 2N4869 IT129 IT129	DG162BP DG163AL DG163AP DG163BP DG164AL	DG162BK DG163AL DG163AK DG163BK DG164AL	DG1918P DG1918P DG1918P DG200AA DG200AK	DGM191CJ DGM191BK DG191BK DG200AA DG200AK
C682A	2N4339	D2T2219	IT129	DG164AP	DG164AK	DG200AL	DG200AL
C683	2N4339	D2T2219A	IT129	DG164BP	DG164BK	DG200AP	DG200AK
C683A	2N4339	D2T2904	IT139	DG180AA	DG180AA	DG200BA	DG200BA
C684	2N4220	D2T2904A	IT139	DG180AL	DG180AL	DG200BK	DG200BK
C684A	2N4220	D2T2905	IT139	DG180AP	DG180AK	DG200BP	DG200BK
C685	2N4220	D2T2905A	IT139	DG180BA	DG180BA	DG200CJ	DG200CJ
C685A	2N4220	D2T918	IT129	DG180BP	DG180BK	DG201AK	DG201AK
C80	2N4338	DA102	2N5196	DG181AA	DGM181AA	DG201AP	DG201AK
C81	2N4338	DA402	2N5196	DG181AA	DG181AA	DG201BK	DG201BK
C84	2N4338	DAC1020LCD	AD7520LD	DG181AL	DGM181AL	DG201CJ	DG201CJ
C85	2N4338	DAC1020LD	AD7520UD	DG181AL	DG181AL	DG210BP	DG201BK
C91	2N4858	DAC1021LCD	AD7520KD	DG181AP	DGM181AK	DG281AA	IH182MTW
C92	2N4091	DAC1021LD	AD7520TD	DG181AP	DG181AK	DG281AP	IH182MJD
C93	2N4393	DAC1022LCD	AD7520JD	DG181BA	DGM181BA	DG281BA	IH182CTW
C94	2N5457	DAC1022LD	AD7520SD	DG181BA	DG181BA	DG281BP	IH182CJD
C94E	2N5457	DAC1218LCD	AD7541BD	DG181BP	DGM181CJ	DG284AP	IH185MJE
C95	2N5457	DAC1218LCN	AD7541LN	DG181BP	DGM181BK	DG284BP	IH185CJE
C95E	2N5459	DAC1218LCN	AD7541KN	DG181BP	DG181BK	DG287AA	IH188MTW
C96E	2N5484	DAC1219LCD	AD7541AD	DG182AA	DGM182AA	DG287AP	IH188MJD
C97E	2N3822	DAC1219LCN	AD7541JN	DG182AA	DG182AA	DG287BA	IH188CTW
C98E	2N3822	DAC1220LCD	AD7521LD	DG182AL	DGM182AL	DG287BP	IH188CJD
CA308	LM308	DAC1220LD	AD7521UD	DG182AL	DG182AL	DG290AP	IH191MJE
CC4445	2N5432	DAC1221LCD	AD7521KD	DG182AP	DGM182AK	DG290BP	IH191CJE
CC4446	2N5434	DAC1221LD	AD7521TD	DG182AP	DG182AK	DG381AA	DGM182AA
CC697	2N4856	DAC1222LCD	AD7521JD	DG182BA	DGM182BA	DG381AK	DGM182AK
CD22001H CD22015E CF2386 CF24 CFM13026	ICM1424C ICM7051A 2N5458 2N3824 2N4858	DAC1222LD DG123AL DG123AP DG123BP DG125AL	AD7521SD DG123AL DG123AK DG123BK DG125AL	DG182BA	DG182BA DGM182CJ DGM182BK DG182BK DG183AL	DG381AP DG381BA DG381BK DG381BP DG381CJ	DGM181BA
CM600	2N4092	DG125AP	DG125AK	DG183AP	DG183AK	DG384AK	DGM185AK
CM601	2N4091	DG125BP	DG125BK	DG183BP	DG183BK	DG384AP	DGM185AK
CM602	2N4091	DG126AK	DG126AK	DG184AL	DGM184AL	DG384BK	DGM184BK
CM603	2N4091	DG126AL	DG126AL	DG184AL	DG184AL	DG384BP	DGM184BK
CM640	2N4093	DG126BP	DG126BK	DG184AP	DGM184AK	DG384CJ	DGM184CJ
CM641	2N4093	DG129AL	DG129AL	DG184AP	DG184AK	DG387AA	DGM188AA
CM642	2N4093	DG129AP	DG129AK	DG184BP	DGM184CJ	DG387AK	DGM188AK
CM643	2N4092	DG129BP	DG129BK	DG184BP	DGM184BK	DG387AP	DGM188AK
CM644	2N4092	DG133AL	DG133AL	DG184BP	DG184BK	DG387BA	DGM187BA
CM645	2N4092	DG133AP	DG133AK	DG185AL	DGM185AL	DG387BK	DGM187BK
CM646	2N4092	DG133BP	DG133BK	DG185AL	DG185AL	DG387BP	DGM187BK
CM647	2N4091	DG134AL	DG134AL	DG185AP	DGM185AK	DG390AK	DGM191AK
CM650	2N5432	DG134AP	DG134AK	DG185AP	DG185AK	DG390AP	DGM191AK
CM651	2N5433	DG134BP	DG134BK	DG185BP	DGM185CJ	DG390BK	DGM190BK
CM652	2N5432	DG139AL	DG139AL	DG185BP	DGM185BK	DG390BP	DGM190BK
CM653 CM697 CM800 CM856 CM860	2N5433 2N5433 2N5433 2N5433 2N5433 2N4868A	DG139AP DG139BP DG140AL DG140AP DG140BP	DG139AK DG139BK DG140AL DG140AK DG140BK	DG185BP DG186AA DG186AL DG186AP DG186BA	DG185BK DG186AA DG186AL DG186AK DG186BA	DG390CJ DG503 DG5040AK DG5040AL DG5040CJ	DGM190CJ AD503 IH5040MJE IH5040MFD IH5040CPE
CMX740	2N5432	DG141AL	DG141AL	DG186BP	DG186BK	DG5040CK	IH5040CJE
CP640	2N4091	DG141AP	DG141AK	DG187AA	DGM187AA	DG5041AA	IH5041MTW
CP643	2N5434	DG141BP	DG141BK	DG187AA	DG187AA	DG5041AK	IH5041MJE
CP650	2N5432	DG142AL	DG142AL	DG187AL	DGM187AL	DG5041AL	IH5041MFD
CP651	2N5433	DG142AP	DG142AK	DG187AL	DG187AL	DG5041CJ	IH5041CPE
CP652	2N5433	DG142BP	DG142BK	DG187AP	DGM187AK	DG5041CK	IH5041CJE
CP653	2N5433	DG143AL	DG143AL	DG187AP	DG187AK	DG5042AA	IH5042MTW
D1101	2N3821	DG143AP	DG143AK	DG187BA	DGM187BA	DG5042AK	IH5042MJE
D1102	2N3821	DG143BP	DG143BK	DG187BA	DG187BA	DG5042AL	IH5042MFD
D1103	2N4338	DG144AL	DG144AL	DG187BP	DGM187BK	DG5042CJ	IH5042CPE
D1177	2N3821	DG144AP	DG144AK	DG187BP	DG187BK	DG5042CK	IH5042CJE
D1178	2N3821	DG144BP	DG144BK	DG188AA	DGM188AA	DG5043AK	IH5043MJE
D1179	2N4338	DG145AL	DG145AL	DG188AA	DG188AA	DG5043AL	IH5043MFD
D1180	2N3822	DG145AP	DG145AK	DG188AL	DGM188AL	DG5043CJ	IH5043CPE
D1181	2N4338	DG145BP	DG145BK	DG188AL	DG188AL	DG5043CK	IH5043CJE
D1182	2N4338	DG146AL	DG146AL	DG188AP	DGM188BK	DG5044AA	IH5044MTW IH5044MJE IH5044MFD IH5044CPE IH5044CJE
D1183	2N4341	DG146AP	DG146AK	DG188AP	DGM188AK	DG5044AK	
D1184	2N4340	DG146BP	DG146BK	DG188AP	DG188AK	DG5044AL	
D1185	2N4339	DG151AL	DG151AL	DG188BA	DGM188BA	DG5044CJ	
D1201	2N4224	DG151AP	DG151AK	DG188BA	DG188BA	DG5044CK	

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL
DG5045AK	IH5045MJE	E211	2N5397	FM1111	2N3957	HI1-0200-8	DG200AK/883B
DG5045AL	IH5045MFD	E212	2N5397	FM1111A	2N5909	HI1-0201-2	DG201AK
DG5045CJ	IH5045CPE	E230	2N4867	FM1112	2N5196	HI1-0201-4	DG201BK
DG5045CK	IH5045CJE	E231	2N4868	FM1200	2N3954	HI1-0201-5	DG201BK
DG506AR	IH6116MJI	E232	2N4869	FM1201	2N3954	HI1-0201-8	DG201AK/883B
DG506BR	IH6116CJI	E270	J270	FM1202	2N3954	HI1-0381-2	DGM182AK
DG506CJ	IH6116CPI	E271	J271	FM1203	2N3955A	HI1-0381-5	DGM181BK
DG507AR	IH6216MJI	E300	2N5397	FM1204	2N3955	HI1-0381-8	DGM182AK/883B
DG507BR	IH6216CJI	E304	2N5486	FM1205	2N3954	HI1-0384-2	DGM185AK
DG507CJ	IH6216CPI	E305	2N5484	FM1206	2N3954	HI1-0384-5	DGM184BK
DG508AP DG508BP DG508CJ DG509AP DG509BP	IH6108MJE IH6108CJE IH6108CPE IH5208MJE IH6208CJE	E308 E309 E310 E311 E312	J308 J309 J310 J310 J310 2N5397	FM1207 FM1208 FM1209 FM1210 FM1211	2N3954 2N3955A 2N3955 2N3955A IT5911	HI1-0384-8 HI1-0387-2 HI1-0387-5 HI1-0387-8 HI1-0390-2	DGM185AK/883B DGM188AK DGM187BK DGM188AK/883B DGM191AK
DG509CJ	IH6208CPE	E400	2N3955	FM3954	2N3954	HI1-0390-5	DGM190BK
DGM111AL	DG111AL	E401	2N3955	FM3954A	2N3954A	HI1-0390-8	DGM191AK/883B
DGM111AP	DG111AK	E402	2N3957	FM3955	2N3955	HI1-0506-2	IH6116MJI
DGM111BP	DG111BK	E410	2N3955	FM3955A	2N3955A	HI1-0506-5	IH6116CJI
DN3066A	2N3821	E411	IT5911	FM3956	2N3956	HI1-0506-8	IH6116MJI/883B
DN3067A	2N4338	E412	IT5911	FM3957	2N3957	HI1-0506A-2	IH5116MJI
DN3068A	2N4338	E413	2N5454	FM3958	IT5911	HI1-0506A-5	IH5116IJI
DN3069A	2N3822	E414	2N3956	FP4339	2N4339	HI1-0506A-8	IH5116MJI/883B
DN3070A	2N3821	E415	2N3957	FP4340	2N4340	HI1-0507-2	IH6216MJI
DN3071A	2N4338	E420	IT5911	FT0654A	2N5486	HI1-0507-5	IH6216CJI
DN3365A DN3365B DN3366A DN3366B DN3367A	2N4220 2N4091 2N3686 2N4091 2N3687	E421 E430 E431 ESM25 ESM25A	J309(X2) J310(X2) U401 U401	FT0654B FT0654C FT0654D FT3820 FT3820	2N5486 2N4221 2N4221 2N5460 2N5019	HI1-0507-8 HI1-0507A-2 HI1-0507A-5 HI1-0507A-8 HI1-0508-2	IH6216MJI/883B IH5216MJI IH5216IJI IH5216MJI/883B IH6108MJE
DN3367B	2N4091	ESM4091	2N4091	FT3909	2N5019	HI1-0508-5	IH6108CJE
DN3368A	2N4341	ESM4092	2N4092	FT703	3N161	HI1-0508-8	IH6108MJE/883B
DN3368B	2N4221	ESM4093	2N4093	FT704	3N163	HI1-0508A-2	IH5108MJE
DN3369A	2N4339	ESM4302	2N5457	G115AP	G115AK	HI1-0508A-5	IH5108IJE
DN3369B	2N4220	ESM4303	2N5459	G115BP	G115BK	HI1-0508A-8	IH5108MJE/883B
DN3370A	2N4338	ESM4304	2N5458	G115BP	G115BJ	HI1-0509-2	IH6208MJE
DN3370B	2N4338	ESM4445	2N5432	G116AL	G116AL	HI1-0509-5	IH6208CJE
DN3436A	2N4341	ESM4446	2N5434	G116AP	G116AK	HI1-0509-8	IH6208MJE/883B
DN3436B	2N4222	ESM4447	2N5432	G116BP	G116BK	HI1-0509A-2	IH5208MJE
DN3437A	2N4340	ESM4448	2N5434	G116BP	G116BJ	HI1-0509A-5	IH5208IJE
DN3437B	2N4220	FE0654A	2N4386	G117AL	G117AL	HI1-0509A-8	IH5208MJE/883B
DN3438A	2N4338	FE0654B	2N5485	G118AL	G118AL	HI1-5040-2	IH5040MJE
DN3438B	2N4339	FE100	2N3821	G118AP	G118AK	HI1-5040-5	IH5040CJE
DN3458A	2N4341	FE100A	2N3821	G119AL	G119AL	HI1-5040-8	IH5040MJE/883B
DN3458B	2N4222	FE102	2N4119	G123AL	G123AL	HI1-5041-2	IH5041MJE
DN3459A	2N4339	FE102A	2N4119	G123AP	G123AK	HI1-5041-5	IH5041CJE
DN3459B	2N4220	FE104	2N4118	GET5457	2N5457	HI1-5041-8	IH5041MJE/883B
DN3460A	2N4338	FE104A	2N4118	GET5458	2N5458	HI1-5042-2	IH5042MJE
DN3460B	2N4220	FE1600	2N4092	GET5459	2N5459	HI1-5042-5	IH5042CJE
DNX1	2N4338	FE200	2N3821	HA2720	ICL8021	HI1-5042-8	IH5142MJE/883B
DNX2	2N4338	FE202	2N3821 9A68	HA7807	IT132	HI1-5043-2	IH5143MJE
DNX3	2N4338	FE204	2N3821 9B6	HA7809	IT132	HI1-5043-5	IH5143CJE
DNX4	2N4869	FE300	2N3822	HD43871	ICM7050H	HI1-5043-8	IH5143MJE/883B
DNX5	2N4868	FE302	2N3821 9A68	HD43871	ICM7050G	HI1-5044-2	IH5144MJE
DNX6	2N4338	FE304	2N3821 9A68	HDIG1030	3N163	HI1-5044-5	IH5144CJE
DNX7	2N4416	FE3819	2N5484	HEP801	2N3822	HI1-5044-8	IH5144MJE/883B
DNX8	2N4416	FE4302	2N5457	HEP802	2N5484	HI1-5045-2	IH5145MJE
DNX9	2N4339	FE4303	2N5459	HEP803	2N5019	HI1-5045-5	IH5145CJE
DS0026	ICL7667	FE4304	2N5458	HEPF0021	2N5484	HI1-5045-8	IH5145MJE/883B
DU4339	2N5397	FE5245	2N4416	HEPF1035	J176	HI1-5046-2	IH5046MJE
DU4340	2N5398	FE5246	2N5484	HEPF2004	2N5484	HI1-5046-5	IH5046CJE
	2N5458	FE5247	2N5486	HEPF2005	2N5459	HI1-5046-8	IH5046MJE/883B
	J204	FE5457	2N5457	HI0-0201-6	DG201C/D	HI1-5047-2	IH5047MJE
	2N5457	FE5458	2N5458	HI0-0381-6	DGM181C/D	HI1-5047-5	IH5047CJE
	2N5459	FE5459	2N5459	HI0-0384-6	DGM184C/D	HI1-5047-8	IH5047MJE/883B
E105	J105	FE5484	2N5484	HI0-0387-6	DGM187C/D	HI1-5049-2	IH5149MJE
E106	J106	FE5485	2N5485	HI0-0390-6	DGM190C/D	HI1-5049-5	IH5149CJE
E107	J107	FE5486	2N5486	HI0-0506-6	IH6116C/D	HI1-5049-8	IH5149MJE/883B
E108	J105	FF400	2N5457	HI0-0506A-6	IH5116C/D	HI1-5050-2	IH5150MJE
E109	J106	FM1100	2N3954A	HI0-0507-6	IH6216C/D	HI1-5050-5	IH5150CJE
E110 COMPANI	J107	FM1100A	2N5906	HI0-0507A-6	IH5216C/D	HI1-5050-8	IH5150MJE/883B
E111 A COMPANI	J111	FM1101A	2N5906	HI0-0508-6	IH6108C/D	HI1-5051-2	IH5151MJE
E1115 COMPANI	ICM1115A	FM1102	2N3954	HI0-0508A-6	IH5108C/D	HI1-5051-5	IH5151CJE
E111A COMPANI	J111	FM1102A	2N5906	HI0-0509-6	IH6208C/D	HI1-5051-8	IH5151MJE/883B
E112	J112	FM1103	2N3955	HI0-0509A-6	IH5208C/D	HI2-0200-2	DG200AA
E112A	J112	FM1103A	2N5908	HI0-5040-6	IH5140C/D	HI2-0200-4	DG200BA
E113	J113	FM1104	2N3957	HI0-5041-6	IH5141C/D	HI2-0200-5	DG200BA
E113A	J113	FM1104A	2N5909	HI0-5042-6	IH5142C/D	HI2-0200-8	DG200AA/883B
E114	J204	FM1105	2N3954A	HI0-5043-6	IH5143C/D	HI2-0381-2	DGM182AA
E1151	ICM11158	FM1105A	IT500	HI0-5044-6	IH5144C/D	HI2-0381-5	DGM181BA
E1426	ICM7050U	FM1106	2N3954A	HI0-5045-6	IH5145C/D	HI2-0381-8	DGM181AA/883B
E174	J174	FM1106A	1T500	HI0-5046-6	IH5046C/D	HI2-0387-2	DGM188AA
E175	J175	FM1107	2N3954	HI0-5047-6	IH5047C/D	HI2-0387-5	DGM187BA
E176	J176	FM1107A	1T500	HI0-5049-6	IH5149C/D	HI2-0387-8	DGM188AA/883B
E177	J177	FM1108	2N3955	HI0-5050-6	IH5150C/D	HI3-0200-5	DG200CJ
E201 E202 E203 E204 E210	J201 J202 J203 J204 2N5397	FM1108A FM1109 FM1109A FM1110	IT502 2N3957 IT503 2N3955 2N5908	HI0-5051-6 HI1-0200-2 HI1-0200-4 HI1-0200-5 HI1-0200-6	IH5051C/D DG200AK DG200BK DG200BK DG200C/D	HI3-0201-5 HI3-0381-5 HI3-0384-5 HI3-0390-5 HI3-0506-5	DG201CJ DGM181CJ DGM184CJ DGM190CJ IH6116CPI

ALTERNATE SOURCE PRODUC	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL
HI3-0506A-5	IH5116CPI	ITC4023	IT137	J109	J106 A40 DT J106 J107 J107 J107 J111 A01M	J4393	ITE4393
HI3-0507-5	IH6216CPI	ITC4024	IT137	J109-18		J4416	ITE4416
HI3-0507A-5	IH5216CPI	ITC4025	IT137	J110		J4856	ITE4856
HI3-0508-5	IH6108CPE	ITE2453	IT120	J110-18		J4857	ITE4857
HI3-0508A-5	IH5108CPE	ITE2639	IT120	J111		J4858	ITE4858
HI3-0509-5	IH6208CPE	ITE2640	IT122	J111-18	J111 GOLM	J4859	ITE4859
HI3-0509A-5	IH5208CPE	ITE2641	IT122	J111A	J111 GOLM	J4860	ITE4860
ID100	ID100	ITE2642	IT120	J111A-18	J111 BOLM	J4861	ITE4861
ID101	ID101	ITE2643	IT122	J112	J112 J112	J4867	2N4867
IMF3954	2N3954	ITE2644	IT122	J112-18	J112 8 1 1 1	J4867A	2N4867A
IMF3954A IMF3955 IMF3955A IMF3956 IMF3957	2N3954A 2N3955 2N3955A 2N3956 2N3957	ITE2720 ITE2721 ITE2722 ITE2903 ITE2913	IT120 IT122 IT120 IT122 IT122	J112A J112A-18 J113 J113-18 J113A	J112 J112 J113 J113 J113	J4867RR J4868 J4868A J4868RR J4869	2N4867 2N4868 2N4868A 2N4868 2N4869
IMF3958	2N3958	ITE2914	IT122	J113A-18	J113	J4869A	2N4869A
IMF5911	IMF5911	ITE2915	IT120	J114	2N5555	J4869RR	2N4869
IMF5912	IMF5912	ITE2916	IT120	J1401	IT501	J5103	2N5484
IMF6485	IMF6485	ITE2917	IT122	J1402	IT502	J5104	2N5485
IT100	IT100	ITE2918	IT122	J1403	IT503	J5105	2N5486
IT101 IT108 IT109 IT120 IT120A	IT101 ITE4416 ITE4416 IT120 IT120A	ITE2919 ITE2920 ITE2936 ITE2937 ITE2972	IT120 IT120 IT120 IT120 IT120 IT122	J1404 J1405 J1406 J174 J174-18	IT503 IT504 IT505 J174 J174	J5163 K114-18 K210-18 K211-18 K212-18	2N5486 2N5555 2N5397 2N5397 2N5397
IT121 IT122 IT124 IT126 IT127	IT121   101 = 101   111   112	ITE2973 ITE2974 ITE2975 ITE2976 ITE2977	IT122 IT120 IT120 IT120 IT120 IT120	J175 J175-18 J176 J176-18 J177	J175 J175 J176 J176 J176 J177	K300-18 K304-18 K305-18 K308-18 K309-18	2N5397 2N5486 2N5484 J308 J309
IT128	IT128	ITE2978	IT120	J177-18	J177	K310-18	J310
IT129	IT129	ITE2979	IT120	J201	J201	KE3684	2N3684
IT130	IT130	ITE3066	2N3685	J201-18	J201	KE3685	2N3685
IT130A	IT130A	ITE3067	2N3686	J202	J202	KE3686	2N3686
IT131	IT131	ITE3068	2N3686	J202-18	J202	KE3687	2N3687
IT132 IT136 IT137 IT138 IT139	IT132 IT136 IT137 IT138 IT139	ITE3347 ITE3348 ITE3349 ITE3350 ITE3351	IT137 IT138 IT139 IT137 IT138	J203 J203-18 J204 J204-18 J210	J203 J203 J204 J204 J204 2N5397	KE3823 KE3970 KE3971 KE3972 KE4091	2N3823 ITE4391 ITE4392 ITE4393 ITE4091
IT140	17140	ITE3680	IT120	J211	2N5397	KE4092	ITE4092
IT1700	171700 658 744	ITE3800	IT132	J212	2N5397	KE4093	ITE4093
IT1701	3N172	ITE3802	IT132	J230	2N4867	KE4220	2N5457
IT1702	3N163	ITE3804	IT130	J231	2N4868	KE4221	2N5459
IT1750	171750	ITE3806	IT132	J232	2N4869	KE4222	2N5459
IT2700	3N165	ITE3807	IT132	J270	J270	KE4223	J204
IT2701	3N165	ITE3808	IT132	J270-18.05	J270	KE4391	ITE4391
IT400	2N4392	ITE3809	IT132	J271	J271	KE4392	ITE4392
IT500	IT500	ITE3810	IT130	J271-18	J271	KE4393	ITE4393
IT500P	IT500	ITE3811	IT130	J300	2N5397	KE4416	ITE4416
IT501	17501	ITE3907	IT120	J304	2N5486	KE4856	ITE4391
IT501P	17501	ITE3908	IT120	J305	2N5484	KE4857	ITE4392
IT502	17502	ITE4017	IT139	J308	J308	KE4858	ITE4393
IT502P	17502	ITE4018	IT139	J309	J309	KE4859	ITE4391
IT503	17503	ITE4019	IT139	J310	J310	KE4860	ITE4392
IT503P	1T503 1T504 1T505 1T550 1T5911	ITE4020	IT139	J315	2N5397	KE4861	ITE4393
IT504		ITE4021	IT139	J316	U309	KE510	ITE4393
IT505		ITE4022	IT139	J317	U310	KE5103	J204
IT550		ITE4023	IT137	J3970	ITE4391	KE5104	ITE4416
IT5911		ITE4024	IT137	J3971	ITE4392	KE5105	ITE4416
IT5912	175912	ITE4025	IT137	J3972	ITE4393	KE511	ITE4392
ITC2972	17122	ITE4091	ITE4091	J401	IT501	KH5196	2N5196
ITC2973	17122	ITE4092	ITE4092	J402	IT502	KH5197	2N5197
ITC2974	17120	ITE4093	ITE4093	J403	IT503	KH5198	2N5198
ITC2975	17120	ITE4117	2N4117	J404	IT503	KH5199	2N5199
ITC2976 ITC2977 ITC2978 ITC2979 ITC3347	IT120 CGGGAM IT120 IT120 IT120 IGCGAM IT120 IT137	ITE4118 ITE4119 ITE4338 ITE4339 ITE4340	2N4118 2N4119 2N4338 2N4339 2N4340	J405 J406 J4091 J4092 J4093	IT504 IT505 ITE4091 ITE4092 ITE4093	KS5183 KS5240B01H KS5240B01J KS5240B10H KS5240B12H	ICM7269 ICM7245B ICM7245A ICM7245D ICM7245E
ITC3348	IT138	ITE4341	2N4341	J410	IT502	KS5240B20H	ICM7245F
ITC3349		ITE4391	ITE4391	J411	IT503	KS5240U01E	ICM7245U
ITC3350		ITE4392	ITE4392	J412	IT503	LDF603	2N4221
ITC3351		ITE4393	ITE4393	J420	IT5911	LDF604	2N4221
ITC3352		ITE4416	ITE4416	J421	IT5912	LDF605	2N4221
ITC3800 ITC3802 ITC3804 ITC3806 ITC3807	17132 04.594 17132 17130 17132 17132 17132 17132	ITE4867 ITE4868 ITE4869 J100 J101	2N4867 2N4868 2N4869 2N5458 2N4338	J4220 J4221 J4222 J4223 J4224	J204 J202 J203 J202 J202	LF11201D LF11201D/883 LF11202D LF11202D/883 LF11508D	DG201AK DG201AK/883B IH202MJE IH202MJE/883B IH6108MJE
ITC3808 ITC3809 ITC3810 ITC3811 ITC4017	IT132 IT132 IT130 IT130 IT130 IT139	J102 J103 J105 J105-18 J106	2N5457 2N5459 J105 J105 J106	J430 J4302 J4303 J4304 J431	J309(X2) 2N4302 2N5459 2N5458 J310(X2)	LF11508D/883 LF11509D LF11509D/883 LF13201D LF13201N	IH6108MJE/883B IH6208MJE IH6208MJE/883B DG201BK DG201CJ
ITC4018	17139 AGCEAN	J106-18	J106	J433	2N5457	LF13202D	IH202CJE
ITC4019	17139 VERSON	J107	J107	J4338	2N5457	LF13508D	IH6108CJE
ITC4020	17139 AGCEAN	J107-18	J107	J4339	2N5457	LF13508N	IH6108CPE
ITC4021	17139 AGCEAN	J108	J105	J4391	ITE4391	LF13509D	IH6208CJE
ITC4022	17139 AGCEAN	J108-18	J105	J4392	ITE4392	LF13509N	IH6208CPE

SOURCE PROD	OUCT EQUIVALENT	SOURCE PRODUC	EQUIVALENT	SOURCE PRODUC	T EWUIVALENTS	SOUNCE PHODO	U DESEMBLY ALERT
LH0042	LH0042	LTC1044	ICL7660	MD7003A	IT132	MEM807A	3N172
LH2108	LH2108	LTC1052	ICL7650	MD7003B	IT132	MEM814	3N161
LH2308	LH2308	LTC7652	ICL7652	MD7004	IT129	MEM816	3N172
LM105	LM105	M103	3N161	MD7007	IT129	MEM817	3N172
LM108	LM105	M104	3N161	MD7007A	IT129	MEM823	MFE823
LM113	ICL8069	M106	3N166	MD7007B	IT129	MEM954	3N188
LM114	IT120	M107	3N189	MD708	IT129	MEM954A	3N188
LM114A	IT120A	M108	3N191	MD708A	IT129	MEM954B	3N188
LM114AH	IT120A	M113	3N161	MD708B	IT129	MEM955	3N190
LM114H	IT120	M114	3N161	MD8001	IT120	MEM955A	3N190
LM115	IT120A	M116	M116	MD8002	IT120	MEM955B	3N190
LM115A		M117	2N4351	MD8003	IT122	MF510	2N4092
LM115AH		M119	3N161	MD918	IT122	MF803	2N4338
LM115H		M163	3N163	MD918A	IT122	MF818	2N4858
LM194		M164	3N164	MD918B	IT122	MFE2000	2N4416
LM305 LM308 LM394 LM4250 LS3069	LM308 IT120A LM4250	M5001 M511 M511A M517 M58434P	ICM7269 3N172 3N172 3N172 3N163 ICM7038D	MD982 MD984 MEF103 MEF104 MEF3069	IT139 IT139 2N5457 2N5459 2N4341	MFE2001 MFE2004 MFE2005 MFE2006 MFE2007	2N4416 2N4093 2N4092 2N4091 2N4860
LS3070	2N5458	M58435P	ICM1115B	MEF3070	2N4339	MFE2008	2N4859
LS3071	2N5458	M58436-001P	ICM7050G	MEF3458	2N4341	MFE2009	2N4859
LS3458	J204	M58437-001P	ICM7070L	MEF3459	2N4339	MFE2010	2N4859
LS3459	J204	MA7807	IT132	MEF3460	2N4338	MFE2011	2N5433
LS3460	J204	MA7809	IT132	MEF3684	2N3684	MFE2012	2N5434
LS3684		MAT-01AH	IT140	MEF3685	2N3685	MFE2012	2N5433
LS3685		MAT-01FH	IT140	MEF3686	2N3686	MFE2093	2N4338
LS3686		MAT-01GH	IT140	MEF3687	2N3687	MFE2094	2N4339
LS3687		MAT-01H	IT140	MEF3821	2N3821	MFE2095	2N4340
LS3819		MB101	ICM7245B	MEF3822	2N3822	MFE2133	2N4860
L\$3821	2N3921	MB103	ICM7245E	MEF3823	2N3823	MFE2912	2N5433
L\$3822		MB105	ICM7245U	MEF3954	2N3954	MFE3002	3N170
L\$3823		MB107	ICM7245D	MEF3955	2N3955	MFE3003	3N164
L\$3921		MB108	ICM7245E	MEF3956	2N3956	MFE3020	3N166
L\$3922		MB143	ICM7245A	MEF3957	2N3957	MFE3021	3N166
LS3966	ITE4416	MB144	ICM7245F	MEF3958	2N3958	MFE4007	2N3686
LS3967	ITE4416	MB510	ICM1115B	MEF4223	2N4223	MFE4008	2N3686
LS3968	ITE4416	MB511	ICM7050H	MEF4224	2N4224	MFE4009	2N3685
LS3969	ITE4416	MB512	ICM7050H	MEF4391	ITE4391	MFE4010	2N2608
LS4220	J204	MB513	ICM7050G	MEF4392	ITE4392	MFE4011	2N2608
LS4221 LS4222 LS4223 LS4224 LS4338	J202 J202	MB521 MB522 MB531 MB533 MB541	ITS9068 ITS9068 ICM7050H ICM7050H ICM7052	MEF4393 MEF4416 MEF4856 MEF4857 MEF4858	ITE4393 ITE4416 2N4856 2N4857 2N4858	MFE4012 MFE823 MHW590 MJ41 MJ6	2N2609 IT1700 AD590 ICM1424C ICM7220
LS4339	2N5458	MB542	ICM7052	MEF4859	2N4859	MK10	2N4416
LS4340		MB7B	ICM7245U	MEF4860	2N4860	MM450H	MM450H
LS4341		MCC14440	ICM1424C	MEF4861	2N4861	MM451H	MM451H
LS4391		MCC14483	ICM7210	MEF5103	ITE4416	MM452D	MM452J
LS4392		MD1120	IT122	MEF5104	ITE4416	MM452F	MM452F
LS4393	ITE4393	MD1121	IT122	MEF5105	ITE4416	MM455H	MM455H
LS4416	ITE4416	MD1122	IT122	MEF5245	ITE4416	MM550H	MM550H
LS4856	ITE4091	MD1123	IT139	MEF5246	2N5484	MM551H	MM551H
LS4857	ITE4092	MD1129	IT129	MEF5247	2N5486	MM552D	MM552J
LS4858	ITE4093	MD1130	IT139	MEF5248	2N5486	MM552F	MM552F
LS4859	ITE4091	MD2218	IT129	MEF5284	2N5484	MM555H	MM555H
LS4860	ITE4092	MD2218A	IT129	MEF5285	2N5485	MMF1	2N5197
LS4861	ITE4093	MD2219	IT129	MEF5286	2N5486	MMF2	2N3921
LS5103	2N5484	MD2219A	IT129	MEF5561	U401	MMF3	2N5198
LS5104	2N5485	MD2369	IT129	MEF5562	U402	MMF4	2N3922
LS5105 LS5245 LS5246 LS5247 LS5248	2N5486 ITE4416 2N5484 2N5486 2N5486	MD2369A MD2369B MD2904 MD2904A MD2905	IT129* 17122 IT122 IT139 IT139 IT139	MEF5563 MEM511 MEM511A MEM511C MEM517	U403 3N172 3N172 3N172 3N172 3N172	MMF5 MMF6 MMT3823 MN6091 MN6092A	2N5199 2N3955A 2N3823 ICM7038B ICM7038E
LS5358 LS5359 LS5360 LS5361 LS5362	J204 J204 J202 J202 J203	MD2905A MD2974 MD2975 MD2978 MD2979	IT139 IT120 IT120 IT120 IT120	MEM517A MEM517B MEM517C MEM550 MEM550C	3N172 3N172 3N172 3N172 3N189 3N189	MN6093 MN6252 MP301 MP302 MP303	ICM7051A ICM7050G IT124 IT124 IT124
LS5363	J203	MD3008	IT120	MEM550F	3N189	MP310	2N4045
LS5364	J203	MD3250	IT132	MEM551	3N190	MP311	2N4045
LS5391	2N4867A	MD3250A	IT131	MEM551C	3N189	MP312	2N4044
LS5392	2N4868A	MD3251	IT132	MEM556	3N172	MP313	IT124
LS5393	2N4869A	MD3251A	IT131	MEM556C	3N172	MP318	IT120A
LS5394	2N4869A	MD3409	IT129	MEM560	3N161	MP350	1T132
LS5395	2N4869A	MD3410	IT129	MEM560C	3N161	MP351	1T130
LS5396	2N4869A	MD3467	IT139	MEM561	3N163	MP352	1T130
LS5457	2N5457	MD3725	IT129	MEM561C	3N163	MP358	1T130A
LS5458	2N5458	MD3762	IT139	MEM562	2N4351	MP360	1T132
LS5459 LS5484 LS5485 LS5486 LS5556	2N5459 2N5484 2N5485 2N5486 2N3685	MD4957 MD5000 MD5000A MD5000B MD7000	IT132 IT132 IT132 IT132 IT132 IT129	MEM562C MEM563 MEM563C MEM711 MEM712	2N4351 2N4351 2N4351 M116 M116	MP361 MP362 MP3954 MP3954A MP3955	IT130A IT130A 2N3954 2N3954A 2N3955
LS5557	2N3684	MD7001	IT139	MEM712A	M116	MP3956	2N3956
LS5558	2N3684	MD7002	IT122	MEM713	3N170	MP3957	2N3957
LS5638	2N5638	MD7002A	IT122	MEM806	3N163	MP3958	2N3958
LS5639	2N5639	MD7002B	IT122	MEM806A	3N163	MP5905	2N5905
LS5640	2N5640	MD7003	IT132	MEM807	3N172	MP5906	2N5906

ALTERNATE SOURCE PRODUCT	INTERSIL	ALTERNATE SOURCE PRODUCT	INTERSIL	ALTERNATE SOURCE PRODUCT	INTERSIL	ALTERNATE SOURCE PRODUCT	INTERSIL
MP5907	2N5907	NF4303	2N5459	PF511	2N5114	SG305	LM305
MP5908	2N5908	NF4304	2N5458	PF5301	2N4118A	SG308	LM308
MP5909	2N5909	NF4445	2N5432	PF5301-1	2N4117A	SG4250	LM4250
MP5911	2N5911	NF4446	2N5433	PF5301-2	2N4118A	SG733	UA733
MP5912	2N5912	NF4447	2N5433	PF5301-3	2N4118A	SI7135CPI	ICL7135CPI
MP7520JD	AD7520JD	NF4448	2N5433	PL1091	2N3823	SI7660	ICL7660
MP7520JN	AD7520JN	NF500	2N4224	PL1092	2N3823	SI7661	ICL7662
MP7520KD	AD7520KD	NF501	2N4224	PL1093	2N3823	SJM181BCC	JM38510/11101BCC
MP7520KN	AD7520KN	NF506	2N4416	PL1094	2N3823	SJM181BIC	JM38510/11101BIC
MP7520LD	AD7520LD	NF5101	2N4867	PM308	LM308	SJM182BCC	JM38510/11102BCC
MP7520LN	AD7520LN	NF5102	2N4867	PN3684	2N3684	SJM182BIC	JM38510/11102BIC
MP7520SD	AD7520SD	NF5103	2N4867	PN3685	2N3685	SJM184BEC	JM38510/11103BEC
MP7520TD	AD7520TD	NF511	2N4860	PN3686	2N3686	SJM185BEC	JM38510/11104BEC
MP7520UD	AD7520UD	NF5163	2N4341	PN3687	2N3687	SJM187BCC	JM38510/11105BCC
MP7521JD	AD7521JD	NF520	2N3684	PN4091	ITE4091	SJM187BIC	JM38510/11105BIC
MP7521JN	AD7521JN	NF521	2N3685	PN4092	ITE4092	SJM188BCC	JM38510/11106BCC
MP7521KD	AD7521KD	NF522	2N3686	PN4093	ITE4093	SJM188BIC	JM38510/11106BIC
MP7521KN	AD7521KN	NF523	2N3865	PN4220	J204	SJM190BEC	JM38510/11107BEC
MP7521LD	AD7521LD	NF530	2N4341	PN4221	J202	SJM191BEC	JM38510/11108BEC
MP7521LN	AD7521LN	NF5301	2N4118A	PN4222	J203	SL301AT	IT129
MP7521SD	AD7521SD	NF5301-1	2N4117A	PN4223	J204	SL301BT	IT129
MP7521TD	AD7521TD	NF5301-2	2N4118A	PN4224	J202	SL301CT	IT129
MP7521UD	AD7521UD	NF5301-3	2N4118A	PN4342	2N5461	SL301ET	IT129
MP7523JN	AD7523JN	NF531	2N4339	PN4360	2N5460	SL360C	IT129
MP7523KN	AD7523KN	NF532	2N4341	PN4391	ITE4391	SL362C	IT129
MP7523LN	AD7523LN	NF533	2N4339	PN4392	ITE4392	SM5011	ICM7050G
MP7621AD	AD7541AD	NF5457	2N5457	PN4416	ITE4416	SM5510	ICM1115B
MP7621BD	AD7541BD	NF5458	2N5458	PN4856	2N4856	SM5530B	ICM7070P
MP7621JN	AD7541JN	NF5459	2N5459	PN4857	2N4857	SU2000	2N4340
MP7621KN	AD7541KN	NF5484	2N5484	PN4858	2N4858	SU2020	2N3954
MP7621SD	AD7541SD	NF5485	2N5485	PN4859	2N4859	SU2021	2N3954
MP7621TD	AD7541TD	NF5486	2N5486	PN4860	2N4860	SU2022	2N3954
MP804	2N5520	NF5555	2N5484	PN4861	2N4861	SU2023	2N3954
MP830	2N5520	NF5638	2N5638	PN5033	2N5460	SU2024	2N3954
MP831	2N5521	NF5639	2N5639	PTC151	2N5484	SU2025	2N3954
MP832	2N5522	NF5640	2N5640	PTC152	2N5485	\$U2026	2N3954
MP833	2N5523	NF5653	2N4860	S1424	ICM1424C	\$U2027	2N3954
MP835	2N3954	NF5654	2N4861	SA2253	IT122	\$U2028	2N3954
MP836	2N3955	NF580	2N5432	SA2254	IT122	\$U2029	2N5197
MP837	2N3955	NF581	2N5432	SA2255	IT122	\$U2029	2N3954
MP838 MP839 MP840 MP841 MP842	2N3956 2N3957 2N5520 2N5521 2N5523	NF582 NF583 NF584 NF585 NF6451	2N5433 2N5434 2N5433 2N4859 U310	SA2644 SA2648 SA2710 SA2711 SA2712	IT120 IT120 IT120 IT120 IT120 IT121	SU2030 SU2030 SU2031 SU2031 SU2032	2N3955 2N3954 2N5198 2N3954 2N3954
MPF102 MPF103 MPF104 MPF105 MPF106	2N5486 2N5457 2N5458 2N5459 2N5485	NF6452 NF6453 NF6454 NKT80111 NKT80112	U310 U310 U310 U310 2N4220 2N4220	SA2713 SA2714 SA2715 SA2716 SA2717	IT121 IT122 IT120 IT120 IT120 IT121	SU2033 SU2034 SU2034 SU2035 SU2035	2N3954 2N3955 2N3954 2N3955 2N3954
MPF107	2N5486	NKT80113	2N3821	SA2718	IT122	SU2074	2N3954
MPF108	2N5486	NKT80211	2N4339	SA2719	IT120	SU2075	2N3954
MPF109	2N5484	NKT80212	2N4339	SA2720	IT121	SU2076	2N3954
MPF111	2N5458	NKT80213	2N4339	SA2721	IT122	SU2077	2N3955
MPF112	2N5458	NKT80214	2N4339	SA2721	IT120	SU2077	2N3955
MPF161 MPF208 MPF209 MPF256 MPF4391	2N5398 2N3821 2N3821 ITE4416 ITE4391	NKT80215 NKT80216 NKT80421 NKT80422 NKT80423	2N4339 2N4339 2N4220 2N4220 2N4220	SA2723 SA2724 SA2726 SA2727 SA2738	TT121 IT122 IT122 IT122 IT122 IT120A	SU2078 SU2079 SU2080 SU2081 SU2098	2N3955 2N3955 U404 U404 2N5197
MPF4392 MPF4393 MPF820 MPF970 MPF971	ITE4392 ITE4393 J310 J175 J175	NKT80424 NPC108 NPC211N NPC212N NPC213N	2N4220 2N5484 2N4338 2N4338 2N4338	SA2739 SCL54301 SCL5478 SDF1001 SDF1002	IT120 ICM1424C ICM7269 2N5432 2N5433	SU2098A SU2098B SU2099 SU2099A SU2365	2N5197 2N5196 2N5197 2N5197 2N5197 2N3954
MPS5010 MSM5001 MSM5011 MSM5977 MTF101	ICL8069 ICM7269 ICM1424C ICM1424C 2N5484	NPC214N NPC215N NPC216N NPD5564 NPD5565	2N4339 2N4339 2N4339 IT550	SDF1003 SDF500 SDF501 SDF502 SDF503	2N5434 2N5520 2N5520 2N5520 2N5520	SU2365A SU2366 SU2366A SU2367 SU2367A	2N3954 2N3955 2N3955 2N3955 2N3955
MTF102 MTF103 MTF104 ND5700 ND5701	2N5484 2N5457 2N5459 IT120A IT120A	NPD5566 NPD8301 NPD8302 NPD8303 OT3	IT550 2N3954 2N3955 2N3956 2N4338	SDF504 SDF505 SDF506 SDF507 SDF508	2N5520 2N5520 2N5520 2N5520 2N5520 2N5520	SU2368 SU2368A SU2369 SU2369A SU2410	2N3956 2N3956 2N3957 2N3957 2N3957 2N5907
ND5702	IT120	P1004	2N5116	SDF509	2N5520	SU2411	2N5908
NDF9401	IT500	P1005	2N5115	SDF510	2N3954	SU2412	2N5909
NDF9402	IT501	P1027	2N5267	SDF512	2N3954	SU2652	U401
NDF9403	IT502	P1028	2N5270	SDF513	2N3954	SU2652M	U401
NDF9404	IT503	P1029	2N5270	SDF514	2N3954	SU2653	U401
NDF9405	IT504	P1069E	2N2609	SDF661	IT122	SU2653M	U401
NDF9406	IT500	P1086E	2N5115	SDF662	IT122	SU2654	U401
NDF9407	IT501	P1087E	2N5516	SDF663	IT122	SU2654M	U401
NDF9408	IT502	P1117E	2N5640	SES3819	2N5484	SU2655	U402
NDF9409	IT503	P1118E	2N5641	SFT601	2N4338	SU2655M	U402
NDF9410	IT504	P1119E	2N5640	SFT602	2N4338	SU2656	U404
NE590	AD590	PF510	2N5115	SFT603	2N4339	SU2656M	U404
NE592	NE592	PF5101	2N4867	SFT604	2N4339	SX3819	2N5484
NF3819	2N5484	PF5102	2N4867	SG105	LM105	SX3820	2N2608
NF4302	2N5457	PF5103	2N4867	SG108	LM108	TC8031P	ICM7038A

ALTERNATE SOURCE PROD		ALTERNATE SOURCE PRODUC	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODU	INTERSIL EQUIVALENT	ALTERNAT SOURCE PROI	E INTERSIL DUCT EQUIVALENT
TC8032P TC8051P TC8052P TC8056PA TC8057P	ICM7038F ICM7038B ICM7038E ICM1115B ICM7038D	TD710 TD711 TD713 TIS14 TIS25	IT122 IT122 IT122 IT122 2N4340 2N3954	U112 U113 U114 U1177 U1178	2N2608 2N2608 2N2608 2N4220 2N3821	U285 U290 U291 U295 U296	2N5454 2N5432 2N5434 2N5432 2N5434
TD100	IT129	TIS26	2N3954	U1179	2N3821	U300	2N5114
TD101	IT129	TIS27	2N3955	U1180	2N4221	U3000	2N4341
TD102	IT129	TIS34	2N5486	U1181	2N4220	U3001	2N4339
TD200	IT129	TIS41	2N4859	U1182	2N3821	U3002	2N4338
TD201	IT129	TIS42	2N4393	U1277	2N3684	U301	2N5115
TD202 TD2219 TD224 TD225 TD226	IT129 IT129 IT122 IT122 IT122	TIS58 TIS59 TIS68 TIS69 TIS70	2N5484 2N5486 2N3955A 2N3955A 2N3956	U1278 U1279 U1280 U1281 U1282	2N3685 2N3686 2N3684 2N38822	U3010 U3011 U3012 U304 U305	2N4341 2N4340 2N4338 U304 U305
TD227	IT122	TIS73	ITE4391	U1283	2N4340	U306	U306
TD228	IT122	TIS74	ITE4392	U1284	2N4341	U308	U308
TD229	IT122	TIS75	ITE4393	U1285	2N4220	U309	U309
TD230	IT121	TIS88	2N4416	U1286	2N4341	U310	U310
TD231	IT121	TIS88A	2N4416	U1287	2N4092	U311	U310
TD232 TD233 TD234 TD235 TD236	IT122 IT122 IT122 IT122 IT122	TIXS33 TIXS35 TIXS36 TIXS41 TIXS42	2N4392 2N4857 2N4391 2N4859 2N5639	U1321 U1322 U1323 U1324 U1325	2N4860 2N3822 2N3822 2N3822 2N3687 2N3686	U312 U314 U315 U316 U317	2N5397 2N5555 2N5397 U309 U310
TD237 TD238 TD239 TD240 TD241	IT122 IT122 IT122 IT121 IT121	TIXS59 TIXS78 TIXS79 TL182CL TL182CN	2N5459 2N4341 2N4341 DGM182BA DGM182CJ	U133 U1420 U1421 U1422 U146	2N2608 2N3821 2N3822 2N3822 2N3822 2N2608	U320 U321 U322 U328 U329	2N5433 2N5434 2N5433 **
TD242 TD243 TD244 TD245 TD246	IT120A IT120A IT129 IT129 IT129	TL182IL TL182IN TL182ML TL185CJ TL185CN	DGM182BA DGM182CJ DGM182AA IH5045CJE IH5045CPE	U147 U148 U149 U168 U1714	2N2608 2N2608 2N2609 2N2609 2N2609 2N4340	U330 U331 U350 U401 U402	** ** U401 U402
TD247	IT129	TL185IJ	IH5045CJE	U1715	2N4340	U403	U403
TD248	IT129	TL185IN	IH5045CPE	U182	2N4857	U404	U404
TD250	IT120A	TL185MJ	IH5045MJE	U183	2N3824	U405	U405
TD2905	IT139	TL188CL	IH5042CTW	U1837E	2N5486	U406	U406
TD400	IT139	TL188CN	IH5042CPE	U184	2N5397	U410	2N3955
TD401		TL188IL	IH5042CTW	U1897E	U1897	U411	2N3956
TD402		TL188IN	IH5042CPE	U1898E	U1898	U412	2N3958
TD500		TL188ML	IH5042MTW	U1899E	U1899	U421	2N5908
TD501		TL191CJ	IH5043CJE	U197	2N4338	U422	2N5908
TD502		TL191CN	IH5043CPE	U198	2N4340	U423	2N5909
TD509	11132 18000	TL191IJ	IH5043CJE	U199	2N4341	U424	2N5908
TD510		TL191IN	IH5043CPE	U1994E	2N4416	U425	2N5908
TD511		TL191MJ	IH5043MJE	U200	2N4861	U426	2N5909
TD512		TL503	AD503	U201	2N4860	U430	J309(X2)
TD513		TL592	NE592	U202	2N4859	U431	J310(X2)
TD514 TD517 TD518 TD519 TD520	IT132 IT132	TLC555 TN4117 TN4117A TN4118 TN4118A	ICM7555 2N4117 2N4117A 2N4118 2N4118A	U2047E U221 U222 U231 U232	2N4416 2N4391 2N4391 U231 U232	U440 U441 UA105 UA108 UA305	IT5911 IT5912 LM105 LM108 LM305
TD521	IT139	TN4119	2N4119	U233	U233	UA308	LM308
TD522		TN4119A	2N4119A	U234	U234	UA733	UA733
TD523		TN4338	2N4338	U235	U235	UC100	2N3684
TD524		TN4339	2N4339	U240	2N5432	UC110	2N3685
TD525		TN4340	2N4340	U241	2N5433	UC115	2N4340
TD526	IT132	TN4341	2N4341	U242		UC120	2N3686
TD527	IT131	TN5277	2N4341	U243		UC130	2N3687
TD528	IT131	TN5278	2N4341	U244		UC155	2N4416
TD5432	2N5432	TP5114	2N5114	U248		UC1700	3N163
TD5433	2N5433	TP5115	2N5115	U248		UC1764	3N163
TD5434	2N5434	TP5116	2N5116	U249	2N5903	UC20	2N3686
TD550	IT129	TSC426	ICL7667	U249A	2N5907	UC200	2N3824
TD5902	2N5902	TSC7106CJL	ICL7106CJL	U250	2N5904	UC201	2N3824
TD5902A	2N5902	TSC7106CPL	ICL7106CPL	U250A	2N5908	UC21	2N3687
TD5903	2N5903	TSC7106RCPL	ICL7106RCPL	U251	2N5905	UC21	2N4416
TD5903A	2N5903	TSC7107CJL	ICL7107CJL	U251A	2N5909	UC2130	2N5452
TD5904	2N5904	TSC7107CPL	ICL7107CPL	U252	IT5911	UC2132	2N5453
TD5904A	2N5904	TSC7107RCPL	ICL7107RCPL	U253	IT5912	UC2134	2N5454
TD5905	2N5905	TSC7109CPL	ICL7109CPL	U254	2N4859	UC2136	2N5454
TD5905A	2N5905	TSC7109IJL	ICL7109IJL	U255	2N4860	UC2138	2N5454
TD5906 TD5906A TD5907 TD5907A TD5908		TSC7109MJL TSC7116CJL TSC7116CPL TSC7117CJL TSC7117CPL	ICL7109MJL ICL7116CJL ICL7116CPL ICL7117CJL ICL7117CPL	U256 U257 U257/TO-71 U266 U273	2N4861 U257 U257/TO-71 2N4856 2N4118A	UC2139 UC2147 UC2148 UC2149 UC220	2N3958 2N3958 2N3958 2N3958 2N3958 2N3822
TD5908A	2N5909	TSC7126CJL	ICL7126CJL	U273A	2N4118A	UC240	2N4869
TD5909		TSC7126RCPL	ICL7126RCPL	U274	2N4119A	UC241	2N4869
TD5909A		TSC7135CJI	ICL7135CJI	U274A	2N4119A	UC250	2N4091
TD5911		TSC7135CPI	ICL7135CPI	U275	2N4119A	UC251	2N4392
TD5911A		TSC7650	ICL7650	U275A	2N4119A	UC2766	3N166
TD5912	IT5912	TSC7660	ICL7660	U280	2N5452	UC300	2N2607
TD5912A	IT5912	TSC9491	ICL8069	U281	2N5453	UC310	
TD700	IT122	TT-590	AD590	U282	2N5453	UC320	
TD701	IT122	U110	2N2608	U283	2N5453	UC330	
TD709	IT122	U111	2N2608	U284	2N5454	UC340	

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
UC40 UC400 UC401 UC411 UC410	2N2608 2N5270 2N5116 2N2608 2N5268						
UC420 UC450 UC451 UC588 UC703	2N5267 2N5114 2N5116 2N4416 2N4220						
UC704 UC705 UC707 UC714 UC714E	2N4220 2N4224 2N4860 2N3822 2N4341						
UC734 UC734E UC751 UC752 UC753	2N4416 2N4416 2N4340 2N4340 2N4341						
UC754 UC755 UC756 UC805 UC807	2N4340 2N4341 2N4340 2N5270 2N5115						
UC814 UC851 UC853 UC854 UC855	2N5270 2N2608 2N2608 2N2608 2N2608 2N2609						
UCN-4111M UCN-4112M UCN-4113M UHP-503 UPD1952P	ICM7038C ICM7051A ICM7038B AD503 ICM7220MFA						
UPD1962C UPD1963C UPD815C UPD816C UPD820C	ICM7050G ICM7050 ICM7038E ICM7038B ICM1115B						
UPD833G UT100 UT101 UXC2910 VCR10N	ICM7223 2N5397 2N5397 IT126 2N4869						
VCR11N VCR12N VCR13N VCR20N VCR2N	VNR11N 2N3958 2N3958 2N4341 VCR2N						
VCR3P VCR4N VCR5P VCR6P VCR7N	VCR2P VCR4N VCR5P VCR6P VCR7N						
VF28 VF811 VF815 VFW40 VFW40A	2N4392 2N4858 2N4858 IT122 IT120						
VR-8069 W245A W245B W245C W300	ICL8069 ITE4416 ITE4416 ITE4416 2N5398		Y				
W300A W300B W300C W300D WG-8038	2N5397 2N5397 2N5397 2N5398 ICL8038						
WK5457 WK5458 WK5459 XR8038 ZDT40	2N5457 2N5458 2N5459 ICL8038 IT129						
ZDT41 ZDT42 ZDT44 ZDT45	IT129 IT129 IT129 IT129						

TISHETAL STANFILLS THEFTAL TOUGHS EDEDGE	MANAGE STANSFELA THRUSHER TOUGHER SOUGH	

#### Section 1 — Selector Guides

Section 1 - Selector Guides



Switches—Junction FET N Channel

PART	PACKAGE	rDS(ON) Ω Max	V <sub>P</sub> V Min	Max	IGSS pA Max	BV <sub>GSS</sub> V Min	D(OFF) PA Max	DSS mA Min	Max	t <sub>ap</sub> ns Max	C <sub>rss</sub> pF Max	C <sub>iss</sub> pF Max	COMMENTS
2N3824	Salaka da S	250		8.0	-100	-50		- 200	0.01	- (1)	3	6	High Isolation
	TO-18	30 8	-4.0	-10.0	-250	-40	250	50	150	50	6 08	25	High Isolation
		60	-2.0	-5.0	-250	-40	250	25	75	90	6 08	25	High Isolation
2N3971													
2N3972	TO-18	100	-0.5	-3.0	-250	-40	250	5	30	180	6	25	High Isolation
* 2N4091	TO-18	30	-5.0	-10.0	-200	-40	200	30		65	5	16	High Isolation
2N4091A	TO-18	30	-5.0	-10.0	-40	-50	200	30		65	5	16	High Isolation
* 2N4092	TO-18	50 8	-2.0	-7.0	-200	-40	200	15		95	5	16	High Isolation
2N4092A	TO-18	50	-2.0	-7.0	40	-50	200	15		95	75 6	16	High Isolation
* 2N4093	TO-18	80	-1.0	-5.0	-200	-40	200	8		140	5 00	16	High Isolation
2N4093A	TO-18	80	-1.0	-5.0	40	-50	200	8	aat	140	5	16	High Isolation
	TO-18	30 🖟	-4.0	-10.0	-100	-40	100	50	150	55	3.5	14	High Isolation
2N4392		60	-2.0	-5.0	-100	-40	100	25	75	75	3.5	14	High Isolation
2N4393	TO-18	100	-0.5	-3.0	-100	-40	100	5	30	100	3.5	14	High Isolation
* 2N4856	TO-18	25	-4.0	-10.0	-250	-40	250	50		34	8	18	High Isolation
* 2N4857	TO-18	40	-2.0	-6.0	-250	-40	250	20	100	60	8	18	High Isolation
* 2N4858	TO-18	60	-0.8	-4.0	-250	-40	250	8	80	120	8	18	High Isolation
* 2N4859	TO-18	25	-4.0	-10.0	-250	-30	250	50		34	8	18	High Isolation
* 2N4860	TO-18	40	-2.0	-6.0	-250	-30	250	20	100	60	8	18	High Isolation
* 2N4861	TO-18	60	-0.8	-4.0	-250	-30	250	8	80	120	8	18	High Isolation
2N4978	TO-18	20	-2.0	-8.0	-500	-30	500	15		55	8	35	Low r <sub>DS(ON)</sub>
2N5432	TO-52	5	-4.0	-10.0	-200	-25	200	150		41	15	30	Low r <sub>DS(ON)</sub>
2N5433	TO-52	7	-3.0	-9.0	-200	-25	200	100		41	15	30	Low r <sub>DS(ON)</sub>
2N5434	TO-52	10	-1.0	-4.0	-200	-25	200	30		41	15	30	Low r <sub>DS(ON)</sub>
2N5555	TO-92	150		-10.0	-1nA	-25	10nA	15		35	1.2	5	Low Cost
2N5638	TO-92	30		-12.0	-1nA	-30	1nA	50		24	4	10	Low Cost
2N5639	TO-92	60		-8.0	-1nA	-30	1nA	25		44	4	10	Low Cost
2N5640	TO-92	100		-6.0	-1nA	-30	1nA	5		63	4	10	Low Cost
2N5653	TO-92	50		-12.0	-1nA	-30	1nA	40		24	3.5	10	Low Cost
2N5654	TO-92	100		-8.0	-1nA	-30	1nA	15		44	3.5	10	Low Cost
ITE4091	TO-92	30	-5.0	-10.0	-200	-40	200	30		65	5	16	Low Cost
ITE4092	TO-92	50	-2.0	-7.0	-200	-40	200	15		95	5	16	Low Cost
ITE4093	TO-92	80	-1.0	-5.0	-200	-40	200	8		140	5	16	Low Cost
ITE4391	TO-92	30	-4.0	-10.0	-100	-40	100	50	150	55	3.5	14	Low Cost
ITE4392	TO-92	60	-2.0	-5.0	-100	-40	100	25	75	75	3.5	14	Low Cost
ITE4393	TO-92	100	-0.5	-3.0	-100	-40	100	5	30	100	3.5	14	Low Cost
J105	TO-92	3	-4.5	-10.0	-3nA	-25	3nA	500		20			Lowest r <sub>DS(ON)</sub>
J106	TO-92	6	-2.0	-6.0	-3nA	-25	3nA	200		20			Lowest r <sub>DS(ON)</sub>
J107	TO-92	8	-0.5	-4.5	-3nA	-25	3nA	100		20			Lowest r <sub>DS(ON)</sub>
J108	TO-92	8	-3.0	-10.0	-3nA	-25	3nA	80		41			Low Cost
J109	TO-92	12	-2.0	-6.0	-3nA	-25	3nA	40		41			Low Cost
J110	TO-92	18	-0.5	-4.0	-3nA	-25	3nA	10		41			Low Cost
J111	TO-92	30	-3.0	-10.0	-1nA	-35	1nA	20		48			Lowest Cost
J112	TO-92	50	-1.0	-5.0	-1nA	-35	1nA	5		48			Lowest Cost
J113	TO-92	100	-0.5	-3.0	-1nA	-35	1nA	2		48			Lowest Cost
J114	TO-92	150		-10.0	-1nA	-25	1nA	15		26			Low Cost

<sup>\*</sup>Also available as JAN/JANTX & JANTXV

<sup>\*\*</sup>Most TO-92's are available lead formed to a TO-18 or TO-5 configuration

#### Switches—Junction FET N Channel

PART			DS(ON)	V <sub>P</sub>		IGSS pA	BV <sub>GSS</sub>	ID(OFF) pA	I <sub>DSS</sub> mA		t <sub>ap</sub>	C <sub>rss</sub>	pF		PART
NUMBER P	ACKAG	E	Max	Min	Max	Max	Min	Max	Min	Max	Max	Max	Max	COMM	ENIS
PN4091	TO-92	0	30	-5.0	-10.0	-200	-40	200	30 -		65	5088	16	Low Cost	
PN4092	TO-92		50	-2.0	-7.0	-200	-40	200	15-		95	5	16	Low Cost	
PN4093	TO-92		80 8	-1.0	-5.0	-200	-40	200	8		140	5 08	16	Low Cost	
PN5432	TO-92		5	-4.0	-10.0	-200	-25	200	150		41	15	30	Lowest r	2013972
PN5433	TO-92		7	-3.0	-9.0	-200	-25	200	100		41	15	30	Lowest r	S(ON)
PN5434	TO-92		10	-1.0	-4.0	-200	-25	200	30		41	15	30	Lowest r	S(ON)
U200			150	-0.5	-3.0	-1nA	-30	InA	3.	25		8 08		Low Cost	
U201 obsidel			75	-1.5	-5.0	-1nA	-30	Ant	15	75		8 00		Low Cost	
U202 staloel			50	-3.5	-10.0	-1nA	-30	1nA	30	150		8 08	30	Low Cost	
U1897	TO-92		30	-5.0	-10.0	-400	-40	200	30		65	5 08	16	Low Cost	
U1898	TO-92		50	-2.0	-7.0	-400	-40	200	15 -		95	5 06	16	Low Cost	
U1899	TO-92		80	-1.0	-5.0	-400	-40	200	8		140	5 08	16	Low Cost	
Isolation		AN	3.6	091	30	. a	001	V 044-	001-	0.6-	8.0-	100		8E-01	SNEASSS
Iso available a															
Most TO-92's a															
teoC															

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"Most TO-92's are evallable lead formed to a TO-18 or TO-5 configuration

PART NUMBER	PACKAGE	r <sub>DS(ON)</sub> Ω Max	V <sub>p</sub> V Min	Max	I <sub>GSS</sub> pA Max	BV <sub>GSS</sub> V Min	I <sub>D(OFF)</sub> pA Max	IDSS mA Min	Max	t <sub>ap</sub> ns Max	C <sub>rss</sub> pF Max	C <sub>iss</sub>	COMMENTS
2N3382	TO-72	300	1.0	5.0	15nA	30	-2nA	18 -3	-30	Max		16 typ	Low r <sub>DS(ON)</sub>
2N3384	TO-72	180	4.0	5.0	15nA	30	-2nA	-15	-30			16 typ	Low r <sub>DS(ON)</sub>
2N3386	TO-72	150	4.0	9.5	15nA	30	-2.5nA	-15	-50			16 typ	Low r <sub>DS(ON)</sub>
3	hight right		OF .	200		or .	10	Andt			1		STOT TOTAL
2N3993	TO-72	150	4.0	9.5	1.2nA	25	01-1.2nA	An -10				16	
2N3994	TO-72	300	1.0	5.5	1.2nA	25	-1.2nA	-2			4.5	16	
2N5018	TO-18	75		12.0	2nA	30	-10nA	-10		100	10	45	TOVE TOVE
	TO-18	150		7.0	2nA	30	-10nA	-10		215		45	Low ros(ON)
	tooni rigilit	130		7.0	ZIIA	30	- IOHA	ABOL		210	10	45	Low rDS(ON)
* 2N5114	TO-18	75	5.0	10.0	500	30	-500	-30	-90	37	7		Low r <sub>DS(ON)</sub>
* 2N5115	TO-18	100	3.0	6.0	500	30	-500	-15	-60	66	7	25	Low r <sub>DS(ON)</sub>
* 2N5116	TO-18	150	1.0	4.0	500	30	-500	-5	-25	102	7	25	Low r <sub>DS(ON)</sub>
IT100	TO-18	75	2.0	4.5	200	35	-100	-10			12	35	TTL Compatible
IT101	TO-18	60	4.0	10.0	200	35	-100	-20			12	35	TTL Compatible
J174	TO-92	85	5.0	10.0	1nA	30	-1nA	-20	-100	22			Low Cost
J175	TO-92	125	3.0	6.0	1nA	30	-1nA	-7	-60	45			Low Cost
J176	TO-92	250	1.0	4.0	1nA	30	-1nA	-2	-25	70			Low Cost
J177	TO-92	300	0.8	2.25	1nA	30	-1nA	-1.5	-20	90			TTL Compatible
PN5114	TO-92	75	5.0	10.0	500	30	-500	-30	-90	37	7	25	Low Cost
PN5115	TO-92	100	3.0	6.0	500	30	-500	-15	-60	68	7	25	Low Cost
PN5116	TO-92	150	1.0	4.0	500	30	-500	-5	-25	102	7	25	Low Cost
U304	TO-18	85	5.0	10.0	500	30	-500	-30	-90	70	7 V	27	High Off Isolation
U305	TO-18	110	3.0	6.0	500	30	-500	-15	-60	105	7	27	High Off Isolation
U306	TO-18	175	1.0	4.0	500	30	-500	-5	-25	140	7	27	High Off Isolation

<sup>\*</sup>Also available as JAN/JANTX & JANTXV

PART (PART TO 71 OR) (PART OF TO 70 OR)

<sup>\*\*</sup>Most TO-92's are available lead formed to a TO-18 or TO-5 configuration



Switches and Amplifiers — MOSFET N-Channel

PART		VGS(TH)		BV <sub>DSS</sub>	I <sub>DSS</sub>		I <sub>GSS</sub>		9fs µmho	rDS(ON)	I <sub>D(ON)</sub>	I <sub>D(ON)</sub>	
	PACKAGE	Min	Max	Min	Max	ACS	Max	(E	Min	Max	Min	Max	COMMENTS
2N4351	TO-72	1.0	5.0	25	10nA	-20A	10	30	1000	300	3	CBT DBF	High Input Z
3N170	TO-72	1.0	2.0	25	10nA		10		1000	200	10		High Input Z
3N171	TO-72	1.5	3.0	25	10nA		10		1000	200	10		High Input Z
IT1750	TO-72	0.5	3.0	25	10nA		10		3000	50	10		Low ros(ON)
M116	TO-72	1.0	5.0	30	10nA		100			100			Diode Protected
M117	TO-72	1.0	5.0	30	10nA		1			100			High Input Z

#### 

Generally used where max, isolation between signal source and logic drive is required; switch "On" resistance varies with signal amplitude.

PART NUMBER	PACKAGE	V <sub>GS(TH)</sub> V Min	Max	BV <sub>DSS</sub> V Min	I <sub>DSS</sub> pA Max	IGSS pA Max	9fs μmho Min	r <sub>DS(ON)</sub> Ω Max	I <sub>D(ON)</sub> mA Min	I <sub>D(ON)</sub> mA Max	COMMENTS
2N4352	TO-72	-1.0	-5.0	-25	-10nA	10	1000	600	-3	0.0	High Input Z
3N155	TO-72	-1.5	-3.2	-35	-1nA	10	1000	600	(TVA-5)		High Input Z
3N155A	TO-72	-1.5	-3.2	-35	-250	10	1000	300	5 b		High Input Z
3N157	TO-72	-1.5	-3.2	-35	-1nA	10	1000		-5		High Input Z
3N157A	TO-72	-1.5	-3.2	-50	-250	10	1000		-5		High Input Z
3N161	TO-72	-1.5	-5.0	-25	-10nA	-100	3500		-40	-120	Diode Protected
3N163	TO-72	-2.0	-5.0	-40	-200	-10	2000	250	-5	-30	High Input Z
3N164	TO-72	-2.0	-5.0	-30	400	10	1000	300	-3	-30	High Input Z
3N172	TO-72	-2.0	-5.0	-40	-400	- 200		250	-5	-30	Diode Protected
3N173	TO-72	-2.0	-5.0	-30	-10nA	-500		350	-5	-30	Diode Protected
IT1700	TO-72	-2.0	-5.0	-40	200		2000	400	-2		High Input Z
IT1701	TO-72	-2.0	-5.0	-40	200	100	2000	400	-2		Diode Protected

#### Low Leakage Diodes

		I <sub>R</sub> @ 1V	I <sub>R</sub> @ 10 V, 125°C	BVR@ 1µA	V <sub>F</sub> @ 1	0mA	
PART NUMBER	PACKAGE	(pA) Typ	(nA) Max	(V) Min	(V) Min	(V) Max	COMMENTS
ID100	TO-78	0.1	10	30	0.8	1.1	(Note 1)
ID101	TO-71	0.1	10	30	0.8	1.1	(Note 1)

Note 1. Used to protect the inputs of MOSFETs such as 3N163, while maintaining input leakage < 0.1pA.

<sup>\*</sup>Also available as JAN/JANTX & JANTXV.

<sup>\*\*</sup>Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.



Amplifiers — Junction FET

N Channel

PART NUMBER PA	CKAGE	9fs μmho Min	I <sub>DSS</sub> mA Min	Max	V <sub>P</sub> V Min	Max	I <sub>GSS</sub> pA Max	BV <sub>GS</sub>	pF Max	C <sub>rss</sub> pF Max	e <sub>n</sub> nV/√Hz Max	COMMENTS
I-Channel:	HV			1 87	35 -	808-	-7.0	1.5	- 0.	14	1A. 002A	BOT COEL
TRUE WOLLDAND	HV SHIM	0000	0.5	7.5	0.0	Ani	100	0.1-	. 0	0.0	450 0 0011	COT Notice Code
	TO-72	2000	2.5	7.5	-2.0	-5.0	-100	-50	4 (1)		150 @ 20Hz	Low Noise
	TO-72	1500	1.0	3.0	-1.0	-3.5	-100	-50	4	1.2	150 @ 20Hz	Low Noise
2N3686 1	TO-72	1000		1.2	-0.6 -0.3	-2.0	-100	-50 -50		1.2	150 @ 20Hz 150 @ 20Hz	Low Noise
2N3087	0-72	500		0.5	-0.3	-1.2	-100	-50	9 01		150 @ 2012	LOW NOISE
* 2N3821 1	TO-72	1500	0.5	2.5		-4.0	-100	-50	6		200 @ 10Hz	GPA
2N3822	TO-72	3000	2.0	10.0		-6.0	-100	-50	6		200 @ 10Hz	GPA GPA
2N3823	ГО-72	3500	4.0	20.0	-1.0	-7.5	-500	-30	6	2	2.5dB @ 100MHz	VHF Amp
2N4117	TO-72	70	0.03	0.09	-0.6	-1.8	-10	-40	3	1.0		Low Leakage
2N4117A	TO-72	70	0.03	0.09	-0.6	-1.8	-90-	-40	3	1.5		Low Leakage
2N4118	TO-72	80	0.08	0.24	-1.0	-3.0	-10	-40	3	1.5		Low Leakage
2N4118A	rO-72	80	0.06	0.24	-1.0	-3.0	-9-8-	-40	3	1.5		Low Leakage
2N4119 7	ГО-72	100	0.2	0.6	-2.0	-6.0	-10	-40	3	1.5		Low Leakage
2N4119A	ГО-72	100	0.2	0.6	-2.0	-6.0	-1_	-40	3	4 5	2 10,000 12	Low Leakage
2N4220	TO-72	1000	0.5	3.0		-4.0	-100	-30	6	2		Low Cost
	TO-72	1000	0.5	3.0		-4.0	-100	-30	6	2	2.5dB @ 100Hz	GPA
2N4221 T	ГО-72	2000	2.0	6.0		-6.0	-100	-30	6	2	NA.	Low Cost
	ГО-72	2000	2.0	6.0		-6.0	-100	-30	6	2	2.5dB @ 100Hz	GPA
2N4222 T	ГО-72	2500	5.0	15.0		-8.0	-100	-30	6	2		Low Cost
2N4222A 1	0-72	2500	5.0	15.0		-8.0	-100	-30	6	2	2.5dB @ 100Hz	GPA
2N4223 1	TO-72	3000	3.0	18.0	-0.1	-8.0	-250	-30	6	2		Low Cost
2N4224	ГО-72	2000	2.0	20.0	-0.1	-0.8	-150	-30	6	2		Low Cost
2N4338 1	TO-18	600	0.2	0.6	-0.3	-1.0	-100	-50	7	3	65 @ 1kHz	General Purpose Am
2N4339 1	ГО-18	800 -	0.5	1.5	-0.6	-1.8	-100	-50	7	3	65 @ 1kHz	General Purpose Am
2N4340 1	ГО-18	1300	1.2	3.6	-1.0	-3.0	-100	-50	7	3	65 @ 1kHz	General Purpose Am
2N4341 7	ГО-18	2000	3.0	9.0	-2.0	-6.0	-100	-50	7	3	65 @ 1kHz	General Purpose Am
2N4416	ГО-72	4500	5.0	15.0		-6.0	-100	-30	4	2		High Gain
2N4867	TO-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5	10 @ 1kHz	Audio Amp
2N4867A	ГО-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5	5 @ 1kHz	Low Noise/GPA
2N4868 7	TO-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5	10 @ 1kHz	Audio Amp
2N4868A 1	ГО-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5	5 @ 1kHz	Low Noise/GPA
2N4869	ГО-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5	10 @ 1kHz	Audio Amp
2N4869A	ГО-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5	5 @ 1kHz	Low Noise/GPA
2N5397 1	ГО-72	6000	10.0	30.0	-1.0	-6.0	-100	-25	5.0	1.2	3.5dB @ 450MHz	VHF Amp
2N5398	ГО-72	5500	5.0	40.0	-1.0	-6.0	-100	-25	5.5	1.3		VHF Amp
2N5457	ГО-92	1000	1.0	5.0	-0.5	-6.0	-1nA	- 25	7	3	3dB @ 1kHz	Low Cost/GPA
2N5458	ГО-92	1500	2.0	9.0	-1.0	-7.0	-1nA	- 25	7	3	3dB @ 1kHz	Low Cost/GPA
2N5459 1	ГО-92	2000	4.0	16.0	-2.0	-8.0	-1nA	-25	7	3	3dB @ 1kHz	Low Cost/GPA
2N5484	ГО-92.	3000	1.0	5.0	-0.3	-0.3	-1nA	-25	5	- 1	120 @ 1kHz	Low Cost RF Amp
2N5485	ГО-92	3500	4.0	10.0	-0.5	-4.0	-1nA	-25	5	1	120 @ 1kHz	Low Cost RF Amp
2N5486	ГО-92	4000	8.0	20.0	-2.0	-6.0	-1nA	- 25	5	1	120 @ 1kHz	Low Cost RF Amp
ITE4416 1	ГО-92	4500	5.0	15.0		-6.0	100	-30	4	2		Low Cost RF Amp
J201 7	ГО-92	500	0.2	1.0	-0.3	-1.5	-100	-40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J202 1	ГО-92	1000	0.9	4.5	-0.8	-4.0	-100	-40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J203 1	ГО-92	1500	4.0	20.0	-2.0	-10.0	-100	-40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J204 7	TO-92				-0.5	-2.0	-100	-25	4typ.	1typ.	10typ.@ 1kHz	GPA/Low Cost
J210 T	ГО-92	4000	2.0	15.0	-1.0	-3.0	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J211 7	TO-92	7000	7.0	20.0	-2.5	-4.5	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J212 7	ГО-92	7000	15.0	40.0	-4.0	-6.0	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost

<sup>\*</sup>Available as JAN/TX/TXV.

<sup>\*\*</sup>Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.



Amplifiers — Junction FET

PART NUMBER P	ACKAG	9fs μmho E Min	I <sub>DSS</sub> mA Min	Max	V <sub>P</sub> V Min	Max	I <sub>GSS</sub> pA Max	BV <sub>GSS</sub> V Min	C <sub>iss</sub> pF Max	C <sub>rss</sub> pF Max	e <sub>n</sub> nV/√Hz Max	COMMENTS
J300	TO-92	4500	4.0	45.0	-1.5	-7.0	-500	-25	5.5	1.7		VHF AMP/Low Co
J308	TO-92	8000	12.0	60.0	-1.0	-6.5	-1nA	-25			2.7dB @ 450MHz	VHF Amp/Low Co
J309 886M	TO-92	10,000	12.0	30.0	-1.0	-4.0	-1nA	-25			2.7dB @ 450MHz	VHF Amp/Low Co
J310 981014	TO-92	8000	24.0	60.0	-2.0	-6.5	-1nA	-25		0.3	2.7dB @ 450MHz	VHF Amp/Low Co
PN4302	TO-92	1000	0.5	5.0	68-	-4.0	- 1nA	-30	6	2	200	A/Low Cost
PN4303	TO-92	2000	4.0	10.0		-6.0	-1nA	-30	6	2	2dB @ 1kHz	¿PA/Low Cost
PN4304	TO-92	1000	0.5	15.0		-10.0	-1nA	-30	6	2	3dB @ 1kHz	GPA/Low Cost
PN4338	TO-92	600	0.2	0.6	-0.3	-1.0	-100	-50	7 0.0	3	1dB @ 1kHz	GPA/VCR
PN4339	TO-92	800	0.5	1.5	-0.6	-1.8	-100	-50	7 00	3	1db @ 1kHz	GPANCR
PN4340	TO-92	1300	1.2	3.6	-1.0	-3.0	-100	-50	7	3	1db @ 1kHz	GPAVCR
PN4341	TO-92	2000	3.0	9.0	-2.0	-6.0	-100	-50	7		1db @ 1kHZ	GPA/VCR
PN4416	TO-92	4500	5.0	15.0		-6.0	-100	-30	4			High Gain/Low Co
PN5163	TO-92	2000	1.0	40.0	-0.4	-8.0_	-10nA	-25	20			Low Cost
U308	TO-52	10,000	12.0	60.0	-1.0	-6.0	-150	-25	7typ.	1.0typ. 2	2.7dB @ 450MHz	VHF Amp
U309	TO-52	10,000	12.0	30.0	-1.0	-4.0	-150	-25	7typ.	1.0typ. 2	2.7dB @ 450MHz	VHF Amp
U310	TO-52	10,000	24.0	60.0	-2.5	-6.0	-150	-25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp
ailable as JAI	N/TY/TY	NOOT to Sha.	977	0 2	-30	661	0.4-		0.0	3.5	0001 9	NOT NOSSAIRS
		ible lead forme	of he	a TO-18 or	TO-5 CO	nfiguratio	n 0.8-					
031 10-02 3 41	Cavano	ibic icad ioiiii	50 10	4 10 10 01	00-	inigulatio	0.9-					
				8 8								
												2N4222A TO-77

P-Channel								0.101	13036742	HAUL IN		
PART NUMBER	PACKAGE	9fs μmho E Min	DSS mA Min	Max	V <sub>P</sub> V Min	Max	IGSS nA Max	BV <sub>GSS</sub> V Min	C <sub>iss</sub> pF Max	C <sub>rss</sub> pF Max	e <sub>n</sub> nV/√Hz Max	TRAS COMMENTS
2N2606	TO-18	110	0.00.1	-0.5	0.5	4.0	os_1nA	30	6	DI	3dB@1kHz	VP Min Waiver
2N2607	TO-18	330	0.0-0.3	-1.5	1.0	4.0	3nA	30	10		400@1kHz	Low Noise/GPA
2N2608	TO-18	01000	0.8-0.9	-4.5	1.0	4.0	10nA	30	17		180@1kHz	Low Noise/GPA
2N2609	TO-18	2500	-2.0	-10.0	1.0	4.0	30nA	30	30		180@1kHz	Low Noise/GPA
2N2609JAN	TO-18	2500	8-2.0	10.0	1.0	4.0	30nA	30	30		3dB@1kHz	Low Noise/GPA
2N3328	TO-72	100		8.0_1.0		6.0	1nA	20	4		400@1kHZ	GPA ALBERTA
2N3329	TO-72	1000	-1.0	-3.0		5.0	10nA	20	20		3db@1kHz	GPA
2N3330	TO-72	1500	-2.0	-6.0		6.0	10nA	20	20		3db@1kHz	GPA
2N3331	TO-72	2000	-5.0	-15.0		8.0	10nA	20	20		4db@1kHz	GPA
2N3332	TO-72	1000	0.8-1.0	-6.0		6.0	10nA	20	20		1db@1kHz	GPA andaus
2N5265	TO-72	900	0.8_0.5	-1.0	0.3	1.5	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5266	TO-72	1000	0.8-0.8	-1.6	0.4	2.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5267	TO 70	1500	-1.5		1.0	4.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5268	TO-72	2000	-2.5	-5.0	1.0	4.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5269	TO-72	2200	-4.0	-8.0	2.0	6.0	2nA	60	7	200	115@100Hz	Low Noise/GPA
2N5270	TO-72	2500	0.7-7.0	-14.0	2.0	6.0	2nA	60	7 -	2	115@100Hz	Low Noise/GPA
2N5460	TO-92	1000	-1.0	-5.0	0.75	6.0	5nA	40	7	2	115@100Hz	Low Noise/Low Co
2N5461	TO-92	1500	-2.0	-9.0	1.0	7.5	5nA	40	7	2	115@100Hz	Low Noise/Low Co
2N5462	TO-92	2500	-4.0	-16.0	1.8	9.0	5nA	40	7 -	2	115@100Hz	Low Noise/Low Co
2N5463	TO-92	1000	8.1-1.0	a -5.0	0.75	6.0	5nA	60	7	2	115@100Hz	Low Noise/Low Co
2N5464	TO-92	1500	-2.0	ar-9.0	1.0	7.5	5nA	60	7	208	115 100Hz	Low Noise/Low Co
2N5465	TO-92	2500	-4.0	-16.0	1.8	9.0	5nA	60	7/-	23	115@100Hz	Low Noise/Low Co
J270	TO-92	6000	-2.0	-15.0	0.5	2.0	0.200	30	32typ	4typ	6typ@1kHZ	Low Noise/Low Cos
J271	TO-92	8000	-6.0	-50.0	1.5	4.5	0.200	30	31typ	4typ	6typ@1kHz	Low Noise/Low Cos
PN4342	TO-92	2000	-4.0	-12.0	0.7	5.0	10nA	25	20	508	80@100Hz	Low Noise/Low Co
PN4343	TO-92	3000	010.0	-30.0	₿ 1.8	8.19.0	10nA	25	20	501	80@100Hz	Low Noise/Low Co
	1000	100000	10.10	200	1/2	- 15 S	NAME OF STREET	P. S.	100	100	73.6	PACIFIC DA SULLIFO

<sup>\*</sup>Available as JAN/TX/TXV.

<sup>\*\*</sup>Most TO-92's are available lead formed to a TO-18 or TO-5 configuration.



Differential Amplifiers —
Dual Monolithic N-Channel Junction FETs

PART		V <sub>GS1-2</sub> mV	ΔV <sub>GS</sub> μV/°C	I <sub>G</sub>	BVGSS	V <sub>P</sub>		9fs mmho*		DSS mA		e <sub>n</sub> nV/√Hz	
	PACKAGE	Max	Max	Max	Min	MinXax	Max	Min	Max	Min	Max	Max	COMMENTS
2N3921	TO-71	5	10	250	-50	Anl	-3.0	0.1.5	7.5	1	10.0	2dB @ 1kHz	GP Diff Amp
2N3922	TO-71	5	25	250	-50		-3.0	1.5	7.5	1	10.0	2dB @ 1kHz	GP Diff Amp
2N3954	TO-71	5	10	-50	-50	-1.0	-4.5	0 1	0.1 3 6	0.5	5.0	160 @ 100Hz	General Purpos
2N3954A	TO-71	5	5	-50	-50	-1.0	-4.5	0.1	0.1 3 0.0	0.5	5.0	160 @ 100Hz	General Purpos
2N3955	TO-71	10	25	-50	-50	-1.0	-4.5	0.8 1	01300	0.5	5.0	160 @ 100Hz	General Purpos
2N3955A	TO-71	5	15	-50	-50	-1.0	-4.5	0.01	3	0.5	5.0	160 @ 100Hz	General Purpos
2N3956	TO-71	15	50	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpos
2N3957	TO-71	20	75	-50	-50	-1.0	-4.5	1	3	OF	5.0	160 @ 100Hz	General Purpos
2N3958	TO-71	25	100	-50	-50	-1.0	-4.5	1	3 0	0.5	5.0	160 @ 100Hz	General Purpos
2N5045	TO-71	bit Sibt	65		-50	-0.5	-4.5	0.81.5	6.0	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5046	TO-71	10	133		-50	-0.5	-4.5	1.5	6.0	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5047	TO-71	15	200		-50	-0.5	-4.5	1.5	6.0	0.5	8.0	70-72 1000	GP Diff Amp
2N5196	TO-71	0015011	5 \$	-15	-50	-0.7	-4.0	0.7 @	200μΑ	0.7	7.0	20 @ 1kHz	Low Noise, GP
2N5197	TO-71	001 5 arr	10	-15	-50	-0.7	-4.0	0.7 @	200μΑ	0.7	7.0	20 @ 1kHz	Low Noise, GP
2N5198	TO-71	00 10	20	-15	-50	-0.7	-4.0	0.7 @	200μΑ	0.7	7.0	20 @ 1kHz	Low Noise, GP
2N5199	TO-71	15	40	-15	-50	-0.7	-4.0	0.7 @	200μΑ	0.7	7.0	20 @ 1kHz	Low Noise, GP
2N5515	TO-71	0015	5	-100	-40	-0.7	-4.0	0.8 1	81.04 0	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5516	TO-71	001 5 81	10	-100	-40	-0.7	-4.0	1.55	0140	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5517	TO-71	10	20	-100	-40	-0.7	-4.0	001	81 4 08	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5518	TO-71	15	40	-100	-40	-0.7	-4.0	0.8 1	37.04 0	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5519	TO-71	15	80	-100	-40	-0.7	-4.0	451	81 4 0	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5520	TO-71	001 5 611	5	-100	-40	-0.7	-4.0	0.61	8 4 0	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5521	TO-71	5	10	-100	-40	-0.7	-4.0	ac 1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5522	TO-71	10	20	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5523	TO-71	15	40	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5524	TO-71	100 115 08	80	-100	-40	-0.7	-4.0	0.01	10 4 03	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5545	TO-71	10015 08	10	-50	-50	-0.5	-4.5	0.81.5	01600	0.5	8.0	180 @ 10Hz	GP Diff Amp
2N5546	TO-71	10	20	-50	-50	-0.5	-4.5	1.5	6	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5547	TO-71	15	40	-50	-50	-0.5	-4.5	1.5	6	0.5	8.0		GP Diff Amp
2N5902	TO-78	5	5	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5903	TO-78	5	10	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5904	TO-78	10	20	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5905	TO-78	15	40	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5906	TO-99	5	5	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5907	TO-99	5	10	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5908	TO-99	10	20	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5909	TO-99	15	40	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5911	TO-99	10	20	-100	-25	-1.0	-5.0	5/10	@ 5mA	7.0	40.0	20 @ 10kHz	RF Amplifier
2N5912	TO-99	15	40	-100	-25	-1.0	-5.0	5/10	@ 5mA	7.0	40.0	20 @ 10kHz	RF Amplifier
2N6483	TO-71	5	5	-100	-50	-0.7	-4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
2N6484	TO-71	10	10	-100	-50	-0.7	-4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
2N6485	TO-71	15	25	-100	-50	-0.7	-4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
IT500	TO-52	5	5	-5	-50	-0.7	-4.0	0.7/1.6	6 @ 200μA	0.7	7.0	35 @ 10Hz	Cascode RF A
IT501	TO-52	5	10	-5	-50	-0.7	-4.0		6 @ 200μA	0.7	7.0	35 @ 10Hz	Cascode RF A
IT502	TO-52	10	20	-5	-50	-0.7	-4.0		6 @ 200μA	0.7	7.0	35 @ 10Hz	Cascode RF A
IT503	TO-52	15	40	-5	-50	-0.7	-4.0		6 @ 200μA	0.7	7.0	35 @ 10Hz	Cascode RF A
IT504	TO-52	25	100	-5	-25	-0.7	-4.0		6 @ 200μA	0.7	7.0	35 @ 10Hz	Cascode RF A
IT505	TO-52	50	200	-5	-25	-0.7	-4.0		6 @ 200μA		7.0	35 @ 10Hz	Cascode RF Ar

<sup>\*@</sup>IDSS



## Differential Amplifiers — continued Dual Monolithic N-Channel Junction FETs

PART NUMBER	PACKAGE	V <sub>GS1-2</sub> mV Max	ΔV <sub>GS</sub> μV/°C Max	I <sub>G</sub> pA Max	BV <sub>GSS</sub> V Min	V <sub>P</sub> V Min	Max	gfs mmho* Min Max	I <sub>DSS</sub> mA Min	Max	e <sub>n</sub> nVI√Hz Vm Max	COMMENTS
IT550	TO-71	50	100	na disebel	-40	-05	-3.0	7.5/12.5 @ 2mA	5.0	30.0	50 @ 10Hz	Cascode RF Amp
IT5911	TO-71	10	20	-100	-25	-1.0	-5.0	5/10 @ 5mA	7.0	40.0	20 @ 10kHz	RF Amplifier
IT5912	TO-71	15	40	-100	-25	-1.0	-5.0	5/10 @ 5mA	7.0	40.0	20 @ 10kHz	RF Amplifier
ITC5911	TO-99	10	20	-100	-25	-1.0	-5.0	5/10 @ 5mA	7.0	40.0	20 @ 10kHz	RF Amplifier
ITC5912	TO-99	15	40	-100	-25	-1.0	-5.0	5/10 @ 5mA	7.0	40.0	20 @ 10kHz	RF Amplifier
U231	TO-71	5	10	-50	-50	-0.5	-4.5	1 5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U232	TO-71	10	25	-50	-50	-0.5	-4.5	1 5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U233	TO-71	15	50	-50	-50	-0.5	-4.5	1 5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U234	TO-71	20	75	-50	-50	-0.5	-4.5	1 5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U235	TO-71	25	100	-50	-50	-0.5	-4.5	1 5	0.5	5.0	80 @ 100Hz	GP Diff Amp
U257	TO-78	100			-25	-1.0	-5.0	4.5 10	5.0	40.0	30 @ 10kHz	Low Cost
U426	TO-78	25	40	-0.5	-40	-0.4	-3.0	0.3 1.5	.06	1.8	70 @ 10Hz	Low Cost
U440	TO-71	10			-25	-1.0	-6.0	4.5/9 @ 5 µA	6	30		High Gain
U441	TO-71	20			-25	-1.0	-6.0	4.5/9 @ 5 μA	6	30		High Gain
	Ten War	0	APRIL 6	COST CO	THESE	THE PARTY	OF EAST FOR		1350		<b>第二十二十五年</b>	FOPTE .

#### **Dual Monolithic P-Channel MOSFETs (Enhancement)**

PART NUMBER	PACKAGE	V <sub>GS(TH</sub> V Min	)Amot g	BV <sub>DDS</sub> V Min/Max	IDSS pA Max	I <sub>GSS</sub> pA Max	9fs μmho Min	I <sub>D(ON)</sub> mA Min	Max	rds(ON) Ω Max	V <sub>GS 1-2</sub> mV Max	COMMENTS
3N165	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	100	Low Leakage
3N166	TO-99	2-2	-5	025 -40	-200	.0 -10	1500	-5.0	-30	300		Low Leakage
3N188	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	100	Diode Protected
3N189	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300		Diode Protected
3N190	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	100	High Input Z
3N191	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300		High Input Z

<sup>\*@</sup>IDSS

	PART NUMBER	PACKAG	V <sub>BE 1-2</sub> mV E Max	ΔV <sub>BE</sub> μVI°C Max	h <sub>FE</sub> (Note 1	I <sub>B1-2</sub> (Note 1) I) nA Max	BV <sub>CEO</sub> V	I <sub>CBO</sub> nA Max	NF dB Max	f <sub>t</sub> MHz @ I <sub>C</sub> Min	C <sub>obo</sub> pF Max	прахода сомм	
1000	2N2453	TO-78	3	10	80		30	5	7 typ.		10	Audio Amp	FFORTS
	2N2453A	TO-78	3	5	80		60	5	4 typ.			Audio Amp	
	2N2920	TO-78	3	10	150		60	2	3 typ.	60 @ 0.5mA	6	High Gain,	Low Noise
	2N2920A	TO-78	1.5	0.015	0.150		60	2	3 typ.	60 @ 0.5mA	6	High Gain,	Low Noise
	2N4044	TO-78	3	0.013	200	Ama 5 ona	60	0.1	2	200 @ 1mA	0.8	Low Capaci	tance
	2N4045	TO-78	5	10	80	25	45	0.1	3	150 @ 1mA	0.8	Low Capaci	tance
	2N4100	TO-78	5	0.00	150	10	55	0.1	3	150 @ 1mA	0.8	Low Capaci	tance
	2N4878	TO-71	1 10 083	3	200	5	60	0.1	2 typ.	200 @ 1mA	0.8	Low Capaci	tance
	2N4879	TO-71	5	0.85	150	10	55	0.1	3 typ.	150 @ 1mA	0.8	Low Capaci	tance
	2N4880	TO-71	085	0.010	80	25	45	0.1	3 typ.	150 @ 1mA	0.8	Low Capaci	tance
	IT120	TO-78	002	0.045	200	or 5 an	45	1.0	2 typ.	150 @ 1mA	2	Low Cost, L	ow Vos
	dw Cost	TO-71											
	IT120A	TO-78	1	00.3	200	A. 2.5	4500-	1.0	2 typ.	150 @ 1mA	02	Low Cost, L	ow Vos
		TO-71											
	IT121	TO-78	3	10	80	25	45	1.0	2 typ.	180 @ 1mA	2	Low Cost	
		TO-71											
	IT122	TO-78	5	20	80	25	45	1.0	2 typ.	180 @ 1mA	2	Low Cost	
		TO-71											
	IT124	TO-78	5	15	1500	0.6A	2 110	0.1	5/1/3	100 @ 100μΑ	0.8	Super $\beta$ for	
												Log Amps	
	IT126	TO-78	Fas is	140/3	150	(MO)(02.5 all	60	0.1	1 typ.	250 @ 10mA	3	Low Vos	
		TO-71				railet raile					othe		
	IT127	TO-78	2		150	5	60	0.1	1 typ.	250 @ 10mA	3	Low Vos	
	kage		100	006	00	0.3- 003					3-	98-OT	
	IT128		3	10	100	10 100	55	0.1	1 typ.	250 @ 10mA	3	Low Vos	
	befosto	TO-71	001	300	88-	0.8- 0.00	000	- : .00	S- ON	8-0-1	9-	. 98-07	
	IT129	TO-78	10	20	70	0 3 - 20 003	45 000	0.1	1 typ.	250 @ 10mA	3	Low Vos	
_		TO-71	-	-	1		744	Shirt					
	LM114	TO-71	2.0	10	250	10		0.050				Low Vos	
	LM114A	TO-71	0.5	2	500	2	45	0.010				Low Vos	
	LM114AH	TO-78	0.5	2	500	2	45	0.010				Low Vos	
	LM114B	TO-71	1.0	5	250	10	45	0.050				Low Vos	
	LM114BH	TO-78	1.0	5	250	10	45	0.050				Low Vos	
	LM114H	TO-78	2.0	10	250	10	45	0.050				Low Vos	

NOTE:

1.  $I_C = 10\mu A$ 

#### **Dual PNP Bipolar Transistors**

PART NUMBER	PACKAGE	V <sub>BE 1:2</sub> mV Max	ΔV <sub>BE</sub> μV/°C Max	h <sub>FE</sub> (Note 1) Min	I <sub>B1-2</sub> (Note 1) nA Max	BV <sub>CEO</sub> V Min	ICBO nA Max	NF dB Max	ft C <sub>obo</sub> MHz @ I <sub>C</sub> pF Min Max CO	MMENTS
2N3810	TO-78	3	10	100	(xell An)	-60	10	3 typ.	100 @ 1mA 4 Lov	v V <sub>OS</sub>
2N3810A	TO-78	1.5	5	100		-60	10	3 typ.	100 @ 1mA 4 Lov	v Vos ramad
2N3811	TO-78	0003	10	225		-60	10	3 typ.	100 @ 1mA 4 Lov	v Vos
2N3811A	TO-78	1.5	5	225	10	-60	10	3 typ.	100 @ 1mA 4 Lov	v Vos
2N5117	TO-78	3	3	100	10	-45	0.1	4 typ.		v Vos
2N5118	TO-78	00.5	5	100	15	-45	0.1	4 typ.	100 @ 0.5mA 0.8 Lov	v Cost
2N5119	TO-78	0005	10 0	50	40	-45	0.1	4 typ.	100 @ 0.5mA 0.8 Lov	v Cost
IT130	TO-78 TO-71	2	5	200	5	-45	1.0	2 typ.		v Vos
IT130A	TO 70	007		200	2.5	-45	1.0	2 typ.	150 @ 1mA 2 Lov	v V <sub>OS</sub>
IT131		3	10	80	25	-45	1.0	2 typ.	150 @ 1mA 2 Lov	v Cost
IT132	TO-78	5	20	80	25	-45	1.0	2 typ.	150 @ 1mA 2 Lov	v Cost
IT136		009	3	150	2.5	-60	0.1	2 typ.	250 @ 10mA 4 Lov	v Vos
IT137	TO-78	002		150	5	-60	0.1	2 typ.	250 @ 10mA 4 Lov	v Vos
IT138		3	10	100	10	-55	0.1	2 typ.	250 @ 10mA 4 Lov	v Vos
IT139 of all		250	20	70	20	-45	0.1	2 typ.	250 @ 10mA 4 Lov	v V <sub>OS</sub>
At+ of 8		75-		XII	60.0	De l		SONNO	might spread row power, fow teakage	GA-GAT CITT
57 + Of 91 e:										
$_{\rm C}$ = 10 $\mu$ A, V <sub>CE</sub>	=5V								TTL level translator/low charge injection awards	VF0S0FII H401/A

#### 3. ANALOG SWITCH & MULTIPLEXERS



#### **General Purpose Analog Switch Selector Guide**

			SWITCH	PARAMETER	RS .		
SWITCH	SPECIAL FEATURES	SWITCH	R <sub>DS(ON)</sub> (ΩMax)	I <sub>D(OFF)</sub> (nA Max)	ton (ns Max)	toff (ns Max)	ANALOG VOLTAGE RANGE (VSUPPLY = ± 15V)
DG118-125	Inverting/non-inver-	PMOS	600	4 4	300	1000 1000	ACOT ADDRESS TO STORY
DG126-54 DG139-164	SPST/DPST SPDT/DPDT switch capability, low RDS(ON) TTL compatible	N-JFET	10 15 30 50 80	10 10 11 1	1000 1000 600 600 600	2500 2500 1600 1600	ATRIBUTE TO
DG180-191	Mature, industry- standard switch, low R <sub>DS(ON)</sub>	NJFET	10 30 75	10 1 1	300 150 250	250 130 130	-7.5 to +15 -7.5 to +15 -10 to +15
DGM181-191	Monolithic replace- ment for DG180 family	CMOS	50 75	2.0 0.5	250 450	200 250	- 15 to + 15 - 15 to + 15
DG200/201 IH5200/5201	Industry-standard low cost	CMOS	70/80 70/80	2.0 0.05	08 1000 700	500 250	-15 to +15 -15 to +15
DG211 * DG212 *	Low leakage, inverting logic inputs	CMOS	175	5.0	68 1000 S	500	-15 to +15
IH5025-38	Low cost, low leakage. O.C. TTL compatible	P-JFET	100 150 100 150	0.5 0.5 0.5 0.5	200 200 200 200 200 200	200 200 200 200	0 to +20 0 to +20 0 to +20 0 to +20
IH5040-53	Low quiescent current Low R <sub>DS(ON)</sub>	CMOS	35 75	1.0 1.0	250 500	150 250	-15 to +15 -15 to +15
IH5140-45	High speed, low power, low leakage	CMOS	50	0.05	100- 200	75- 125	-15 to +14
IH5148-51 *	Low R <sub>DS(ON)</sub> , high speed, low power	CMOS	25	0.05	250- 500	200- 250	-14 to +14
IH6201/ IH401/A	TTL level translator/low charge injection switch	NJFET	30-50	0.05	456		AS=207 V/51 = 0)

<sup>\*</sup>New Product

#### 3. ANALOG SWITCH & MULTIPLEXERS



#### General Purpose Analog Switch Selector Guide. (Continued)

	UBINUUU NO					TCH CONFIG	URATION				
SPST	DUAL SPST		TRIPLE	QUAD	FIVE SPST	SPDT	DUAL SPDT	DPST	DUAL	DPDT	4PST
4   IH5010	BENT STORM	2508	HI HI	DG118	DG123 DG125	800 B	9.0 S.0	100 134	artual P.	Deput switch	1145003424
* IH6362	DG141 DG151 DG133			01 4 61 61	- 0	DG146 DG161 DG144	0.4	175	DG140 DG153 DG129	DG145 DG163 DG139	INSAT/62*
	DG152 DG134					DG162 DG143			DG154 DG126	DG164 DG142	New Product
1	DG180 DG181 DG182					DG186 DG187 DG188	DG189 DG190 DG191		DG183 DG184 DG185	81	exelqitlu
	DGM182	SUIDI	Heriza			DGM187 DGM188	DGM190 DGM191		DGM184 DGM185		
- CHANNET	DG200 IH5200	at 1	CHANNE	DG201 IH5201	KO-S	PANGE RANGE	and a	61 (130)0	uoisa, s	DEATOR	WITCH APE
JATINE	636	13	JAITM	DG211 DG212	END	(Att T)		D Canada	Coulcie and		
IH5037 IH5038	IH5033 IH5034	1	H5029 H5030	IH5025 IH5026	E(14)	S÷ol čS – (flugni)	1000	0.1	502	stry standard vis. fauth action up to	
819811	IH5035 IH5036		H5031 H5032	IH5027 IH5028	đS	- 25 to +		0.11		Jugal N	
IH5040	IH5048 IH5041			IH5052 IH5053		IH5042	IH5051 IH5043	IH5044	IH5049 IH5045	IH5046	IH5047
IH5140	IH5141		16,018	1 60	13HL 51	IH5142	IH5143	IH5144	IH5145	ets, low leaked Record break	H6168 pho
	IH5148			1		IH5150	IH5151		IH5149	re make switch	
				IH401 IH401A							

				T SWING						
	NUMBE	RO HER				1000			INPLIT	COMSUM-
		MELS	(x dW V)	(xsW V)			(KBM Au)			
SEASONEUS IN	STATE TO STATE OF	FREE COLUMN 19-10	decise to proceed and	THE STREET, ST	omnicotionació		CONTRACTOR OF THE	METO TOTAL SUSTEM	parameter substitute	COMPANIES CONTRACTOR
0123										
										55

				DOTA NO	SHOO SIO	Thirds	ANALOG VOLTAGE	SWI	тсн со	NFIGURA	TION
SWITCH FAMILY	SPECIAL FEATURES JAMES	SWITCH TYPE	r <sub>DS(ON)</sub> (Ω Max)	I <sub>D(OFF)</sub> (nA Max)	ton	t <sub>OFF</sub> (ns Max)	RANGE (V <sub>SUPPLY</sub> = ±15V)	SPST	DUAL SPST	TRIPLE SPST	QUAD SPST
IH5009-24	Lowest cost; virtual ground switch	P-JFET	100 150 100 150	0.2 0.2 0.2 0.2	500 500 500 500	500 500 500 500	-0.2 to +0.2 -0.2 to +0.2 -0.2 to +0.2 -0.2 to +0.2	IH5022 IH5023	IH5017 IH5018 IH5019 IH5020	IH5015	IH5009 IH5010 IH5011 IH5012
IH5341/52*	Video Switch, off- isolation 60 dB (10 MHz)	CMOS	75	1.0	300	150	-15 to +15		IH5341	100	* IH5352

<sup>\*</sup> New Product

#### Multiplexers

OMITOLL	2			191	4623	ANALOG		CONFIC	GURATION	
SWITCH	SPECIAL FEATURES	r <sub>DS(ON)</sub> (Ω Max)	I <sub>D(OFF)</sub> (nA Max)	t <sub>ON</sub> (ns Max)	t <sub>OFF</sub> (ns Max)	VOLTAGE RANGE VSUPPLY = (±15V)	8-CHANNEL SINGLE- ENDED	4-CHANNEL DIFFER- ENTIAL	16-CHANNEL SINGLE- ENDED	8-CHANNEL DIFFER- ENITAL
IH5108	Industry standard pinouts, fault	900	1.0	1500	1000	-25 to +25 (Input)	IH5108	IH5208	HISOSA HISOSA	1H5038
	protection up to ±25V input, low leakage,	1000	1.0	1500	1000	- 25 to + 25 (Input)	750876 848028	HEDSHI HEDSS	*IH5116	*IH5216
	low input current			12	0880		1 SECOND		114504E	
TMO	Industrial standard	awani.	MADELTA	\$1	GENT	0-08FII	E205H		HEGIN	DECEMB
IH6108	pinouts, low leakage,	300	1.0	1500	1000	- 14 to + 14	IH6108	IH6208	TETERI	195146
	low R <sub>DS(ON)</sub> break before make switching	600	1.0	1500	1000	- 14 to + 14			IH6116	IH6216

#### **Drivers for JFET Switches**

		OUTPU	TSWING		The latest the same			LOGIC	POWER
TYPE	NUMBER OF CHANNELS	POSITIVE (V Max)	NEGATIVE (V Max)	ton (ns Max)	toff (ns Max)	I <sub>INL</sub> (μΑ Max)	INH (μΑ Max)	INPUT LEVEL	CONSUM- (mW)
D123	6	V <sub>SUPPLY</sub>	- 19.7	250	400-800	1.0	1.0	TTL/DTL	20
D125	6	VSUPPLY	-19.7	250	400-800	700	1.0	TTL	50
D129	4	VSUPPLY	-19.3	250	1000	200	0.25	TTL/DTL	55
IH6201	2	+14.0	-14.0	200	300	1.0	1.0	TTL	350

	TYPE	DESCRIPTION	l <sub>QUIESCENT</sub> (Per Channel) (μΑ Typ)	V <sub>SUPPLY</sub> (V Max)	V <sub>OS</sub> (mV Max)	IBIAS (nA Max)	GBW (MHz)	COMPEN- SATION	TEMPERATURE RANGE (°C)
SINGLES	ICL7611 ICL7612 ICL7613 ICL8021M ICL8021C	CMOS, Selectable I <sub>Q</sub> CMOS, Extended CMVR CMOS, Input Protected Bipolar, Selectable I <sub>Q</sub> Bipolar, Selectable I <sub>Q</sub>	10 10 10 30 30	±9 ±9 ±9 ±18 ±18	2, 5, 15 2, 5, 15 2, 5, 15 3 6	0.05 0.05 0.05 20 30	0.044 0.044 0.044 0.27 0.27	INT INT INT INT	0 to +70 -55 to +125 -55 to +125 0 to +70
DUALS	ICL8022M ICL8022C	Dual 8021M Dual 8021C	30 30	±18 ±18	3 6	20	0.27 0.27	eggint, 2016 Int Blds	-55 to +125
TRIPLES	ICL7631 ICL7632 ICL8023M ICL8023C	CMOS, Selectable I <sub>Q</sub> CMOS, Selectable I <sub>Q</sub> Triple 8021M Triple 8021C	10 10 30 30 30	±9 ±9 ±18 ±18	5, 10, 20 5, 10, 20 3 6	0.05 0.05 20 30	0.044 0.044 0.27 0.27	INT NONE INT INT	0 to <sub>8</sub> +70 -55 to +125 -55 to +125 0 to +70
QUADS	ICL7642	CMOS, Fixed IQ	10 0000	±9	5, 10, 20	0.05	0.044	Ipolar, Super-	0 to +70 -55 to +125

#### **Operational Amplifiers: General Purpose**

anu	TARETYPE BOMAR	DESCRIPTION	Vos (mV Max)	I <sub>BIAS</sub> (pA Max)	SLEW RATE (VIµs)	GBW (MHz)	COMPEN- SATION	V <sub>SUPPLY</sub> (V Max)	TEMPERATURE RANGE (°C)
SINGLES	LM108 LM308 ICL7611 ICL8007M ICL8007C	Bipolar, Super-Beta Bipolar, Super-Beta CMOS, Selectable I <sub>Q</sub> JFET Input Op-Amp JFET Input Op-Amp	2.0 7.5 2, 5, 15 20 50	2000 7000 50 20 50	1.6 6 6	1.0 1.0 1.4 1.0 1.0	EXT EXT INT INT	±20 ±18 ±9 ±18 ±18	-55 to +125 0 to +70 0 to +70 -55 to +125 -55 to +125 0 to +70
DUALS	LH2108 LH2308 ICL7621 ICL8043M ICL8043C	Bipolar, Super-Beta Bipolar, Super-Beta CMOS, Fixed IQ JFET Input Op-Amp JFET Input Op-Amp	2.0 7.5 2, 5, 15 20 50	2000 7000 50 20 50	0.16 6 6	1.0 1.0 0.48	EXT EXT INT INT	±20 ±18 ±9 ±18 ±18	-55 to +125 0 to +70 0 to +70 -55 to +125 -55 to +125 0 to +70
TRIPLES	ICL7631	CMOS, Selectable IQ	5, 10, 20	50	1.6	1.4	INT INT CONTROL PART PART PART PART PART PART PART PART	20149 2016	{ 0 to +70 -55 to +125
QUADS	ICL7641	CMOS, Fixed IQ	5, 10, 20	50	1.6	1.4	QMAINT MG	±9	{ 0 to +70 -55 to +125

# Operational Amplifiers: High Output Current

	orde- (	67 INI	140.0	05,01 A	3.0	08.1	Fixed to	SOMO	TEMPRATURE
	TYPE	DESCRIPTION	lout (A Min)	V <sub>OUT</sub> (V Min)	V <sub>SUPPLY</sub> (V Max)	V <sub>OS</sub> (mV Max)	IBIAS (nA Max)	Avol. (dB Typ)	RANGE (°C)
	ICH8510M	Hybrid Amplifier	1.0	±26	±32	3.0	250	100	-55 to +125
	ICH8510I	Hybrid Amplifier	1.0	±26	±32	6.0	250	100	-25 to +85
ES	ICH8515M	Hybrid Amplifier	1.5	±12	±18	3.0	250	100	-55 to +125
Jg.	ICH8515I	Hybrid Amplifier	1.25	±12	±18	6.0	50	100	-25 to +85
SINGLES	ICH8520M	Hybrid Amplifier	2.0	±26	±32	3.0	250	100	-55 to +125
٠,	ICH8502I	Hybrid Amplifier	2.0	±26	±32	6.0	500	100	-25 to +85
	ICH8530M	Hybrid Amplifier	2.7	±25	±32	3.0	250	100	-55 to +125
	ICH8530I	Hybrid Amplifier	2.7	±25	±32	6.0	500	100	-25 to +85



Operational Ampliflers: General Purpose

# Operational Amplifiers: Low/Ultra-low Input Offset Voltage

23	TYPE O to + 270	DESCRIPTION	(u)	Vos / Max	300	ΔVos/ΔT (μV/°C) (Max)	ΔVos/Δt (nV/month) (Typ)	I <sub>BIAS</sub> (pA Ma		GBW (MHz)	V <sub>SUPPLY</sub> (V Max)	TEMPERATURE RANGE (°C)
SINGLES	ICL7650C ICL7650I ICL7650M ICL7652C ICL7652I	CMOS, Chopper- stabilized CMOS, Chopper- stabilized Low-noise 7650C Low-noise 7650I	0 0	±5 ±5 ±5 ±5	0 20 20 0	±0.05 ±0.05 ±0.05 ±0.05 ±0.05	100 874 100 874 100 84 100 84 100 84	10 10 10 30 30	30 30 10 10	2.0 2.0 2.0 2.0	±9 ±9 ±9 ±9	0 to +70 -25 to +85 -55 to +125 0 to +70 -25 to +85
	LM108A LM308A	Bipolar, Super-Beta Bipolar, Super-Beta	0	500 500	20	5.0 5.0	87 ±	2000 7000	30	1.0	±20 15 ±18	-55 to +125 0 to +70
DUALS	LH2108A LH2308A	Bipolar, Super-Beta Bipolar, Super-Beta		500		5.0	<u>                                     </u>	7000		1.0	±20 ±20	-55 to +125 0 to +70

#### Operational Amplifiers: Low Input Bias Current

	TYPE	And the second	RIPTION	IBIAS (pA Max	los (pA Typ)	V <sub>OS</sub> (mV Max	GBW (MHz)	COMPEN- SATION	V <sub>SUPPLY</sub> (V Max)	TEMPERATURE RANGE (°C)
SINGLES	ICL7611 ICL7612 ICL7613 ICL7614 ICL7615 ICL8007M ICL8007AM ICL8007C ICL8007AC ICH8500 ICH8500A	CMOS, CMOS, CMOS, CMOS, JFET II JFET II JFET II	Selectable IQ Extended CM Input Protecte Fixed IQ Input Protecte Input Op-Amp Input, Low Bias Input Low Bias Input, Low Bias Input, Low Bias	50 50 50 50 4.0 50 4.0 0.1	0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.2 0.5	2, 5, 15 2, 5, 15 2, 5, 15 2, 5, 15 2, 5, 15 2, 5, 15 20 30 50 30 50 50	1.4 1.4 1.4 0.48 0.48 1.0 1.0 1.0 1.0 7 0.7	INT INT EXT EXT INT INT INT INT INT INT INT	±9 ±9 ±9 ±9 ±9 ±18 ±18 ±18 ±18 ±18	0 to +70 -55 to +125 -55 to +125 -55 to +125 0 to +70 0 to +70 -25 to +85 -25 to +85
DUALS	ICL7621 ICL7622 ICL8043M ICL8043C	CMOS, JFET II	Fixed I <sub>Q</sub> Offset Null Pinput Op-Amp	50 50 20 50	0.5 0.5 0.5 0.5	2, 5, 15 2, 5, 15 20 50	0.48 0.48 1.0 1.0	TAI TAI TAI TAI TAI	±9 ±9 ±18 ±18	0 to +70 -55 to +125 -55 to +125 0 to +70
TRIPLES	ICL7631 ICL7632		Selectable IQ Selectable IQ	50 50	0.5	5, 10, 20 5, 10, 20	1.4	INT NONE	±9 ±9	0 to +70 -55 to +125
QUADS	ICL7641 ICL7642	Control of the public belongs before the	Fixed I <sub>Q</sub>	50 50	0.5 0.5	5, 10, 20 5, 10, 20	1.4	INT INT	±9 ±9	0 to +70 -55 to +125
	EDWAR (P")	30yA (q(7 0ti)	anigt (xsNt Ani)	eo <sup>V</sup> (miv friant)	Vaggers, v (V Max)	(A MIN)	TUO! (alld A)	SCRIPTION		3917
	7+ of 88-4 + of 88-4		250 250 250 350 250 250 500	0.8 0.8 0.8 0.8 0.8 0.0 0.0 0.0	SE±	#25 #25 #12 #12 #25 #26 #25 #25		Ampilliar Ampilliar Ampilliar Ampilliar Ampilliar Ampilliar Ampilliar Ampilliar		



Power Supply Circuits (CMOS)

#### Commutating Auto-Zero (CAZ) Instrumentation Amplifiers

(0°) BIOMAR <b>TYPE</b> 0 to + 0  -56 to + 02	DESCRIPTION  VOI - of Val - to separate	V <sub>OS</sub> (μV Max)	ΔVos/ΔT (μV/°C) (Max)	△Vos/△t (nV/month) (Typ)	I <sub>BIAS</sub> (pA Max)	SIGNAL BANDWIDTH (Hz Max)	A <sub>VOL</sub> (dB Typ)	TEMPERATURE RANGE (°C)
ICL7605C ICL7605I ICL7605M	CMOS, Compensated CMOS, Compensated CMOS, Compensated	5.0 5.0 5.0	0.2 0.2 0.2	40 40 40	1500 1500 1500	10 30 30 T	105 105 105	-25 to +85 -55 to +125
ICL7606C ICL7606I ICL7606M	CMOS, Uncompensated CMOS, Uncompensated CMOS, Uncompensated	5.0 5.0 5.0	0.2 0.2 0.2	40 40 40	1500 1500 1500	10 10	105 105 105	0 to +70 -25 to +85 -55 to +125

#### **Log/Antilog Amplifiers**

ТҮРЕ	DESCRIPTION	ABSOLUTE ERROR (mV Max)	V <sub>OS</sub> (mV Max)	ΔVout/ΔT (mV/°C) (Typ)	DYNAMIC RANGE (dB)	OUTPUT SWING (V Typ)	V <sub>SUPPLY</sub> (V Max)	TEMPERATUR RANGE (°C)
ICL8048BC	Logarithmic Amplifier,	30	25	0.8	120	±14	±18	0 to +70
ICL8048CC	1V/Decade Output	60	50	0.8	120	±14	±18	0 to +70
ICL8049BC	Antilog Amplifier 1V/Decade Input	10	25	0.38	60	±14	±18	0 to +70
ICL8049CC		25	50	0.55	60	±14	±18	0 to +70
851 + 01 d3-	V812 0 V812 8 V812 8 V812 8	or or a	0000		0.01± 1 0.01± 1 0.01±		Hold Input.	195112 195113 195114

#### **Power Transistor Drive Amplifiers**

TYPE	DESCRIPTION	lout (mA Min)	V <sub>OUT</sub> (V Min)	V <sub>OS</sub> (mV Max)	Avol (V/V)	SUPPLY CURRENT (mA Max)	V <sub>SUPPLY</sub> (V Max)	TEMPERATURE RANGE (°C)
ICL8063M	Bipolar Monolithic	+50/-25	±27V	50	6	6	±35	-55 to +125
ICL8063C	Driver Amplifier	+40/-20	±27V	75	6	7	±35	0 to +70

#### **Video Amplifiers**

TYPE	DESCRIPTION	A <sub>V</sub> (V/V)	SIGNAL BANDWIDTH (MHz)	V <sub>oo</sub> (V Max)	I <sub>BIAS</sub> (μA Max)	ē <sub>n</sub> (μV RMS)	V <sub>SUPPLY</sub> (V Max)	TEMPERATURE RANGE (°C)
NE592	Bipolar, Programmable	100/400	90/40	0.75	30	12	±8	0 to +70
SE592	gain amplifier	100/400	90/40	0.75	20	12	±8	-55 to +125

#### **Power Supply Circuits (CMOS)**

TYPE	FUNCTION	DESCRIPTION FALSOVA TALGOVA	TEMPERATURE RANGE (°C)
ICL7660	Voltage Converter	The ICL7660 performs supply voltage conversion from positive to negative. Input range is $+1.5V$ to $+10V$ resulting in complementary output voltages of $-1.5V$ to $-10V$ .	0 to +70 -55 to +125
ICL7662*	Voltage Converter	This device is similar to the ICL7660 in its operation, except the input voltage range extends from +4.5V to +20.0V.	0 to +70 -55 to +125
ICL7663	Positive Voltage Regulator	The ICL7663 is a low-power, high-efficiency device ( $I_Q = 4\mu$ A max) that accepts an input of 1 to 10V, and provides an adjustable output of 1 to 10V at up to 40mA load.	0 to +70
ICL7664	Negative Voltage Regulator	The ICL7664 is similar in operation to the ICL7663, except that it accepts an input of $-1$ to $-10V$ and provides an adjustable output of $-1$ to $-10V$ at up to $-40\text{mA}$ load.	0 to +70
ICL7673*	Automatic Battery- Backup Switch	The ICL7673 automatically switches between a main power supply (eg. +5V) and a battery backup supply, when the main supply is removed. Load current is 0 to 38mA.	0 to +70 -25 to +85

Commutating Auto-Zero (CAZ) Instrumentation Ampliflers

<sup>\*</sup>New Product

Sample	and	Hold	Circuits

TYPE	DESCRIPTION	V <sub>INPUT</sub> (V Max)	ACQUISITION TIME (µ8)	CHARGE INJECTION ERROR (mV)	V <sub>OS</sub> (mV)	DRIFT RATE (mV/sec)	V <sub>SUPPLY</sub> (V Max)	TEMPERATURE RANGE (°C)
IH5110	General purpose	±7.5	6	5	40	5	±16V	Yoursens tou
IH5111	Sample/Hold Circuit,	±10.5	6	5	40	5	±16V	-25 to +85
H5112	TTL Compatible	±7.5	6	5	10	5	±16V	8
IH5113	Hold Input	±10.0	6	5	10	5	±16V	-55 to +125
IH5114		±7.5	6	5	5	5	±16V	THE STATE OF LOTE
H5115		±10.0	6	5	5	5	±16V	/

TARBOVA

	YJARUS THERRUD (xsat Ace)			DESCRIPTION	эчүт
				Bipolar Monolithic Chiver Applifiler	

					TYPE DESCRIPTION
	ficefil V)				
	AND RESIDENCE OF THE PARTY OF T	STATE STATE STATE			SE SENSO DE DESCRIPCIO DE COMPOSITION DE SENSO DE COMPOSITION DE C
					NESSE Blooter, Programmable
		27	0.76		SESS2 gain amplifier

TYPE	DESCRIPTION	ACCURACY (°C)	V <sub>SUPPLY</sub> (V)	TEMPERATURE RANGE (°C)
AD5901	The AD590 is a 2-wire,	±10	4 to 30	-55 to +150
AD590J	current-output	±5.0	4 to 30	-55 to +150
AD590K	temperature transducer.	±2.5	4 to 30	-55 to +150
AD590L	Output current	±1.0	4 to 30	-55 to +150
AD590M	varies linearly at 1µA/°K.	±0.5	4 to 30	-55 to +150

### Voltage References and Detectors

TYPE	FUNCTION OF	Var thus 7 to 100 ft transcript VED+ or 0 to 10 to 100 the though blot value value to 100 to	TEMPERATURE RANGE (°C)
ICL7665	Programmable Micropower Voltage Detector	Contains two individually programmable voltage comparators, and requires only $3\mu A$ supply current. Intended for battery operated systems that require low or high voltage warnings etc. Open drain outputs for interfacing.	0 to +70
ICL8069	Low Voltage Reference	A 1.20V temperature compensated bandgap voltage reference. It achieves excellent stability and low noise at currents as low as 50µA.	0 to +70 -55 to +125
ICL8211	Programmable Voitage Detector	The ICL8211 is a micropower voltage detector. It contains a 1.15V reference, a comparator, a hysteresis output and a non-inverting main-output.	0 to +70 -55 to +125
ICL8212	Programmable Voltage Detector	The ICL8212 is similar in operation to the ICL8211 except that its main output is inverting as opposed to non-inverting.	0 to +70 -55 to +125

#### Miscellaneous Circuits

TYPE	FUNCTION	DESCRIPTION	TEMPERATURE RANGE (°C)
ICM7206	CMOS Touch Tone* Encoder	The ICM7206 is a 2-of-8 sine wave DTMF generator for use in telephone dialing systems. Requires a 3.58 MHz crystal & will work with 3 x 4 or 4 x 4 keypads.	-40 to +85
ICL7667	Dual Power MOSFET Driver	The ICL7667 is a TTL-compatible high-speed CMOS driver designed to provide high output current (1.5A) and voltage (up to +15V) for driving the gates of power MOSFETs.	0 to +70 -55 to +125
ICL8013	4-Quadrant Analog Multiplier	The ICL8013 is a bipolar 4-quadrant multiplier. The output is proportional to the product of two input voltages. An internal op-amp is included for level shifting.	0 to +70 -55 to +125
ICL8038	Precision Waveform Generator	The ICL8038 is a bipolar function generator and is capable of producing high accuracy sine, square and triangular waveforms. Frequency range is 0.001 Hz to 300 kHz.	0 to +70 -55 to +125

<sup>\*</sup>New Product



#### Integrating Analog-to-Digital Converters with Display Drivers (CMOS)

	TYPE	ACCURACY SPECIAL FEATURES	DISPLAY	CONVER- SIONS/SEC	INPUT VOLTAGE RANGES	NON LIN- EARITY	ROLLOVER ERROR	STABILITY ZERO INPUT DRIFT	SUPPLY VSUPPLY ISUPPLY	TEMP RANGE (°C)
	ICL7106	Low Cost	LCD, 7-0-1-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 1.8 mA (Max)	0 to +70
	ICL7107	Low Cost	LED, 7- Segment Common Anode	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 1.8 mA (Max)	0 to +70
	ICL7116	Display Hold Input	LCD, 7- Segment Direct Drive	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 1.8 mA (Max)	0 to +70
3-1/2 DIGIT	ICL7117	Display Hold Input	LED, 7- Segment Common Anode	0.1 to 15	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	8 41μV/°C	±5V (Typ) 1.8 mA (Max	0 to +70
	ICL7126	Low Power Operation	LCD, 7- Segment Direct Drive	0.1 to 4	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	og r A nd 1μV/°C	+9V (Typ) 100 µA (Max)	0 to +70
	ICL7136	Improved '7126, Low Power Operation	LCD 7- Segment Direct Drive	0.1 to 4	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	+9V (Typ) 100 μA (Max)	0 to +70
	ICL7137	Improved '7107, Low Power Operation	LED 7- Segment Common Anode	0.1 to 4	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 200 μA max	0 to +70
4 1/2 DIGIT	ICL7129	Range, Display- Hold & Decimal Point Inputs	LCD, 7- Segment Triplexed	2	0 to ±0.2V 0 to +2.0V	±1 Count	0.5 Count (typ)	±0.5μV/°C (typ)	+9V (Typ) 1.4 mA (Max)	0 to +70

		HOFFEIDERIG	
	CMOS Touch Tone* Engage	The IGM7205 is a 2 ol-8 aine wave DTMF generator folloss in telephone dialing systems. Requires a 3.58 MHz orystet & with 9 x \$ or \$ x \$ reypads.	
		The ICL7887 is a TYL compatible high-speed CMDS driver designed to provide high output current (1,5A) and voltage (up to +15V) for driving the gates of power MOSFETs.	0 to +70 +55 to +125
ICLBOTS		The ICLIBOTS is a bipolar a quadrant invitibilier. The output is proportional to the product of two input walkings. An Internal opening is included for level shiftling.	6 to +70 -55 to +125
	Precision Waveform	The ICLB038 is a bipolar function generator and is capable of producing high accuracy also, square and triangular waveforms. Frequency range is 0.001 Hz to 300 kHz.	0 to +20 -65 to +128

#### 6. DATA ACQUISITION



#### Integrating Analog-to-Digital Converters (CMOS)

	TYPE (P)	SPECIAL FEATURES	DIGITA OUTPU FORMA	T M	CONVER- SIONS PER SECOND	INPUT VOLTAGE RANGES	NON LINEARITY	ROLLOVER ERROR	STABILITY ZERO INPUT DRIFT	SUPPLY V <sub>SUPPLY</sub>	TEMP RANGE (°C)
4-1/2 DIGIT	ICL7135	Under & over range outputs, polarity output	Multiplexed BCD with strobes	(xas)	0.1 to 7.5 A	0 to ±0.2V 0 to ±2.0V	±1 Count	±1 Count	2μVI°C	±5V (Typ) 3.0 mA (Max)	0 to +70
	ICL7109	μP-Compatible, run/hold input, UART Handshake	8/4 Bits, Separate Enables	(av7	30 (Max)	0 to ±4.0V 0 to ±3.5V	±1 Count	±1 Count	1μV/°C	±5V (Typ) 1,5 mA (Max)	0 to +70 -25 to +85 -55 to +125
12-BIT	ICL7104-12 ICL8052	μP-Compatible, 2-Chip Set, Low Input Leakage	8/4 Bits, Separate Enables	top?	48.8 (Max)	±10V	+1 LSB	+1 LSB	5μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
	ICL7104-12 ICL8068	μP-Compatible, 2-Chip Set, Low Input Noise	8/4 Bits, Separate Enables	(XE58)	48.8 (Max)	±10V	+1/LSB	+1 LSB	5μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
BIT	ICL7104-14 ICL8052	μP-Compatible, 2-Chip Set, Low Input Leakage	8/4 Bits, Separate Enables	(gy7)	12.2 (Max)	±10V	+1 LSB	+1 LSB	2μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
14·E	ICL7104-14 ICL8068	μP-Compatible, 2-Chip Set, Low Input Noise	8/4 Bits, Separate Enables	(qyf)	12.2 (Max)	±10V	+1 LSB	+1 LSB	2μV/°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
BIT	ICL7104-16 ICL8052	μP-Compatible, 2-Chip Set, Low Input Leakage	8/8 Bits, Separate Enables	(suM	3 (Max)	±10V	+1 LSB	+1 LSB	2μVI°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70
16.6	ICL7104-16 ICL8068	μP-Compatible, 2-Chip Set, Low Input Noise	8/8 Bits, Separate Enables	(U) 0 (24) 6N	3 (Max)	± 10V	+1 LSB	+1 LSB	2μVI°C	+5V and ±15V (Typ) 1.0 mA (Max)	0 to +70

#### Successive Approximation Analog-to-Digital Converters (CMOS)

Paramoteria.	TYPE	SPECIAL FEATURES	DIGITAL OUTPUT FORMAT	CONVERSION SPEED (µs)	INPUT VOLTAGE RANGE	OVERALL ACCURACY	TOTAL	GAIN TEMP. COEFF.	SUPPLY V <sub>SUPPLY</sub> I <sub>SUPPLY</sub>	TEMP RANGE (°C)
	ADC0802	μP-Compatible, Differential Inputs	8-Bit Binary	114 (Max)	0 to +5.0V	-	± ½ LSB (Unadjusted)	Inamus no	+5V (Typ) 25 mA (Max)	0 to +70 -40 to +85 -55 to +125
8-BIT	ADC0803	μP-Compatible, Differential Inputs	8-Bit Binary	114 (Max)	0 to +5.0V	-	±1/2 LSB (Adjusted)	-	+5V (Typ) 25 mA (Max)	0 to +70 -40 to +85 -55 to +125
	ADC0804	μP-Compatible, Differential Inputs	8-Bit Binary	114 (Max)	0 to +5.0V	-	±1 LSB (Unadjusted)	1-	+5V (Typ) 25 mA (Max)	0 to +70 -40 to +85 -55 to +125
14-BIT	ICL7115- J/K	μP-Compatible, High Speed Converter	8/6 Bits A <sub>0</sub> Byte Enable	40 (Max)	0 to +5.0V 0 to -5.0V	0.01% (J) 0.006% (K)	+1 LSB	4 ppm/°C	+5V (Typ) 5 mA (Typ)	0 to +70

	TYPE	SPECIAL FEATURES	DIGITAL	SETTLING TIME (TO 0.05% FS)	OUTPUT VOLTAGE CURRENT	NON LIN- EARITY	GAIN ERROR	STABILITY GAIN LINERITY	SUPPLY VSUPPLY ISUPPLY	TEMP RANGE (°C)
8-BIT	AD7523	μP-Compatible, Low Power Multiplying DAC	Binary/ Offset Binary	200 ns (Max)	±V <sub>REF</sub> A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	1.5% (Max)	10 ppm/°C 2 ppm/°C	+15V (Typ) 100μA (Max)	0 to +70 -25 to +85 -55 to +125
	AD7520	μP-Compatible, 8, 9, 10 Bit Lin. Multiplying DAC	Binary/ Offset Binary	500 ns (Typ)	±V <sub>REF</sub> A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 -25 to +85 -55 to +125
10-BIT	AD7530	Same as '7520 But no leakage /feed thru specs	Binary/ Offset Binary	500 ns (Typ)	±V <sub>REF</sub> A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 -25 to +85 -55 to +125
	AD7533	μP-Compatible, Lowest Cost 10-bit DAC	Binary/ Offset Binary	600 ns (Typ)	±V <sub>REF</sub> A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	1.4% (Max)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 -25 to +85 -55 to +125
	AD7521	μP-Compatible, 8, 9, 10 Bit Lin. Multiplying DAC	Binary/ Offset Binary	500 ns (Typ)	±V <sub>REF</sub> A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 -25 to +85 -55 to +125
12-BIT	AD7531	Same as '7521 But no leakage /feed thru specs	Binary/ Offset Binary	500 ns (Typ)	±V <sub>REF</sub> A 10KΩ (Max)	0.2% (J,A,S) 0.1% (K,B,T) 0.05% (L,C,U)	0.3% (Typ)	10 ppm/°C 2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 -25 to +85 -55 to +125
	AD7541	μP-Compatible, High perform- ance DAC	Binary/ Offset Binary	1 μs (Max)	± V <sub>REF</sub> A 10KΩ (Max)	0.02% (J,A,S) 0.01% (K,B,T) 0.01% (L,C,U)	0.3% (Max)	2 ppm/°C	+15V (Typ) 2 mA (Max)	0 to +70 -25 to +85 -55 to +125
14-BIT	AD7134	μP-Compatible, Low power Multiplying DAC	Binary/ 2's Complement	3 μs (Max)	±V <sub>REF</sub> A 7KΩ (Max)	0.1% (J,A,S) 0.006% (K,B,T) 0.003% (L,C,U)	0.02% (J) 0.012% (K) 0.006% (L)	5 ppm/°C 1 ppm/°C	+5V (Typ) 0.5 mA (Max)	0 to +70 -25 to +85 -55 to +125

# Quad Current Switches For D/A Conversion (Singles or Matched Pairs)

TYPE	DESCRIPTION	ABSOLUTE ERROR (% Max)	DARBOTE	RROR MPCO. M°C Max)	V <sub>SUPPLY</sub> (V Max)	ISUPPLY (mA Max)	TEMPERATURE RANGE (°C)	
ICL8018A ICL8019A ICL8020A	High precision current switches for use in summing D/A converters	±0.01 ±0.10 ±1.00		±5 ±25 ±50	±20 ±25 ±20	10 ±20 10	0 to +70 -55 to +125	ADDOSG2
	- +5V (Typ) (2.5 mA(Nax)	BBJ et a: (Kedeushek)		W0.6+ of 0	) 114 (Valvi)	Bloop	precompacine, Differential Inputs	execced <sub>A</sub>
0 to +70 -40 to +85 -55 to +125	- 45V (Typ) 25mA@4ex						pP-Compatible, Ditterantial inputs	POSSOGA
	(cy7) V8+ (cy7) Am 8 (cy7)					Bit Bits A <sub>0</sub> Byte Enable	aP-Compatible, High Speed Converter	

#### **Timer/Counters With Display Drivers**

			D	ISPL	AY				2.4	Lean Inches			FU	NC	TIO	NS									SPECIAL STATUTES
		11100	LED		LCD	VF		COL			UN	UN	RS	AL	109	Kont	SHEE	TEST	1517)	255	(380)	2003	10426680	1000	SCHOOL CONTRACTOR MARKS
		Je, Non-MUX	ode, MUX	de, MUX	Ion-MUX	ius I sri ri k	Aug up	18 y	in tols	(Hr/Min/Sec)	en but	ri ri	Ratio S E	( ti	Outputs	10 to	ing & gai	10 10 10	Blanking	la si	Register	Zero Output	38 equi cutrer 86. Los a tong	Avails	CM7565 Low power the large su power power py to power the power for ponents for
OF DIGITS	TYPE	Common Anode,	Common Cathode, MUX	Common Anode, MUX	Direct Drive, Non-MUX	Non-MUX	Up/Down	Up only	Decade	Modulo 60 (H	Frequency	Period	Frequency R	Time Interval	MUX BCD Out	Display Latch	Display Blanking	Count Enable	Leading Zero	Preset Count	Comparison R	Equal and Zer	MAX COUNT SPEED (MHz)		TYPICAL APPLICATIONS AND COMMENTS
	ICM7217	mis	tore:		bagi	30		100	0	ex	=	190		Ol			•	16					2	-	Industrial control; preset/predetermin-
	ICM7217A								•						•	•	•		•	•			2		ing counters, sequencers, on/off delay timers, batch counters. Presets and
	ICM7217B						•			•					•		•		•	•		•	2		loads compare register from thumbwheel switches
0	ICM7217C									•					•	•	•					•	2		(numbwheer switches
DIGIT	ICM7227								•						•							•	2		Microprocessor compatible interface.
	ICM7227A												78			•	•						2	1-1-21	Industrial control: preset/predetermin- ing counters, sequencers, on/off delay
	ICM7227B							-		•			*****	-		•		F	•				2		timers, batch counters. Presets and loads compare register from a
	ICM7227C	12.5	•	rian.	cetat	2000				•	13	83			•				•	•			2	7,103	microprocessor
Section 1	ICM7224	2000	238	19311		1200		•	•	SIZ	=		olaja	23/0	阳也	•	7195	•		245	THE STATE OF THE S	155	15		
	ICM7224A			3.730		1 18	H			•	200					•	-				-	-	15	1	cascaded for more digits
0.4	ICM7225										=			19	-			•					15		Has brightness adjustment, 10 µA cur-
41/2 DIGIT	ICM7225A		1/2	CHAV	lesiu	9 6		•		•	15.	1									0	ir i	15	4.6	rent with display blanked, cascadable
	ICM7236		T	UH.	1001			•	•	All columns		4		10	.0						.0	100	15		Up to 30 V output drive for Vacuum
	ICM7236A		217	UEA	1,000			•	2	•	22	0.0		20	Ų	•					0		15	10	Fluorescent
5-1/2 DIGIT	ICM7249	129	100	0.00	•	1 8 19 200		•	•	SP)	300	8.0		•	8,1	0 0					0 0 0	100	0	20 100	Event timer/counter, hour meter. 14 programmable modes. Selectable input filtering
BIGIT	ICM7215	.81	•	nik	selu art 8 art 0	3.5		•	SHE SE		14 1 83 1 32 1	f. 4		•	AVA AVA AVA	000	•	•			0.0.0	11 151 151	3 8	4544	4 functions: start/stop/reset, split, taylor, time out. 1/100's seconds and low battery
7 DIGIT	ICM7208	350		1150	taelu oH)	1.1	1	•	•	ST.				9V	SUN SUN	•		•		0	010	1	2.5	100	Use with ICM7207/A for a 7-digit frequency counter
	ICM7216A		-					•	•		•	•	•	•	-								10		Universal frequency counter with
	ICM7216B								•		•		•										10		display drivers. 4 internal gate times
Di	ICM7216C							•	•		•				-			-					10	1	auto decimal point, leading zero blanking, overflow indication. Displa
BIGIT	ICM7216D							•			•									T			off, hold, and res	off, hold, and reset inputs.	
	ICM7226A							•	0		•	•						•					10		Same as ICM7216 plus period and
	ICM7226B							•	•														10		time interval averaging, BCD output µP PIA compatible.

<sup>■</sup> These counters will measure frequency when used with the ICM7207 (0.01 and 0.1 second timebase) or the ICM7207A (0.1 and 1.0 second timebase)

#### 7. TIMER/COUNTER CIRCUITS



#### **Timers/Counters Without Display Drivers**

TYPE	SPECIAL FEATURES	DESCRIPTION
ICM7555		Low power CMOS equivalent of industry standard 555 timer—only $80\mu$ A supply current. ICM7555 does not have the large supply current transients of the bipolar 555 and does not require the large bypassing capacitors needed by the 555. Low leakage threshold and trigger inputs allow use of higher impedance RC timing components for extra long time delays.
ICM7556		An ICM7556 is a dual ICM7555, a CMOS, low power equivalent of the Bipolar 556 Timer.
ICM7240 ICM7250 ICM7260	Binary 0-225 BCD 0-99 Time 0-59	Programmable CMOS counter/timer. Uses on-board RC oscillator or an external clock. The count is programmed by wire-AND connection of the outputs. Excellent for ON/OFF delay timers, + N counters, and long period delays.
ICM7242	Fixed 128/255	RC oscillator + 8-bit counter, similar to ICM7240 but with fixed 256 count. Used for extremely long time delays. Cascadable,

#### Oscillator/Divider Selector Guide

TYPE	OUTPUT	SUPPLY VOLTAGE (V)	TYPICAL CURRENT (µA)	PULSE WIDTH (ms)	CRYSTAL FREQUENCY	OTHER OUTPUTS/COMMENTS
ICM7213 221016	1 Pulse/Min	2-4	100	125, 1000	4.19 MHz	1 Pulse/Sec, 2048, 1024, 34.133, 16 Hz
ICM7207A	0.5 Hz	4-5.5	260	1000, 0.391	5.24288 MHz	5 Hz, 1600 Hz (Note 1)
ICM7213	1 Hz	2-4	100	7.8	4.19 MHz	1 Pulse/Min, 2048, 1024, 34.133, 16 Hz
ICM7207A	5 Hz 00 01 00	4-5.5	260	100, 0.391	5.24288 MHz	0.5, 1600 Hz
ICM7207	5 Hz cospicor3	4-5.5	260	100, 0.312	6.5536 MHz	50 Hz, 1280 Hz
ICM7213	16 Hz	2-4	100	Sq. Wave	4.19 MHz	1 Pulse/Min, 2048, 1024, 34.133, 1 Hz
ICM7207	50 Hz	4-5.5	260	20, 0.312	6.5536 MHz	5 Hz, 1280 Hz
ICM7213 ICM7213 ICM7207A ICM7207	1000 Hz 1024 Hz 1280 Hz 1600 Hz	2-4 2-4 4-5.5 4-5.5	100 100 260 260	Sq. Wave Sq. Wave Sq. Wave Sq. Wave	4.096 MHz 4.19 MHz 5.24288 MHz 6.5536 Mhz	2000, 2000 Pulses/Min 1 Pulse/Min, 2048, 34.133, 16, 1 Hz 0.5, 5 Hz 5, 50 Hz
ICM7213	2048 Hz	2-4	100	Sq. Wave	4.19 MHz	1 Pulse/Min, 1024, 34.133, 16, 1 Hz
ICM7209	250 kHz- 10 MHZ	4.5-5.5	11,000	Sq. Wave	1-10 MHz	(Note 2)

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#### Notoe

1. Oscillator/controller for frequency counter.

2. Two buffered outputs—Crystal Frequency and +8 output. Drives up to 5 TTL loads.

M These counters will missure frequency when used with the ICMT207 (0.01 and 0.1 second timebase) or the ICMT207A (0.1 and 1.0 second bimebase)

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# OF FEATURES AND ENGLISHED ON THE CHARACTERS DISPLAY OR DIGITS TYPE FONT INTERFACE 0.P. # of Decimal Points or Annunciators
# of Alphanumeric 14 Segments + D.
# of Alphanumeric 16 Segments
# of Alphanumeric 18 Segments
# of Alphanumeric 18 Segments Annunclators and Blank) # of Dot Matrix

LED. Common Anode Nor-MUX

LED. Common Cethode MUX

LED. Common Anode MUX

LCD. Direct Drive

LCD. # of Ways MUX'D

Vacuum Fluorescent

Hexadecimal (0-9, A-F)

Code 8 (0-9, H, E, L, P., and Bia ant Digits Points or # of 7-Segment (su) Cycle TYPE . . 0 1000 Drives Conventional LCD Displays. Includes RC ICM7211 0 Oscillator, Divider Chain, Latches, Interface and LCD ICM72114 0 0 ICM7211M 0 . Drivers. Evaluation Kit Available ICM7211AM 200 Δ . 0 ICM7212 0 0 1000 -4-. Drives Common Anode LED Displays. 28 Current ICM7212A • . 0 Controlled Outputs. Includes Latches, Interface and ICM7212M 0 . Brightness Control. Evaluation Kit Available. ICM7212AM 4 0 . 200 . ICM7218A 0 0 0 8 8 . 3 Decode Formats Drives UP to 64 Independent LED's. ICM7218B 0 0 . 550 Includes 8x8 Memory, Multiplexed LED Drivers, 8 8 0 0 0 ICM7218C . Decoders, Interface and control. Applications Include ICM7218D 0 0 8 8 . 0 500 Bar Graphs. State to repersy bende apile 1-SOMEM! 0 0 ICM7218E 8 8 . . 8 Digits, 16 Annunciators on COM 3, Hexadecimal 8 16 0 0 500 ICM7231A 3 8 Digits, 16 Annunciators on COM 3, Code B 8 16 . 0 500 3 8 Digits, 16 Annunicators on COM 1+3, Code B ICM7231C 8 16 3 . 0 500 ICM7232A ● 350 10 Digits, 20 Annunciators on COM 3, Hexadecimal 3 . ICM7232B 10 20 10 Digits, 20 Annunciators on COM 3, Code B ● 350 3 . ICM7232C 10 20 ● 350 10 Digits, 20 Annunciators on COM 1+3, Code B 3 0 0 0 ICM7233A 500 4 Alphanumeric Characters. Evaluation Kit Available 3 ICM7233B 500 4 Alphanumeric Characters, Full-Width Numbers 3 ICM7234A 3 5 Alphanumeric Characters, Half-Width Numbers ● 350 ICM7234B 3 9 ● 350 5 Alphanumeric Characters. Full-Width Numbers Drives 30 Volt Vacuum Fluorescent Displays Directly. ICM7235 . 0 0 ICM7235A 1000 Includes Latch/Decoder µP Interface or 4-Bit Input. 0 0 4 . ICM7235M 0 200 Hexadecimal or Code B Format Available. . 4 ICM7235AM 4 . 0 0 200 ICM7243A 250 8 Alphanumeric Characters + Decimal Pt. can be Daisy 8 . 0 0 ICM7243B 250 Chained or Cascaded, Evaluation Kit Available. 8 . 0 0 1x80 Ch. Dot Matrix LCD Controller and Row Driver. 78 ICM7280° 0 . 14 400 80 10 Use with ICM7281. 2x40 Ch. Dot Matrix LCD Controller and Row Driver. 16 0 0 400 14 80 ICM7283\* Use with ICM7281. ICM7281\* Column Driver for use with ICM7280 or ICM7283. \*New Product

#### Microcontrollers, Microperipherals, Memory

#### Microcontrollers CHA STAUTAST

BASIC PART NUMBER	DESCRIPTION	f <sub>c</sub> MHz	MEMO	0.750700-0.0	PACKAGE	TEMPERATURE		
NUMBER	DESCRIPTION		101112	ROM	RAM	司 國際語	(°C)	
IM80C48*	8048/80C48 Family Compatible	188	6	1K x 8	64 x 8	PL, JL	181	
IM80C49*	2X the memory of IM80C48	*   1913	6	2K x 8	128 x 8	PL, JL	0 - +70	
IM80C35*	Same as IM80C48 without ROM	\$ 1 Jak	6	None	64 x 8	PL, JL	-40 - +85	
IM80C39*	Same as IM80C49 without ROM	8 5 5 5	6	None	128 x 8	PL JL	9 6	

DISPLAT

#### Microprocessor Peripherals — See also Display Drivers, Counters, A/D, and D/A Converters.

TYPE	addition A ID rectaular DESCRIPTION to B	f <sub>C</sub> (MHz) Max	PACKAGE	TEMPERATURE RANGE (°C)
ICM7170*	μP-Compatible Real-Time Clock, Binary Time Format, Micropower Standby Operation (2μΑ @ 2.8V)	4.19	PG, JG	-40 — +85
IM6402 IM6402-1 IM6402A	CMOS Industry Standard Compatible UART High-Speed Version of IM6402 10V Operating Version of IM6402	1.0 2.0 4.0	PL, JL PL, JL	-40 - +85 -55 - +125
IM6403 IM6403-1 IM6403A	Like Corresponding IM6402  Device but with On-board Crystal  Oscillator and Baud Rate Generator	2.46 3.58 6.0	PL PL, JL PL, JL	-40 - +85 -55 - +125
M82C43*	CMOS I/O Expander for 80C48/49 Microcomputers	0	PG, JG	0 - +70 -40 - +85
IM4702/12	Baud Rate Generator	3.58	PE, JE	-40 - +85

#### CMOS EPROMS CONTROL OF THE CONTROL OF T

ORGANIZATION/ TYPE	MAX ACCESS TIME (ns)	v <sub>cc</sub>	I <sub>CC</sub> MAX (mA) OPERATING	ICC MAX (µA) STANDBY	PACKAGE	TEMPERATURE RANGE (°C)
1024 x 4	Total Salomico Do	NOTES OF STATE	ritive patt 5	9 9 67	08	CIATZERO 154
IM6653I	550	5	6	140	JG	-40 - +85
IM6653M	600	5	40 0805 6 006	140 86	JG	-55 - + 125
IM6653-11	450	5	riliw sall 6	140	JG	-40 - +85
IM6653AI	300	10	12	140	JG	-40 - +85
IM6653AM	350	10	12	140	JG	-55 - + 125
512 x 8				THE RESERVE TO SERVE		New Product
IM6654I	550	5	6	140	JG	-40 - +85
IM6654M	600	5	6	140	JG	-55 - +125
IM6654-11	450	5	6	140	JG	-40 - +85
IM6654AI	300	10	12	140	JG	-40 - +85
IM6654AM	350	10	12	140	JG	-55 - +125

<sup>\*</sup>New Product

# Section 2 — Discretes

Section 2 - Discretes

#### 2N2607-2N2609 2N2609JAN

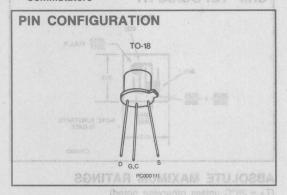
P-Channel JFET
General Purpose Amplifier

# Low Level Onoppers

e Data Switches

#### **APPLICATIONS**

- Low-Level Choppers
- Data Switches
- Commutators

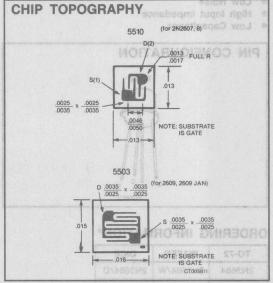


#### **ORDERING INFORMATION\***

TO-18	WAFER	DICE
2N2607	2N2607/W	2N2607/D
2N2608	2N2608/W	2N2608/D
2N2609	2N2609/W	2N2609/D
2N2609JAN	2445 _ 3035	2N2665 2N

\*When ordering wafer/dice refer to Section 10, page 10-1.

# Low Noise Amplifier FEATURES COW HORSE LOW CONSTRUCT LOW CONSTRUCT COW HORSE LOW CONSTRUCT



#### ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted)

Gate-Source Voltage	30V
Gate-Drain Voltage	30V
Gate Current	
Storage Temperature Range65°C to	+200°C
Operating Temperature Range55°C to	+175°C
Lead Temperature (Soldering, 10sec)	. +300°C
Power Dissipation	300mW
Derate above 25°C	2mW/°C

#### ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

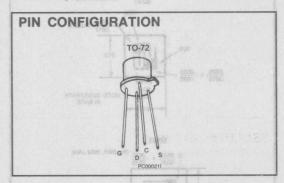
Au lac	2.0-   2.0-	18.0-	-0.5		607	2N2608		2N2609		UNIT
SYMBOL	PARAMETER	TEST CONI	MIN	MAX	MIN	MAX	MIN	MAX		
Cata Ballanda Carrata		V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0	0 = 85A 'A08	" SOV	-3	to other to	10	Cammac	30	nA
IGSSR	Gate Reverse Current	V <sub>GS</sub> = 5V, V <sub>DS</sub> = 0, T <sub>A</sub> = 150°C			3		10	Conduct	30	μΑ
BVGSS	Gate-Drain Breakdown Voltage	$1_{G} = 1 \mu A, V_{DS} = 0$				30	enwoß	30		V
Vp	Gate-Source Pinch-Off Voltage	$V_{DS} = -5V$ , $I_{D} = -1$	μA 0 = gay Vos	- abv L	4	_1_	4	Blog and	4	V
IDSS	Drain Current at Zero Gate Voltage	$V_{DS} = -5V, V_{GS} = 0$	) (I elon) s	-0.30	-1.50	-0.90	-4.50	-2	-10	mA
9fs a	Small-Signal Common-Source Forward Transconductance	V <sub>DS</sub> = -5V, V <sub>GS</sub> = 0	), f = 1kHz	330		1000	stance gure (No	2500	(ac	μs
C <sub>iss</sub>	Common-Source Input Capacitance	V <sub>DS</sub> = -5V, V <sub>GS</sub> = 1 (Note 1)	IV, f = 1MHz	Veg =	10		17		30	pF
N.E		$V_{DS} = -5V$ , $V_{GS} = 0$ , $V_{GS} = 0$ , $V_{GS} = 1$ , $V_{GS} = 1$		boses	330	rah yin	o signans	len ngia	t For di	370
NF	Noise Figure (Note 1)						3	100	3	dB

NOTE 1: For design reference only, not 100% tested.

#### Low Noise Amplifier

#### **FEATURES**

- Low Noise
- High Input Impedance
   HIGH Input Impedance
- Low Capacitance



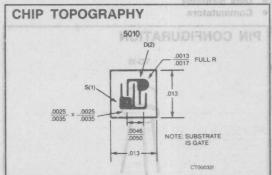
#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N3684	2N3684/W	2N3684/D
2N3685	2N3685/W	2N3685/D
2N3686	2N3686/W	2N3686/D
2N3687	2N3687/W	2N3687/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### APPLICATIONS

- Low Level Choppers
- **Data Switches**
- Multiplexers
- Low Noise Amplifiers



#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

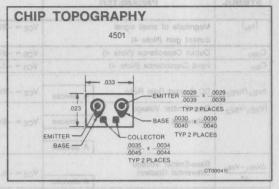
Gate-Source or Gate-Drain Voltage	50V
Gate Current	50mA
Storage Temperature Range65°C	to +200°C
Operating Temperature Range55°C	to +175°C
Lead Temperature (Soldering, 10sec)	+ 300°C
Power Dissipation	
Derate above 25°C	.2.0mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

20004	U*d6= egnar eruhate	Operating Temp	2N3	684	2N3685		2N3686		2N3687		equal (
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
BVGSS	Gate to Source Breakdown Voltage	$V_{DS} = 0$ , $I_{G} = 1.0 \mu A$	-50		-50		-50		-50		
V <sub>P</sub>	Pinch-Off Voltage	$V_{DS} = 20V$ , $I_{D} = 0.001 \mu A$	-2.0	-5.0	-1.0	-3.5	-0.6	-2.0	-0.3	-1.2	V
IGSS	Total Gate Leakage Current	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0	-	-0.1		-0.1	towaster's	-0.1		-0.1	nA
00	T <sub>A</sub> = 150°C			-0.5		-0.5		-0.5		-0.5	μΑ
IDSS	Saturation Current, Drain-to-Source	V <sub>GS</sub> = 0, V <sub>DS</sub> = 20V	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA
Y <sub>fs</sub>	Forward Transadmittance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	2000	3000	1500	2500	1000	2000	500	1500	μs
Gos	Common Source Output Conductance	f = 1kHz	egV -W	50	4	25	Inera	10	vell als	5	μs
Ciss	Common Source Input	06 0	soy a	4.0		4.0	/ nevols	4.0	land-sig	4.0	pF
V	Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	. dl . vi			egatiko	11000	on Pini	1008-600	al	Va
Crss	Common Source Short Circuit Reverse Transfer Capacitance	f=1MHz (Note 1)	IV. Vo	1.2		1.2	Zerr G	1.2	ale Cue	1.2	pF
rDS(on)	On Resistance	$V_{DS} = 0, V_{GS} = 0$		600		800	S-sports	1200	ole lies	2400	ohms
NF	Noise Figure (Note 1)	$f = 100Hz$ , $R_G = 10M\Omega$	(C) A 'AC	0.5		0.5	natoubr	0.5	trawa	0.5	dB
9g 00	31 01	$NBW = 6Hz, V_{DS} = 10V,$ $V_{GS} = 0V$	av, va	- Pag			Bagn!	ออามกร	ctomene	9	Cies

NOTE 1: For design reference only, not 100% tested.

# PIN CONFIGURATION TO-78 SHADE A AGENT A AGEN



#### **ORDERING INFORMATION\***

TO-78	WAFER	DICE
2N3810	2N3810/W	2N3810/D
2N3810A		
2N3811	2N3811/W	2N3811/D
2N3811A		No.

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

#### ABSOLUTE MAXIMUM RATINGS

(T <sub>A</sub> = 25°C unless otherwise noted)	
Emitter-Base Voltage (Note 1)	5V
Collector-Base or Collector-Emitter Voltage	
(Note 1)	60V
Collector Current (Note 1)	50mA
Storage Temperature Range65°C	
Operating Temperature Range55°C	to +175°C
Lead Temperature (Soldering, 10sec)	+ 300°C
ONE SIDE	BOTH SIDES

Power Dissipation 500mW 600mW Derate above 25°C 3.3mW/°C 4.0mW/°C

#### **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

						2N3811/A		
SYMBOL	PARAMETER	TEST CONDITIONS			MAX	MIN	MAX	UNIT
BVCBO	Collector-Base Breakdown Voltage	$I_{C} = -10\mu A$ , $I_{E} = 0$	$I_{C} = -10\mu A, I_{E} = 0$					
BVCEO	Collector-Emitter Breakdown Voltage (Note 2)	I <sub>C</sub> = -10mA, I <sub>B</sub> = 0		-60		-60		V
BVEBO	Emitter-Base Breakdown Voltage	$I_E = -10\mu A$ , $I_C = 0$	$I_E = -10\mu A, I_C = 0$			-5		
IC(off)	Collector Cutoff Current	Mark Control of the			-10		-10	nA
	$T_A = +150^{\circ}C$	$V_{CB} = -50V, I_{E} = 0$			-10	, Marin	-10	μΑ
IE(off)	Emitter Cutoff Current	V <sub>BE</sub> = 4V, I <sub>C</sub> = 0			-20		-20	nA
hFF			$I_C = -10\mu A$	100	11/5	225		
	Static Forward Current	$V_{CE} = -5V$	$I_C = -100\mu A$ to $-1mA$	150	450	300	900	
"FE	Transfer Ratio		I <sub>C</sub> = 10mA (Note 2)	125		250		
	$T_A = -55^{\circ}C$		$I_C = 100\mu A$	75	T-want	150		
V	Base-Emitter Saturation Voltage	V <sub>CE</sub> = -5V	$I_B = -10\mu A$		-0.7		-0.7	1917
VBE(sat)	Base-Emitter Saturation Voltage	$I_{\rm C} = -100 \mu {\rm A}$	$I_B = -100\mu A$		-0.8		-0.8	
VCE(sat)	Collector-Emitter Saturation Voltage	$I_B = -10\mu A$ , $I_C = -10\mu A$	100μΑ		-0.2		-0.2	V
	(Note 2)	$I_B = -100 \mu A$ , $I_C = -$	-1mA		-0.25		-0.25	
hie	Input Impedance (Note 4)	V <sub>CE</sub> = -10V		3	30	10	40	kS
h <sub>fe</sub>	Forward Current Transfer Ratio (Note 4)	$I_C = -1mA$		150	600	300	900	
h <sub>re</sub>	Reverse Voltage Transfer Ratio (Note 4)	f = 1kHz		1	0.25		0.25	
hoe	Output Admittance (Note 4)			5	60	5	60	μ

#### 2N3810/A, 2N3811/A



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

OVMDOL	DADAMETED		TEST CONDITIONS			2N3810/A		2N3811/A	
SYMBOL	PARAMETER	TOPOG				MAX	MIN	MAX	UNIT
Ihfel	Magnitude of small signal		V <sub>CE</sub> = -5V	I <sub>C</sub> = -1mA, f = 100MHz	1	5	1	5	
	current gain (Note 4)		<b>建筑线</b>	$I_C = -500 \mu A$ , $f = 30 MHz$	100	VI.	1		
C <sub>obo</sub>	Output Capacitance (Note 4)		V <sub>CB</sub> = -5V, I <sub>E</sub> =	0, f = 1MHz		4		4	
C <sub>ibo</sub>	Input Capacitance (Note 4)		V <sub>CB</sub> = -0.5V, I <sub>C</sub> = 0, f = 1MHz			8		8	pF
	- FED -	-60			0.9	1.0	0.9	1.0	
hFE <sub>1</sub> /hFE <sub>2</sub>	DC Current Gain Ratio	A devices	$V_{CE} = -5V$ , $I_{C} =$	0.95	1.0	0.95	1.0		
VBE1-VBE2	Base-Emitter Voltage	p csu		$I_C = 10\mu A$ to 10mA	114-0	-5		-5	
	Differential	A devices	$V_{CE} = -5V$		1111	-2.5		-2.5	mV
	COLLECTOR TYPE PLACE	V- nervous		$I_C = 100 \mu A$	1111	-3		-3	
	4690 x 8000	A devices			1551	-1.5		-1.5	
$\frac{\Delta V_{BE_1} - V_{BE_2}}{\Delta T}$	Base-Emitter Voltage Differential Gradient	A devices	$V_{CE} = -5$ , $I_{C} = 1$	Αμ00	/5 /6 u 109834	10 5		10 5	μV/°C
	SOMITAR MUMIX	LUTE MA		= $-100\mu$ A, R <sub>G</sub> = $3k\Omega$ , Bandwidth = $20$ Hz	OTA	MÃO	91449	4	(30A)
NF	(baton sziwiedło Spot Noise Figure (atol/) a			= $-100\mu$ A, R <sub>G</sub> = $3K\Omega$ , Bandwidth = $200k$ Hz	1010	3	WAFE	1.5	C-OT
/08	agatioV retrimitate Voltage		V <sub>CE</sub> = -10V, I <sub>C</sub> f = 10kHz, Noise	= $-100\mu$ A, R <sub>G</sub> = $3k\Omega$ Bandwidth = $2k$ Hz	NOTEER	2.5	OTUSE	1.5	dB
	(Note 4)		V <sub>CE</sub> = -10V, I <sub>C</sub> Noise Bandwidth	= $-100\mu$ A, R <sub>G</sub> = $3k\Omega$ , = 15.7kHz (Note 3)	VEREN Y	3.5	11867	2.5	

NOTES: 1. Per transistor.

1. Fer transistor.
2. Pulse width ≤ 300 µs, duty cycle ≤ 2.0%.
3. 3dB down at 10Hz and 10kHz.
4. For design reference only, not 100% tested.

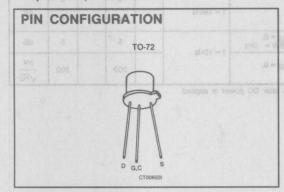
	ANT	21428	ANDI					
Tibili		para,						
								08018
			-01-					
					Amr - of August - and			
							Base-Emitter Saturation Voltage	
					Auto	01 10 MA: 15 10		
							Forward Current Transfer Radio (Note 4)	
						( = 1)d-(z		
			00					

# 2N3821, 2N3822, JAN, JTX, JTXV N-Channel JFET

N-Channel JFET High Frequency Amplifier

#### **FEATURES**

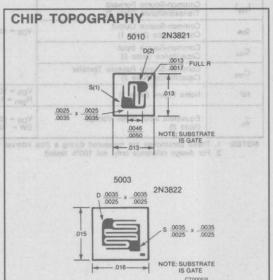
- Low Capacitance
- Up to 6500 μs Transconductance



#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

\*When ordering wafer/dice refer to Section 10, page 10-1. †add JAN, JTX, JTXV to basic part number to specify these devices.



#### **ABSOLUTE MAXIMUM RATINGS**

 (TA = 25°C unless otherwise noted)

 Gate-Source Voltage
 -50V

 Gate-Drain Voltage
 -50V

 Gate Current
 10mA

 Storage Temperature Range
 -65°C to +200°C

 Operating Temperature Range
 -55°C to +175°C

 Lead Temperature (Soldering, 10sec)
 +300°C

 Power Dissipation
 300mW

 Derate above 25°C
 2.0mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	DADAMETER	TEGT COMPLETIONS	2N3	2N3821		2N3822		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
IGSS				-0.1		-0.1	nA	
	Gate Reverse Current T <sub>A</sub> = 150°C	$V_{GS} = -30V, V_{DS} = 0$		-0.1		-0.1	μΑ	
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$	-50		-50			
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 0.5nA		-4		-6		
VGS		$V_{DS} = 15V, I_D = 50\mu A$	-0.5	-2			7 V	
	Gate-Source Voltage	$V_{DS} = 15V$ , $I_{D} = 200 \mu A$			-1	-4		
DSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	0.5	2.5	2	10	mA	

9fs	Common-Source Forward Transconductance (Note 1)	19	f = 1kHz	1500	4500	3000	6500	TOIL
lyfs	Common-Source Forward Transadmittance (Note 2)	CHIP	f = 100MHz	1500		3000	3 12 12 1	μs
9os	Common-Source Output Conductance (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	f = 1kHz		10	onetio	20	wal
Ciss	Common-Source Input Capacitance (Note 2)			babno	6	Chia J	6	qu
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)		f = 1MHz	MOL	3	FIGU	430	pF
NF	Noise Figure (Note 2)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, R <sub>gen</sub> = 1meg, BW = 5Hz	f = 10Hz	57-0	5		5	dB
ēn	Equivalent Input Noise Voltage (Note 2)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, BW = 5Hz	1 - 10/12	-	200		200	nV √H

NOTES: 1. These parameters are measured during a 2ms interval 100ms after DC power is applied.

2. For design reference only, not 100% tested.

опредіна інголиатіон"

70-72 WAFER DIGE 2N3821 SN3821/D SN3821/D 2N3822 SN3822/W SN3832/D

ABSOLUTE WAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted) Cete-Sharos Voltage

Gate-Drain Voltage — 50

Gate Current — 10m

Storage Temperature Range — 55°C to + 175°

Operating Temperature Range — 55°C to + 175°
Lead Temperature (Roldering 10mm) — 430°

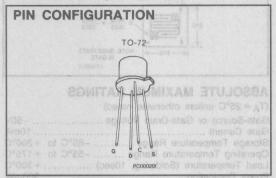
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noteth

			1.0-		

#### **High Frequency Amplifier**

#### **FEATURES**

- Low Noise
- Low Capacitance
- Transductance Up to 6500 µs



#### ORDERING INFORMATION\*

TO-72	WAFER	DICE	1
2N3823	2N3823/W	2N3823/D	1

\*When ordering wafer/dice refer to Section 10, page 10-1. †add JAN,JTX,JTXV to basic part number to specify these devices

# CHIP TOPOGRAPHY .0035 0025 FULL R .0035 x .0035 NOTE: SUBSTRATE

#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage30V
Gate Current
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +175°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation300mW
Derate above 25°C2.0mW/°C

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

SYMBOL	PARAMETE	RIGHTIGHOO	TEST CO	MIN	MAX	UNIT	
	THE RESERVE THE PROPERTY OF THE PARTY OF THE	and the second of the second o	and the second s	ere executation libraries	-0.5	nA	
IGSS	Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = -20V, V_{DS} = 0$	Payerse	-0.5	μΑ	
BVGSS	Gate-Source Breakdown Vo	Itage	$I_G = 1\mu A$ , $V_{DS} = 0$	Al	-30		
VGS(off)	Gate-Source Cutoff Voltage		$V_{DS} = 15V, I_{D} = 0.5nA$	aganov nwopxee	HE SUMBO	-8	V
VGS	Gate-Source Voltage	V40	$V_{DS} = 15V$ , $I_{D} = 400 \mu A$	-1.0	-7.5	mount	
IDSS	Saturation Drain Current		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		20	mA
9fs	Common-Source Forward Transconductance (Note 1)		Vos = 15V, Vos = 0	f = 1kHz	3,500	6,500	Cine Cine
Yfs	Common-Source Forward Transadmittance (Note 2)			f = 100MHz	3,200	anoD	
9os	Common-Source Output Transconductance (Note 1)		- adv .vo - abv	f = 1kHz	(P)	35	μs
9iss .	Common-Source Input Conductance (Note 2)		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	f = 200MHz		800	16 33
9oss .	Common-Source Output Conductance (Note 2)				200		
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)			f = 1MHz		6	pF
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note	Source Reverse				2	pr
NF	Noise Figure (Note 2)		$V_{DS} = 15V$ , $V_{GS} = 0$ $R_G = 1k\Omega$	f = 100MHz		2.5	dE

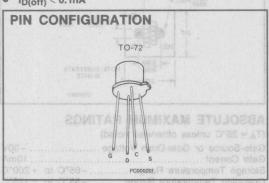
NOTES: 1. These parameters are measured during a 2ms interval 100ms after DC power is applied. 2. For design reference only, not 100% tested.

#### 2N3824 N-Channel JFET Switch



#### **FEATURES**

- rds < 250 Ohms
- ID(off) < 0.1nA



#### ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N3824	2N3824/W	2N3824/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted

CHIP	TOPOGRAPHY	
	5003 STREET WOLLD CONTROL OF S	
	015 s .0035 x .0035 .0025 .0025 .0025	
	CT00051I	

#### ABSOLUTE MAXIMUM RATINGS

ADOUGH IN MAINTAIN
(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage50V
Gate Current
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +175°C
Load Temperature (Soldering, 10sec)+300°C
Power Dissipation
Derate above 25°C2.0mW/°C

tedd JAN, JTX, JTXV to basic part number to specify trese devices

10		2	
elektrikenseljes	and the second second second		

					LIN	IITS	
SYMBOL	PARAMETER M	orrigues Ti	TEST COND	ITIONS TEMARAS	MIN	MAX	UNIT
An I a		0	" 80V VDS- = 80V Tone	se Cureral	noveA ed	o E−0.1	nA
IGSS	Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = -30V, V_{DS} = 0$	postfoli medisposii i	en collection	-0.1	μΑ
BVGSS	Gate-Source Breakdown Voltage	Li	$I_{G} = 1 \mu A, V_{DS} = 0$	society Motors	-50		V
		Avi	100 = ct . 407 or act/	animin/ a	- na.	0.1	nA
ID(off)	Drain Cutoff Current	T <sub>A</sub> = 150°C	$V_{DS} = 15V, V_{GS} = -8V$	State Current	mokatik	0.1	μΑ
rds(on)	Drain-Source ON Resistance		V <sub>GS</sub> = 0V, I <sub>D</sub> = 0	f = 1kHz		250	Ω
Ciss	Common-Source Input Capacitance (Note 1)		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	clance (Note 1)		6	6)(3
C <sub>rss</sub>	Common-Source Reverse Transfer C (Note 1)	apacitance	V <sub>GS</sub> = -8V, V <sub>DS</sub> = 0	f = 1MHz and a sour	dinibaso	3	pF

NOTE 1: For design reference only, not 100% tested.

OGB

2HMACOS = 1

OGB

2HMACOS

## **2N3921, 2N3922**Dual N-Channel JFET

Dual N-Channel JFET General Purpose Amplifier

#### FEATURES HAR XAM HAR

- Low Drain Current
- High Output Impedance
- Matched VGS, AVGS, and gfs

# PIN CONFIGURATION TO-71 S, D, G, D, S, G, D, PC000511

#### **ORDERING INFORMATION\***

TO-71	WAFER	DICE
2N3921	2N3921/W	2N3921/D
2N3922	2N3922/W	2N3922/D

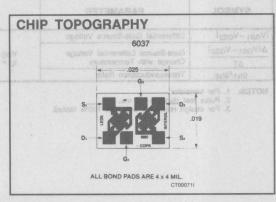
\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDI	TIONS	MIN	MAX	UNIT
						-1	nA
IGSS	Gate Reverse Current	T <sub>A</sub> = 100°C	$V_{GS} = -30V, V_{DS} = 0$			-1	μΑ
BVDGO	Drain-Gate Breakdown Voltage		$I_D = 1 \mu A, I_S = 0$		50		
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage		V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA			-3	٧
VGS	Gate-Source Voltage		$V_{DS} = 10V, I_{D} = 100 \mu A$		-0.2	-2.7	
						-250	рА
IG	Gate Operating Current	T <sub>A</sub> = 100°C	$V_{DG} = 10V, I_D = 700\mu A$			-25	nA
IDSS	Saturation Drain Current (Note 1)		V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		1	10	mA
9fs	Common-Source Forward Transconductance (Note 2)			f=1kHz	1500	7500	
gos	Common-Source Output Conductance		101/1/	1-18112		35	μs
Ciss	Common-Source Input Capacitance (Note 3)		$V_{DS} = 10V, V_{GS} = 0$			18	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitan (Note 3)	се		f=1MHz		6	pF
9fs	Common-Source Forward Transconductance	STATE FILE			1500		
goss	Common-Source Output Conductance		$V_{DG} = 10V, I_D = 700\mu A$	f = 1kHz	1000	20	μs
NF	Spot Noise Figure (Note 3)		V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0	f = 1kHz, R <sub>G</sub> = 1meg		2	dB

## **BINITERSIL**



#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage (Note 1)50V
Gate Current (Note 1) 50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +200°C
Load Temperature (Soldering, 10sec)+300°C
Total Power Dissipation300mW
Derate above 25°C1.7mW/°C

SYMBOL	PARAMETER	TEST C	CONDITIONS	2N3	921	2N3	3922	UNIT
STWIBUL	YHRAROOROT S	INO I LESI C	CNDITIONS	MIN	MAX	MIN	MAX	TABE
IVGS1-VGS2	Differential Gate-Source Voltage		PRESIDENT OF		5	Curre	5	mV
$\frac{\Delta  V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Differential Voltage Change with Temperature	$V_{DG} = 10V,$ $I_{D} = 700\mu A$	T <sub>A</sub> = 0°C T <sub>B</sub> = 100°C	er and ena	10	ini h	25	μV/°C
9fs1/9fs2	Transconductance Ratio		f = 1kHz	0.95	1.0	0.95	1.0	2.030

NOTES: 1. Per transistor.

2. Pulse test duration = 2 ms.

3. For design reference only, not 100% tested.

ALL BOND PAGE ARE'S X 4 MIL.
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#### ABSOLUTE MAXIMUM RATINGS

11 A = 25°C uniess comennies noted)

Gate-Source or Gate-Orain Voltage (Note 1) ... -50V

Gate Current (Note 1) ... 50mA

Storage Temperature Range ... -55°C to +200°C

Operating Temperature Range ... -55°C to +200°C

Load Temperature (Soldering, 10sec) ... +300°C



#### DEDERING INFORMATION\*

		MIRAW	TO-71
insin	Marie Barrier Rational Strategic Barrier Strategic Barrier		
	CATSECHS		

Whon produing water/dice refer to Section 10, page 10-1.

#### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: (25°C unless otherwise neted

		EGERA		TEST CONDIT			
Art							
				g = 50A 'A08 - = 59A			
						Drain-Gala Breakdown Voltage	
				Ant = gl., V01 = anv			
				Vos = 10V, 10 = 100gA			
				V0G = 10V, 10 = 700pA	0°001 = AT		
	OF			Vos = 10V, Vos = 0		Saturation Drain Ourreint (Note 1)	loss
	7500		Tertification of the state of t			Common-Source Forward Transconductance (Note 2)	
24	96			Vos=10V, Vos=0		Common-Source Output Conductance	
						Contract-Source Input Capacitance	
			2+16/1=1		agacilance	Common-Source Reverse Transfur C (Note: 3)	
						Corsmon-Source Forward Transcond	
BU				Non = 10V. (p = 700ps.			
Eb.	2		f = fielz Rg = tmag	Vos = 10V, Vos = 9		Spot Noise Figure (Note 2)	

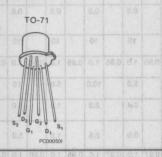
#### Dual IT VIIAIIICI VI LI

#### General Purpose Amplifier

#### **FEATURES**

- Low Offset and Drift
- Low Capacitance
- Low Noise
- Superior Tracking Ability
- Low Output Conductance

#### PIN CONFIGURATION

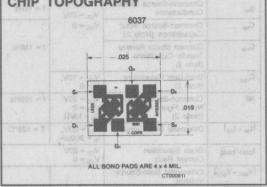


#### **ORDERING INFORMATION\***

TO-71	WAFER	DICE
2N3954	2N3954/W	2N3954/D
2N3954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

#### CHIP TOPOGRAPHY

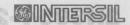


#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Drain or Gate-Source Voltage50V
Gate-to-Gate Voltage±50V
Gate Current50mA
Total Device Dissipation 85°C (Each Side)250mW
Case Temperature (Both Sides)500mW
Power Derating (Each Side) 2.86mW/°C
(Both Sides)4.3mW/°C
Storage Temperature Range65°C to +200°C
Lead Temperature (1/16" from case
for 10 seconds)300°C

OVINDAL			o	ONDITIONS	2N3	2N3954		2N3954A		2N3955		955A	2N3	3956	2N3	2N3957 2N		958	
SYMBOL	PARAN	IETEK	TEST C	ONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNI
	Gate Reverse	e Current	$V_{GS} = -30V$ ,			-100	88733	-100		-100		-100		-100		-100		-100	pA
IGSS		T <sub>A</sub> = 125°C	V <sub>DS</sub> = 0			-500		-500		-500		-500		-500		-500		-500	nA
BV <sub>GSS</sub>	Gate-Source Breakdown V	oltage	$V_{DS} = 0$ $I_{G} = -1\mu A$		-50		-50		-50		-50		-50		-50		-50		
V <sub>GS(off)</sub>	Gate-Source Voltage	Cutoff	$V_{DS} = 20V,$ $I_D = 1nA$		-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	130
V <sub>GS(f)</sub>	Gate-Source Voltage	Forward	$V_{DS} = 0$ $I_G = 1 \text{mA}$			2.0		2.0		2.0		2.0		2.0		2.0		2.0	V
				$I_D = 50\mu A$		-4.2	. In	-4.2		-4.2		-4.2		-4.2		-4.2		-4.2	
V <sub>GS</sub>	Gate-Source	Voltage	$V_{DS} = 20V$	$I_{D} = 200 \mu A$	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.4	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	N. F.
	Gate Operating	g Current	V <sub>DS</sub> = 20V,			-50		-50	1	-50		-50		-50	To be	-50		-50	pA
IG		T <sub>A</sub> = 125°C	$I_{D} = 200 \mu A$			-250		-250		-250		-250		-250		-250		-250	nA
I <sub>DSS</sub>	Saturation Dra Current	in	$V_{DS} = 20V,$ $V_{GS} = 0$	N. S.	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA

#### 2N3954-2N3958 2N3954A/2N3955A



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

				2N3	954	2N39	954A	2N3	955	2N39	955A	2N3	956	2N3	957	2N3	958	34.1
SYMBOL	PARAMETER	TEST CC	NDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNI
	Common-Source Forward		f = 1kHz	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	
g <sub>fs</sub>	Transconductance	(Note 2)	f = 200MHz	1000		1000		1000		1000		1000		1000		1000		
g <sub>os</sub>	Common-Source Output Conductance	V <sub>DS</sub> = 20V,	f = 1kHz		35		35		35		35		35	lows	35	ukiri Mari	35	μs
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)	$V_{GS} = 0$			4.0		4.0		4.0		4.0		4.0	vocu	4.0	Cap	4.0	9 4
C <sub>rss</sub>	Common Source Reverse Transfer Capacitance (Note 2)		f = 1MHz		1.2		1.2		1.2		1.2	offitty tame	1.2	nkis naO	1.2	noh Duti	1.2	pF
C <sub>dgo</sub>	Drain-Gate Capacitance (Note 2)	$V_{DG} = 10V,$ $I_{S} = 0$			1.5		1.5		1.5		1.5	DIT	1.5	UD	1.5	100	1.5	150
NF	Common-Source Spot Noise Figure (Note 2)	$V_{DS} = 20V$ $V_{GS} = 0$ $R_G = 10M\Omega$	f = 100Hz		0.5		0.5		0.5		0.5	1-01	0.5		0.5		0.5	dB
$\left  I_{G1} - I_{G2} \right $	Differential Gate Current	$V_{DS} = 20V,$ $I_{D} = 200\mu A$	T = 125°C		10		10		10		10		10		10		10	nA
I <sub>DSS1</sub> /I <sub>DSS2</sub>	Drain Saturation Current Ratio	$V_{DS} = 20V$ $V_{GS} = 0$		0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	
IV <sub>GS1</sub> -V <sub>GS2</sub> I	Differential Gate-Source Voltage				5.0		5.0		10.0		5.0		15		20		25	
Δ V <sub>GS1</sub> -V <sub>GS2</sub>	Gate-Source Differential	TE MAX	T = 25°C to -55°C		0.8		0.4		2.0		1.2		4.0		6.0		8.0	mV
$\Delta T$	Voltage Change With Temperature	$V_{DS} = 20V,$ $I_{D} = 200\mu A$	T = 25°C to 125°C		1.0		0.5		2.5		1.5	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	5.0		7.5		10.0	
gfs1/gfs2	Transconductance Ratio	. sgafloV st	f = 1kHz	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	

NOTES: 1. Per Transistor.

	186	2263									
			MAM		14925				3553A		
										.400- = 50V	
			-4.5						0.1-		
	0.9									Am and Am = pl	
							0.6-				V <sub>03</sub> V
										$V_{cst} = 20V_c$	

#### **FEATURES**

- Low rDS(on)
   ID(OFF) < 250pA</li>
   Fast Switching

## PIN CONFIGURATION TO-18

#### **ORDERING INFORMATION\***

TO-18	WAFER	DICE
2N3970	2N3970/W	2N3970/D
2N3971	2N3971/W	2N3971/D
2N3972	2N3972/W	2N3972/D

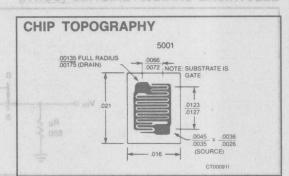
<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

#### **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted

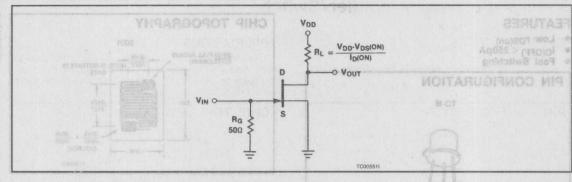
overno.	242445			CONDITIO	NO	2N:	3970	2N:	3971	2N3972		
IDGO	PARAMET	EH	IESI	CONDITIO	NS .	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
BVGSS	Gate Reverse Breakdown	n Voltage	$I_G = -1\mu A$ , $V_{DS}$	= 0		-40		-40		-40	3 19.5	V
DGO	Drain Reverse Current						250		250	HIST.	250	pA
		T <sub>A</sub> = 150°C	$V_{DG} = 20V$ , $I_{S} =$	0			500		500		500	nA
D(off)	Drain Cutoff Current		V 00V V 10V				250	46	250		250	pA
		T <sub>A</sub> = 150°C	$V_{DG} = 20V, V_{GS}$	= -12V			500		500		500	nA
VGS(off)	Gate-Source Cutoff Volta	ige	V <sub>DS</sub> = 20V, I <sub>D</sub> =	1nA		-4	-10	-2	-5	-0.5	-3	٧
IDSS	Saturation Drain Current (Pulse width 300 µs, duty	V <sub>DS</sub> = 20V, V <sub>GS</sub>	= 0		50	150	25	75	5	30	mA	
				ID = 5	mA					8 J. B.	2	
V <sub>DS(on)</sub>	Drain-Source ON Voltage	9	V <sub>GS</sub> = 0	I <sub>D</sub> = 10	mA				1.5			V
				mA		1	19/201					
rDS(on)	Static Drain-Source ON I	Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 1mA				30		. 60		100	
rds(on)	Drain-Source ON Resista	ince	$V_{GS} = 0, I_{D} = 0$		f = 1kHz		30		60		100	Ω
Ciss	Common-Source Input C	apacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> =	= 0 (Note 1)			25		25		25	
Crss	Common-Source Reverse Capacitance	Transfer	V <sub>DS</sub> = 0, V <sub>GS</sub> = (Note 1)	-12V	f = 1MHz		6		6		6	pF
t <sub>d</sub>	Turn-On Delay Time (No	V <sub>DD</sub> = 10V, V <sub>GS</sub>	RL		10		15		40			
tr	Rise Time (Note 1)		2N3970 20m	nA -10V	450Ω		10		15		40	ns
toff	Turn-Off Time (Note 1)		2N3971 10m 2N3972 5m		850Ω 1.6KΩ		30		60		100	

NOTE 1: For design reference only, not 100% tested.

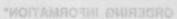


#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage40V
Gate Current 50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +200°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation
Derate above 25°C10mW/°C



#### ABSOLUTE MAXIMUM RATINGS



DICE	WAFER	TO-18
	2NG971/W	

"When ordering water/dice refor to Seption 10, page 10-1.

#### LECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise note

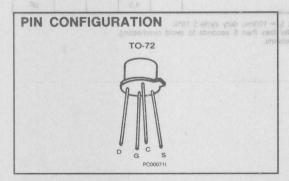
					250	
PARAMETER						
Orașn Reverse Corrent TA - 150°C						
	V <sub>DG</sub> = 20V, V <sub>GS</sub> = -					
				27		
Common-Source Reverse Transfer Ceascilance						
Turn-On Delay Time (Note 1)						
		ig ve -				

WOOTE to Realph reference only, not 100% tested.

Low rps(on)

 High Yts/Ciss Ratio (High-Frequency Figure-of-Merit)

\* реакие



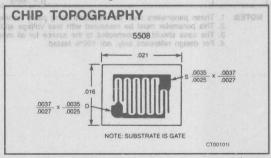
#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N3993	2N3993/W	2N3993/D
2N3994	2N3994/W	2N3994/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **APPLICATIONS**

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch  $\pm 10$  VAC. Can be driven direct from TTL or CMOS logic.



#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)
Drain-Gate Voltage25V
Drain-Source Voltage25V
Continuous Forward Gate Current10mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +175°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation300mW
Derate above 25°C2.0mW/°C

#### **ELECTRICAL CHARACTERISTICS** @ 25°C free-air temperature (unless otherwise noted)

		TEST	CONDITIONS	2N3	1993	2N3	3994	
SYMBOL	PARAMETER		MIN	MAX	MIN	MAX	UNIT	
BVGSS	Gate-Source Breakdown Voltage	$I_G = 1\mu A$ ,	$V_{DS} = 0$	25	PERMIT	25		٧
		$V_{DG} = -15V$ ,	I <sub>S</sub> = 0		-1.2		-1.2	nA
IDGO	Drain Reverse Current	$V_{DG} = -15V$ ,	I <sub>S</sub> = 0, T <sub>A</sub> = 150°C		-1.2		-1.2	μΑ
IDSS	Zero-Gate-Voltage Drain Current	$V_{DS} = -10V,$	V <sub>GS</sub> = 0, (See Note 1)	-10		-2		mA
		$V_{DS} = -10V$	V <sub>GS</sub> = 6V				-1.2	nA
		$V_{DS} = -10V$ ,	V <sub>GS</sub> = 6V, T <sub>A</sub> = 150°C				-1	μΑ
ID(off)	Drain Cutoff Current	$V_{DS} = -10V$ ,	V <sub>GS</sub> = 10V		-1.2			nA
		$V_{DS} = -10V$ ,	V <sub>GS</sub> = 10V, T <sub>A</sub> = 150°C		-1			μΑ
VGS(off)	Gate-Source Voltage	$V_{DS} = -10V$ ,	$I_D = -1\mu A$	4	9.5	1	5.5	٧
rds(on)	Small-Signal Drain-Source On-State Resistance	V <sub>GS</sub> = 0, f = 1kHz	I <sub>D</sub> = 0,		150		300	Ω
lyfsl	Small-Signal Common-Source Forward Transfer Admittance	V <sub>DS</sub> = -10V, f = 1kHz,	V <sub>GS</sub> = 0, (See Note 1)	6	12	4	10	μs
Ciss	Common-Source Short-Circuit Input Capacitance (Note 4)	V <sub>DS</sub> = -10V, f = 1MHz,	V <sub>GS</sub> = 0, (See Note 2)		16		16	pF

#### 2N3993, 2N3994

#### **BINTERSIL**

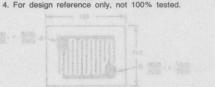
#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL		TES	TEST CONDITIONS		2N3993		2N3994	
	PARAMETER	HINGA	(Note 3)	MIN	MAX	MIN	MAX	UNIT
	Crss Common-Source Short-Circuit Reverse Transfer Capacitance (Note 4)	V <sub>DS</sub> = 0, f = 1MHz	V <sub>GS</sub> = 6V,		LATELLY A	002	no 5	pF
oerib nevnt		$V_{DS} = 0$ , $f = 1MHz$	V <sub>GS</sub> = 10V,		4.5			pF

NOTES: 1. These parameters must be measured using pulse techniques, t<sub>p</sub> = 100ms, duty cycle ≤ 10%.

2. This parameter must be measured with bias voltage applied for less than 5 seconds to avoid overheating.

3. The case should be connected to the source for all measurements.





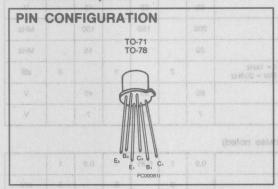
Orain-Source Voltage -25V
Centinuous Forward Gate Current -10mA
Storage Temperature Range -55°C to +200°C
Operating Temperature Range -55°C to +175°C

				XAM:	1979/5	X,0,50	
		V <sub>GS</sub> = 0, (See Note 1)					
		Vgs = 6V, TA = 160°C					
	V05 = -10V						
	,V07 - = 20V					5.5	
Small-Signal Drain-Source On-State Resistance							
	V01 - = 20V ,shift = 1	Vas = 0, (See Note 1)	0		N.		
		VGS * 0,					

General Purpose Amplifier

#### SMASTS SMAGTS SMAGSO UNIT FEATURES HIM XARI SHAR XARE MIM

- High Gain at Low Current
- Low Output Capacitance
- Good hee Match
- Tight VBE Tracking
- Dielectrically Isolated Matched Pairs for **Differential Amplifiers**

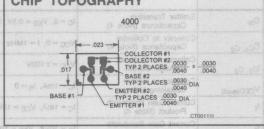


#### **ORDERING INFORMATION\***

TO-78	TO-71	WAFER	DICE
2N4044	2N4878	2N4044/W	2N4044/D
2N4045	2N4879	2N4045/W	2N4045/D
2N4100	2N4880	2N4100/W	2N4100/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### CHIP TOPOGRAPHY



#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

(IA TO C CITIODO CITIOTITICO TIOTO	
Collector-Base or Collector-Emitter 2N4044, 2N4878	
2N4100, 2N4879	55V
2N4045, 2N4880	45V
Collector-Collector Voltage	100V
Emitter Base Voltage (Note 2)	7V
Collector Current (Note 1)	
Storage Temperature Range	65°C to +175°C
Operating Temperature Range	55°C to +175°C
Lead Temperature (Soldering, 10s	ec)+300°C

	THE RESERVE OF THE PARTY OF THE	-71	TO-78		
	ONE	BOTH	ONE	BOTH	
Power Dissipation Derate above 25°C			250mW	500mW	
(mW/°C)		2.7	1.7	3.3	

SYMBOL	PARAMETER	TEST CONDITIONS	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT
10-01-U	85	eloV) V8 = ggV Ami = gl	MIN	MAX	MIN	MAX	MIN	MAX	
hFE	DC Current Gain	$I_C = 10 \mu A$ , $V_{CE} = 5V$	200	600	150	600	80	800	
Bu		I <sub>C</sub> = 1.0mA, V <sub>CE</sub> = 5V	225	00	175	and treatment	100	-	
Ou	$T_A = -55^{\circ}C$	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 5V	75		50	and floor	30		
V <sub>BE(on)</sub>	Emitter-Base On Voltage			0.7	Montaglitaca	0.7	v i	0.7	V
VCE(sat)	Collector Saturation Voltage	I <sub>C</sub> = 1.0mA, I <sub>B</sub> = 0.1mA		0.35	emission be	0.35		0.35	
Ісво	Collector Cutoff Current	I <sub>E</sub> = 0, V <sub>CB</sub> = 45V, 30V*		0.1	NAME OF STREET	0.1	Tradesign to the	0.1*	nA
T <sub>A</sub> = 150°C	of employee with home allow 6 T become	S sever	0.1	ettou sort	0.1	Partition of	0.1*	μΑ	
IEBO	Emitter Cutoff Current	IC = 0, VEB = 5V 00000000 101 13	en as hi	0.1	cibaci s	0.1	o teamo	0.1	nA
Cobo	Output Capacitance (Note 4)	I <sub>E</sub> = 0, V <sub>CB</sub> = 5V, f = 1MHz	JORNALS	0.8	Dist. Sale	0.8	a abson	0.8	pF

#### 2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880



#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER			2N4044 2N4878		2N4100 2N4879		2N4045 2N4880	
	OGRAPHY	CHIP TOP	MIN	MAX	MIN	MAX	MIN	MAX	PART
C <sub>te</sub>	Emitter Transition Capacitance (Note 4)	I <sub>C</sub> = 0, V <sub>EB</sub> = 0.5V, f = 1MHz		1		uO <sub>1</sub> w	at Lo	Gpin	pF
C <sub>C1</sub> , C <sub>2</sub>	Collector to Collector Capacitance (Note 4)	V <sub>CC</sub> = 0, f = 1MHz		0.8		0.8	Mate	0.8	pF
IC <sub>1</sub> , C <sub>2</sub>	Collector to Collector Leakage Current	V <sub>CC</sub> = ±100V	t aska	9 590	Mute	5	ily ist	5	рА
VCEO(sust)	Collector to Emitter Sustaining Voltage	I <sub>C</sub> = 1mA, I <sub>B</sub> = 0	60	upreusia.	55	na es	45	1200	V
ft	Current Gain Bandwidth Product (Note 4)	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 10V	200		150		150		MHz
ft	Current Gain Bandwidth Product (Note 4)	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 10V	20		15	Ť	15		MHz
NF	Narrow Band Noise Figure (Note 4)	$I_C = 10\mu A$ , $V_{CE} = 5V$ $f = 1kHz$ $BW = 200Hz$		2	5	3		3	dB
BV <sub>CBO</sub>	Collector Base Breakdown Voltage	$I_C = 10\mu A, I_E = 0$	60		55	7	45		V
BVEBO	Emitter Base Breakdown Voltage	$I_E = 10\mu A, I_C = 0$	7		7		7		V

#### MATCHING CHARACTERISTICS (25°C unless otherwise noted)

hFE1/hFE2	DC Current Gain Ratio (Note 3)	$I_C = 10\mu A$ to 1mA, $V_{CE} = 5V$		0.9	1 8	0.85	1	0.8	1	
IV <sub>BE1</sub> - V <sub>BE2</sub> I	Base Emitter Voltage Differential	$I_{C} = 10 \mu A$ , $V_{CE} = 5 V$			3		5		5	mV
I <sub>B1</sub> - I <sub>B2</sub>	Base Current Differential	$I_{C} = 10\mu A$ , $V_{CE} = 5V$			5	MTAI	10	HMI I	25	nA
∆(V <sub>BE1</sub> - V <sub>BE2</sub> ) /△T	Base Emitter Voltage Differential Change with Temperature	I <sub>C</sub> = 10μA, V <sub>CF</sub> = 5V	- dvi	ISIO NAOAN		WAF	- 5	TO-7	10	μV/°C
∆(  <sub>B1</sub> -   <sub>B2</sub> ) /△T		TA = -55°C to +125°C		101 MS	0.3	DO PARTS	0.5	2NAB	1 00	nA/°C

#### SMALL SIGNAL CHARACTERISTICS COMMENTS SERVING STATEMENT OF STATEMENT O

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	UNIT
hlb	Input Resistance		28	Ω
h <sub>rb</sub>	Voltage Feedback Ratio	I <sub>C</sub> = 1mA, V <sub>CB</sub> = 5V (Note 4)	43	x 10 <sup>-3</sup>
h <sub>fe</sub>	Small Signal Current Gain	V6 = 20V Aug) = 03	250	24
hob	Output Conductance	10 = 1.00pt, Veg = 5V	60	μS
h <sub>le</sub>	Input Resistance	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V (Note 4)	9.6	kΩ
h <sub>re</sub>	Voltage Feedback Ratio	6	42	x 10 <sup>-3</sup>
h <sub>oe</sub>	Output Conductance	Ami. 0 = gi Am0.1 = 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	12	μS

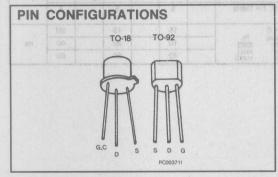
- The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed 10μA.
   The lowest of two h<sub>FE</sub> readings is taken as h<sub>FE1</sub> for purposes of this ratio.
   For design reference only, not 100% tested.

### CITTUD IT LITTUDU JAN, JTXV, JANTX\* N-Channel JFET

Switch

#### **FEATURES**

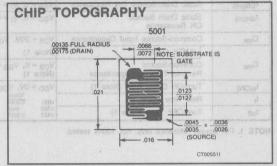
- Low rps(on)
- ID(OFF) < 100pA (JAN TX Types)
  Fast Switching



#### **ORDERING INFORMATION\***

TO-92	TO-18†	WAFER	DICE		
ITE 4091	2N4091	2N4091/W	2N4091/D		
ITE 4092	2N4092	2N4092/W	2N4092/D		
ITE 4093	2N4093	2N4093/W	2N4093/D		

tadd JANTX to these part numbers if JANTX processing is desired. \*When ordering wafer/dice refer to Section 10, page 10-1.



#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise r Gate-Source or Gate-Drain Vo Gate Current	ltage	10m/
Storage Temperature Range Operating Temperature Range Lead Temperature (Soldering,	55°C	to +200°0
	10-18	10-92
Power Dissipation  Derate above 25°C		360mW 3.3mW/°C
Plastic Storage	55°C -55°C	to +150°0

SYMBOL	PARAMETER	TES	TEST CONDITIONS 2N/ITE 4091		000000000000000000000000000000000000000	2N/ITE 4092		2N/ITE 4093		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
BVGSS	Gate-Source Breakdown Voltage		V <sub>DS</sub> = 0	-40		-40		-40		٧
	Drain Reverse Current				200		200		200	pA
IDGO	(Not JANTX Specified) T <sub>A</sub> = 150°C	$V_{DG} = 20V$	$I_S = 0$		400		400	N. C.	400	nA
	Gate Reverse Current				-100		-100		-100	pA
IGSS	(JANTX, ITE devices only) TA = 150°C	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0			-200		-200		-200	nA
	JANTX	V <sub>DS</sub> = 20V	$V_{GS} = -12V(4091)$		100		100		100	pA
I <sub>D(OFF)</sub>	JAN, JTXV; T <sub>A</sub> = 25°C		$V_{GS} = -8V(4092)$ $V_{GS} = -6V(4093)$		200		200		200	
	Drain Cutoff Current JANTX				200		200		200	
	JAN, JTXV, T <sub>A</sub> = 150°C				400		400		400	nA
VP	Gate-Source Pinch-Off Voltage	V <sub>DS</sub> = 20V,	I <sub>D</sub> = 1nA	-5	-10	-2	-7	-1	-5	٧
I <sub>DSS</sub>	Drain Current at Zero Gate Voltage	V <sub>DS</sub> = 20V, Pulse Test	V <sub>GS</sub> = 0, Duraton = 2ms	30		15		8		mA
			I <sub>D</sub> = 2.5mA					(8)	0.2	
V <sub>DS(ON)</sub>	Drain-Source ON Voltage	V <sub>GS</sub> = 0	I <sub>D</sub> = 4mA				0.2			V
			I <sub>D</sub> = 6.6mA		0.2					

#### ITE4091-ITE4093 2N4091-2N4093 JAN, JTXV, JANTX\*



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	PARAMETER	TEST CONDITIONS		ITE 191	2N/ITE 4092		2N/ITE 4093		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	8280
rDS(on)	Static Drain-Source ON Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 1mA		30		50	Winds.	80	
rds(on)	Static Drain Source ON Resistance	$V_{GS} = 0$ , $I_D = 0$ , $f = 1kHz$		30		50	100	80	Ω
Ciss	Common-Source Input Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0, f = 1MHz		16	TXT	116	Acce	16	losa!
	JANTX Only	(Note 1)		5		5	gnid	5	pF
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	V <sub>DS</sub> = 0, V <sub>GS</sub> = -20V, f = 1MHz (Note 1)	1	5	MOF	5	ion	5	PIN
t <sub>d</sub> (ON)	Turn-ON Delay Time (Note 1)	V <sub>DD</sub> = 3V, V <sub>GD(ON)</sub> = 0		15		15		20	1
t <sub>r</sub>	Rise Time (Note 1)	ID(on)   VGS(off)   R1   4091   6.6mA   -12V   42512	1	10		20		40	ns
toff	Turn-OFF Time (Note 1)	4092 4mA -8V 700Ω 4093 2.5mA -6V 1120Ω		40		60		80	

NOTE 1. For design reference only, not 100% tested.

#### ABSOLUTE MAXIMUM RATINGS

Power Disappation 1.6W 260mW/°C 3.3mW/°C 3.5mW/°C

Storage -55°C to +150°C
Operating -55°C to +135°C

TO-92 TO-181 WAFER DICE

TO-92 TO-181 SNAO91/W SNAO91/D

ITE A092 SNAO92 SNAO92/W SNAO92/D

ITE 4093 SNAO93 SNAO93/W SNAO93/D

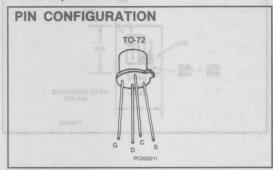
THU	\MS 00	331 92				т соирітюна			
		MAM	16135	KAM	KAM BIM				
								Gate-Source Brackflown Vollage	
				400			V00 = 20V	(Not JANTX Specified) TA = 150°C	
						0 = agV A	Vgs = -20V		
				00f		(1804) VSt - # 90V			
				200		Vgs = -8V(4082) Vgs = -6V(4083)		JAM, JTXM, TA = 25°C.	
								JAN JIXV. IA = 190°C	
						Ani = gi			
							Vos = 20V, Pulse Test		
							0=20V	Drain-Source ON-Voltage	

## 2N4117-19, 2N4117A-19A N-Channel JFET

General Purpose Amplifier Switch Switches Amplifier Switch Switches Amplifier Switches Switch

#### **FEATURES**

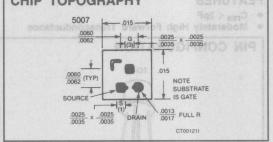
- Low Leakage
- Low Capacitance



ORD	EDIN	0	INIC	ODRA	ATI	ONI*
Unu	CDIN	CI.		Univi	29 1 1	OIA

TO-72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	Pap=	soneR so
2N4118	2N4118/W	2N4118/D
2N4118A		, grimesiaud)
2N4119	2N4119/W	2N4119/D
2N4119A	_	_

CHIP TOPOGRAPHY 5007



#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage40\	1
Gate Current 50mA	1
Storage Temperature Range65°C to +200°C	3
Operating Temperature Range55°C to +175°C	0
Lead Temperature (Soldering, 10sec)+300°C	5
Power Dissipation	V
Derate above 25°C2.0mW/°C	5

\*When ordering wafer/dice refer to Section 10, page 10-1.

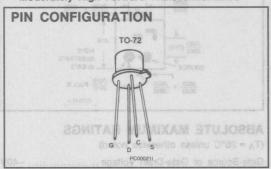
#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

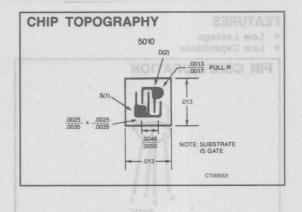
SYMBOL	PARAMETER	TEST CONDITIONS	2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		UNIT
	66- 06- 08-	O # gry Au	MIN	MAX	MIN	MAX	MIN	MAX	
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A$ , $V_{DS} = 0$	-40		-40	DA HOND	-40	COURSE)	No.
V 8-	Gate Reverse Current A devices	(1554MS) AUOUS = QI   VEI (1554MS) AUOUS = QI   VEI (1554MS) AUOUS = QI	n priý	-10 -1		-10 -1	V essed	-10 -1	pA
IGSS	$T_A = +100$ °C A devices	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0	r = adV	-25 -2.5	afold) :	-25 -2.5	tion Drai	-25 -2.5	nA
VGS(off)	Gate-Source Pinch-Off Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA	-0.6	-1.8	-1	-3	-2	-6	V
DSS	Drain Current at Zero Gate Voltage (Note 1)	V <sub>DS</sub> = 10V V <sub>GS</sub> = 0	0.02	0.09	0.08	0.24	0.20	0.60	mA
9fs OF	Common-Source Forward Transconductance (Note 1)	V <sub>DS</sub> = 10V   0 = 20V VBI	70	210	80	250	100	330	200
9fs 3	Common-Source Forward Transconductance (Note 2)	V <sub>GS</sub> = 0, f = 30MHz	60		70	tota 2)	90	Capac	μs
9os S	Common-Source Output Conductance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0, f = 1kHz		3	Note 2)	5	er Capac	10	201
Ciss	Common-Source Input Capacitance (Note 2)	$V_{DS} = 10V, V_{GS} = 0,$ f = 1MHz	bokra	- 30r	is. Only, that	3	test du tesign re	3 5	iores:
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0, f = 1MHz		1.5		1.5		1.5	pF

NOTES: 1. Pulse test: Pulse duration of 2ms used during test.

#### **FEATURES**

- Crss < 2pF
- Moderately High Forward Transconductance





#### ORDERING INFORMATION\*

TO-72	WAFER	DICE
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	30V
Gate Current	10mA
Storage Temperature Range65°C to	+200°C
Operating Temperature Range55°C to	
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

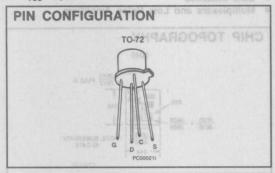
								2N4221		2N4222		
SYMBOL	PARAMETER	(beton TE	(beton TEST CONDITIONS (88)			MAX	MIN	MAX	MIN	MAX	UNI	
	2N4116 2N4119	NP.	DIAS.	244			-0.1		-0.1		-0.1	nA
lgss	Gate Reverse Current	150°C	$V_{GS} = -15V$	$V_{GS} = -15V$ , $V_{DS} = 0$ $G = -10\mu A$ , $V_{DS} = 0$				BMAR	0.40.1		-0.1	μА
BVGSS	Gate-Source Breakdown Voltage	e was	$I_G = -10\mu A$					-30		-30	4	V
VGS(off)	Gate-Source Cutoff Voltage	-	V <sub>DS</sub> = 15V, I <sub>I</sub>	-	-4		-6	-0.4	-8	- V/C		
V <sub>G</sub> S	Gate-Source Voltage	01-	V <sub>DS</sub> = 15V	I <sub>D</sub> = 50 $\mu$ I <sub>D</sub> = 200 I <sub>D</sub> = 500	-0.5	-2.5	-1 Inem	-5	-2	-6	V	
IDSS	Saturation Drain Current (Note	1) ===	V <sub>DS</sub> = 15V, V	GS = 0	A68 S6A	0.5	3	2	6	5	15	mA
9fs	Common-Source Forward Transconductance (Note 1)	8.5	88-	Ant wa	f = 1kHz	1000	4000	2000	5000	2500	6000	Lane W
lyfsl	Common-Source Forward Transadmittance (Note 2)	80.0	50.0		f = 100MHz	750	9/)	750	in his	750	g ·	μs
9os	Common-Source Output Conductance (Note 1)	210	V <sub>DS</sub> = 15V,	V <sub>GS</sub> = 0	f = 1kHz		10	onswio?	20	nemmo	40	215
Ciss	Common-Source Input Capacitance (Note 2)		09	SMMO	Vgg = 0, 1 = 1		6	Parvino -	906.08	noning	6	ati
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)	8			f = 1MHz		2		2	nemme	2	pF

NOTES: 1. Pulse test duration 2m

#### 2N4223, 2N4224 N-Channel JFET High Frequency Amplifier

#### **FEATURES**

- NF = 3dB Typical at 200MHz aggregation lavel well as
- Crss < 2pF

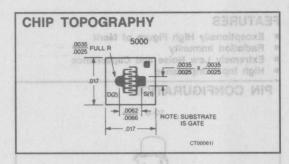


#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N4223	2N4223/W	2N4223/D
2N4224	2N4224/W	2N4224/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## 1 NITERS IL



#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage30V
Gate Current
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +175°C
Lead Temperature (Soldering, 10sec)+300°C
Lead Temperature (Soldering, 10sec) +300°C Power Dissipation 300mW
Derate above 25°C2.0mW/°C
Branch and the state of the sta

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

AM STULIOSBA

	no.	PARAMETER TEST CONDITIONS				2N4	223	2N4224		UNIT
SYM	BUL	PARAMETER	IES	MIN	MAX	MIN	MAX	UNIT		
	Cots Barrers Correct		V 00V V				-0.25		-0.5	nA
IGSS		Gate Reverse Current T <sub>A</sub> = +150°C	$V_{GS} = -20V, V_{DS} = 0$				-0.25		-0.5	μΑ
BVGSS	3	Gate-Source Breakdown Voltage	$I_{G} = -10\mu A$ , $V_{DS} = 0$			-30	MACE	-30	BICAL	D3.
VGS(of	ff)	Gate-Source Cutoff Voltage	2M4636	V/== = 15\/		-0.1	-8	-0.1	-8	V
Vgs	XAM	Gate-Source Voltage	V <sub>DS</sub> = 15V		(2N4223) (2N4224)	-1.0	-7.0	-1.0	-7.5	овыч
IDSS	1.0-	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0			3	18	2	20	mA
9fs	10-	Common-Source Forward Transconductance (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		f = 1kHz	3000	7000	2000	7500	μs
Ciss	3-	Common-Source Input Capacitance (Output Shorted)	V <sub>DS</sub> = 15V, V <sub>G</sub>	S = 0	kgt a + gl ,Våt =	eaV	en16	Jug sous	6	ES(nth)
Crss	(-10)	Common-Source Reverse Transfer Capacitance	(Note 2)		f = 1MHz	904	2 1/15	nuO flotui	2	pF
y <sub>fs</sub>	0000	Common-Source Forward Transadmittance	0081 009		UP BBY WEI	2700	Porward	1700	Commo	
giss .	0.0	Common-Source Input Conductance (Output Shorted)	V <sub>DS</sub> = 15V, V <sub>G</sub>	c = 0	15V, Vas = 0	soy —	800	вольювения	800	μS
9oss	008	Common-Source Output Conductance (Input Shorted)	(Note 2)	5	f = 200MHz	a Vos	200	parios ON	200	(00)3
Gps		Small Signal Power Gain				10	ment	ершо8-п	ummoD.	-
NF		Noise Figure (Note 2)	$V_{DS} = 15V, V_{G}$ $R_{gen} = 1k\Omega$	is = 0,	4 16V. Ves = 6	eaV -	5	anuce-a	Соста	dB

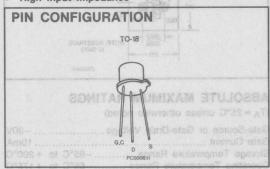
NOTES: 1. Pulse test, duration 2ms.

#### 2N4338-2N4341 N-Channel JFET

#### Low Noise Amplifier

#### **FEATURES**

- Exceptionally High Figure of Merit
- Radiation Immunity
- Extremely Low Noise and Capacitance
- High Input Impedance



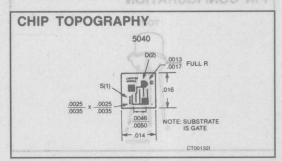
#### ORDERING INFORMATION\*

TO-18	WAFER	DICE
2N4338	2N4338/W	2N4338/D
2N4339	2N4339/W	2N4339/D
2N4340	2N4340/W	2N4340/D
2N4341	2N4341/W	2N4341/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **APPLICATIONS**

- Low-level Choppers Book to Book T She = 488 e
- **Data Switches**
- Multiplexers and Low Noise Amplifiers



#### ABSOLUTE MAXIMUM RATINGS

ADOOLO IL MANAGONI INTINIO	
(T <sub>A</sub> = 25°C unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	50mA
Operating Temperature Range55°C to Lead Temperature (Soldering, 10sec)	+175°C
Power Dissipation	

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

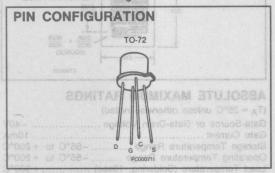
V	8- 1:0- 8- 1:0- (8526/85) And 0-di		2N4338		2N4339		2N4340		2N4341		V03(0	
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Am	1 18   2   20	Carlo	0+9	aV /Va	-0.1	(4)	-0.1	memuO	-0.1	паплад	-0.1	nA
IGSS	Gate Reverse Current TA = 150°C	$V_{GS} = -30V$ , $V_{I}$	DS = 0	eW VE	-0.1		-0.1	TEWNO!	-0.1	Commo	-0.1	μΑ
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A$ , $V_{DS} = 0$	-	-50		-50	(1	-50	TOOK PLANT	-50	-	.,
VGS(off)	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_{D} = 0.1 \mu A$		-0.3	" til	-0.6	-1.8	-1	-3	-2	-6	V
ID(off)	Drain Cutoff Current	V <sub>DS</sub> =15V, SHM = 1 V <sub>GS</sub> = ( )			0.05		0.05	Ravers	0.05	Commo	0.07	nA (V)
IDSS	Saturation Drain Current	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA
9fs	Common-Source Forward Transconductance	V 45V V		600	1800	800	2400	1300	3000	2000	4000	1 year
9os -	Common-Source Output Conductance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	f = 1kHz	sV.Ve	5		15	utput Sh	30	Conduct	60	μs
rDS(on)	Drain-Source ON Resistance	V <sub>DS</sub> = 0, I <sub>DS</sub> = 0		- 0	2500		1700	pur Sno	1500	Ognduc	800	ohm
Ciss	Common-Source Input Capacitance				7		7	NOC CAR	7	S Rem3	7	999
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0 (Note 1)	f = 1MHz	Oals	3		3	(% 600 modernia	3	T SECUL	3	pF
NF	Noise Figure (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0 R <sub>gen</sub> = 1meg, BW = 200Hz	f = 1kHz		1	esa droc	1 ton	tria con	prefes n	piseb no	1	dB

CHIP TOPOGRAPHY

N-Channel JFET Switch

#### **FEATURES**

- Low ON Resistance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage



#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N4351	2N4351/W	2N4351/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY .0025 x .0029 .016 NOTE: SUBSTRATE CT00141I

#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted) Drain-Source Voltage or Drain-Body Voltage ....... 25V Peak Gate-Source Voltage (Note 1) .....±125V Drain Current......100mA Storage Temperature Range ..... -65°C to +200°C Operating Temperature Range ..... -55°C to +150°C Lead Temperature (Soldering, 10sec) .....+300°C Power Dissipation .......375mW Derate above 25°C......3mW/°C

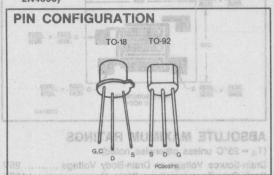
#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

SYMBOL	PARAMETER (beton e	TEST CONDITIONS	MIN	MAX	UNIT
BVDSS	Drain-Source Breakdown Voltage	$I_D = 10 \mu A, V_{GS} = 0$	25		V
IGSS RAPE	Gate Leakage Current	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0	PART AND SHO	10	pA
IDSS	Zero-Gate-Voltage Drain Current	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0	AARAG	10 10	nA
V <sub>GS(th)</sub>	Gate-Source Threshold Voltage	$V_{DS} = 10V, I_{D} = 10\mu A$	1	5	V
ID(on)	'ON' Drain Current	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	3		mA
V <sub>DS(on)</sub>	Drain-Source "ON" Voltage	I <sub>D</sub> = 2mA, V <sub>GS</sub> = 10V		1	V
rDS(on)	Drain-Source Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0, f = 1kHz	Source Breakd	300	ohms
lyfsl	Forward Transfer Admittance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 2mA, f = 1kHz	1000		μs
Crss 008	Reverse Transfer Capacitance (Note 2)	V <sub>DS</sub> = 0, V <sub>GS</sub> = 0, f = 1MHz	memory Horaco	1.3	(tho)(II
Ciss	Input Capacitance (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0, f = 1MHz	Source Rorway	5.0	pF
C <sub>d(sub)</sub>	Drain-Substrate Capacitance (Note 2)	V <sub>D(SUB)</sub> = 10V, f = 1MHz	Source Caroli	5.0	VCS(off)
td(on) 08 a	Turn-On Delay (Note 2)	(an) Vps = 20V, Vps = 0	otion Drain Cox 1)	45	580)
t <sub>r</sub>	Rise Time (Note 2)	Yan John College College	Source ON Vo	65 merQ	ns
td(off) oor	Turn-Off Delay (Note 2)		Down-80 mag	60	(no)8(01)
t <sub>f</sub> 001	Fall Time (Note 2)	U + Cl O W SOV ]	OUTPUT TO SAMPLING OSCILLOSCOPE	100	(ds(cn)

NOTES: 1. Device must not be tested at ±125V more than once or longer than 300ms.

#### **FEATURES**

- rds(on) < 300 Ohms (2N4391)
- ID(OFF) < 100pA
- Switches ±10VAC With ±15V Supplies (2N4392, 2N4393)



#### **ORDERING INFORMATION\***

TO-92	TO-18	WAFER	DICE
ITE 4391	2N4391	2N4391/W	2N4391/D
ITE 4392	2N4392	2N4392/W	2N4392/D
ITE 4393	2N4393	2N4393/W	2N4393/D

#### CHIP TOPOGRAPHY 5001 .00135 FULL RADIUS -0068 .00175 (DRAIN) NOTE: SUBSTRATE IS GATE. bfortesurf wo.J . .0123 .021 .0025 x .0029 (SOURCE) .016 CT006601

#### ABSOLUTE MAXIMUM RATINGS

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage40V
Gate Current
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +200°C
Lead Temperature (Soldering, 10sec)+300°C
TO T

	"MOITAMR	TO-18	TO-92
Power Dissipation Derate above 25°C		10mW/°C	360mW 3.3mW/°C
Plastic Plastic			ninshte, ast/IW

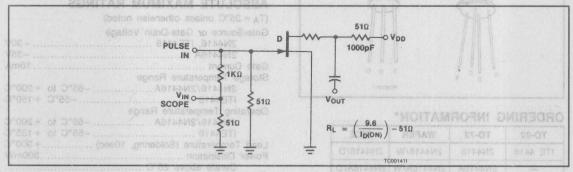
-55°C to +150°C Storage..... 

Aq 0				91	43	92	43	93	(GSS)
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNI
Am	E	V01 = anV_V07 = anV	1	- 100	asoCF 'b	- 100		- 100	pA
IGSS	Gate Reverse Current T <sub>A</sub> = 150°C	$V_{GS} = -20V$ , $V_{DS} = 0$	ttove 13	- 200	in-Sou	- 200		- 200	nA
BVGSS	Gate-Source Breakdown Voltage	$I_G = -1\mu A$ , $V_{DS} = 0$	-40	seFl es	-40	mil Em	-40	100	V
an	= 1842 1000	$V_{GS} = -5V (4393)$	thembA.	100	E brusier	100		100	pA
ID(off)	Drain Cutoff Current  TA = 150°C	$V_{DS} = 20V   V_{GS} = -7V (4392)   V_{GS} = -12V (4391)$	Capac	200	S ex	200		200	nA
V <sub>GS(f)</sub>	Gate-Source Forward Voltage	IG = 1mA, V <sub>DS</sub> = 0	etoVI)	1	neO to	n 1		1	Cina
VGS(off) 0.	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	-4	-10	-2	-5	-0.5	-3	V
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	50	150	25	75	5	30	mA
V <sub>DS(on)</sub>	Drain-Source ON Voltage	V <sub>GS</sub> = 0   I <sub>D</sub> = 3mA (4393)   I <sub>D</sub> = 6mA (4392)   I <sub>D</sub> = 12mA (4391)	(S	0.4	amiT a	0.4		0.4	V
rDS(on)	Static Drain-Source ON Resistance	VGS = 0, ID = 1mA	(Z 810)	30	1 1757-13	60		100	Holp!
rds(on)	Drain-Source ON Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 0   f = 1kHz		30		60	I ROPE OF THE PARTY OF	100	Ω

SYMBOL	PARAMETER	TEST CONDITIONS			MiN	MAX	MIN	MAX	MIN	MAX	UNI
Ciss	Common-Source Input Capacitance (Note 2)	V <sub>DS</sub> = 20V,	V <sub>GS</sub> = 0			14		14	esic	14	1 9
	programma market may make		$V_{GS} = -5V$			SOME	aloeg	O NO	sunar	3.5	2 9
Crss	Common-Source Reverse Transfer Capacitance (Note 2)	V <sub>DS</sub> = 0	$V_{GS} = -7V$	f = 1MHz		9	2/18710	3.5	7335973	O WE	pF
			V <sub>GS</sub> = -12V			3.5	NAME OF STREET	PURTING	CHARLE	t ngi	4
t <sub>d</sub>	Turn-ON Delay Time (Note 2)	$V_{DD} = 10V$	V <sub>GS(on)</sub> = 0			15		15	10-19/0	15	
tr	Rise Time (Note 2)		ID(on)	VGS(off)		5	Same of	5	Caras	5	55/05
toff	Turn-OFF Delay Time (Note 2)	4391	12mA	- 12V		20	E 2 2 2 2 2	35	1245	50	ns
tf	Fall Time (Note 2)	4392 4393	6	-7 -5	401	15		20		30	

NOTES: 1. Pulse test required, pulse width = 300 µs, duty cycle ≤ 3%

2. For design reference only, not 100% tested.



ELECTRICAL CHARACTERISTICS (25°C unless officialise noted)

Common-Source Reverse Transfer Capacitainos (More 1)	V00 = 15V, V05 = 0			

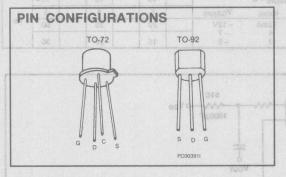
## N-Channel JFET High Frequency Amplifier



CT000611

#### **FEATURES**

- Low Noise
- Low Feedback Capacitance
- Low Output Capacitance
- High Transconductance
- High Power Gain



#### **ORDERING INFORMATION\***

TO-92	TO-72	WAFER	DICE
ITE 4416	2N4416	2N4416/W	2N4416/D
ALL TRANSPORTED AND SECURE OF	2N4416A	2N4416A/W	2N4416A/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY 0035 FULL R 5000 0035 - 0035 - 0035 - 0035 - 0025

#### ABSOLUTE MAXIMUM BATINGS

ABSOLUTE MAXIMUM HATINGS	and disconnected the
(T <sub>A</sub> = 25°C unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	
2N4416, ITE4416	30V
2N4416A	35V
Gate Current	10mA
Storage Temperature Range	
2N4416/2N4416A65°C to	
ITE441655°C	+150°C
Operating Temperature Range	
2N4416/2N4416A65°C to	+200°C
ITE441655°C to	+135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	
Derate above 25°C	
2N4416/2N4416A1	.7mW/°C
ITE44162	7mW/°C

SYMBOL	PARAMETE	R	TEST CONDITIONS			MAX	UNIT
V <sub>GS(f)</sub>	Gate-Source Forward Voltage		I <sub>G</sub> = 1mA, V <sub>DS</sub> = 0			1	٧
						-0.1	nA
IGSS	Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = -20V, V_{DS} = 0$		1000	-0.1	μΑ
		2N4416/ITE4416			- 30		
BVGSS	Gate-Source Breakdown Voltage	2N4416A	$I_{G} = -1\mu A, V_{DS} = 0$		- 35		V
		2N4416/ITE4416				-6	
VGS(off)	Gate-Source Cutoff Voltage	2N4416A	$V_{DS} = 15V, I_{D} = 1nA$		- 2.5	-6	
IDSS	Drain Current at Zero Gate Volta	ge			5	15	mA
9fs	Common-Source Forward Transco	onductance		f = 1kHz	4500	7500	μS
9os .	Common-Source Output Conducts	ance				50	μs
C <sub>rss</sub>	Common-Source Reverse Transfe (Note 1)	er Capacitance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0			0.8	pF
C <sub>iss</sub>	Common-Source Input Capacitano	urce Input Capacitance (Note 1)		f = 1MHz		4	
Coss	Common-Source Output Capacita	nce (Note 1)		T = TMHZ		2	pF

## ITE4416, 2N4416/A

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

OVERDOL			10	OMHz	40	死, 夏岛		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
giss	Common-Source Input Conductance			100		1000	PENESS	
biss	Common-Source Input Susceptance			2500		10,000		
9oss	Common-Source Output Conductance	N. 914(7)		75		100	ITA-	
boss	Common-Source Output Susceptance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0 (Note 1)		1000		4000	μS	
9fs	Common-Source Forward Transconductance		Supplies	Vich ±15Y	4000	Vort sed		
Gps	Common-Source Power Gain	V <sub>DS</sub> = 15V, I <sub>D</sub> = 5mA (Note 1)	18		10	BENNY AND		
NF	Noise Figure (Note 1)	$V_{DS} = 15V$ , $I_D = 5mA$ , $R_G = 1k\Omega$		2	PERSON A 400	initians	dB	

NOTE 1: For design reference only, not 100% tested.

A.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range -- 65°C to + 200°C
Cooraing Temperature Range -- 55°C to + 200°C

Detate above 25°C......10mW/°C

овревине инговиатион

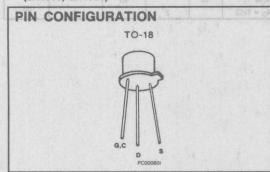
	WAFER	
		†08854S
2N48577D		
	ZNAGSS/W	

The species of the same and the same species and

	PARAMETER	TEST COMPITIONS		501941		XASE	
and the second second second	Gata-Sauce						
	Breakdown Voltage	16 = -1µA, Voe = 0					
	Drain CutoW Digrant						
	Cate-Source Cutoff Voltage	And 0 = of , Vat = 2 oV					
		VDS=16V, Vd3=G					
(no)86 <sup>1</sup> /							
	Chain-Sounce Old Resistance						

#### **FEATURES**

- Low rps(on)
- ID(off) < 250pA
- Switches ±10V Signals With ±15V Supplies (2N4858, 2N4861)



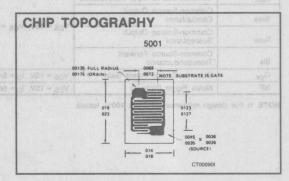
#### **ORDERING INFORMATION\***

TO-18	WAFER	DICE
2N4856†	2N4856/W	2N4856/D
2N4857†	2N4857/W	2N4857/D
2N4858†	2N4858/W	2N4858/D
2N4859	2N4859/W	2N4859/D
2N4860	2N4860/W	2N4860/D
2N4861	2N4861/W	2N4861/D

†add JAN, JTX, JTXV, to basic part number to specify these devices.

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

OVILIDOI	242445		7507 00111	NITIONIO	2N48	56,59	2N48	57,60	2N4858,61		
SYMBOL	PARAMETER		TEST CONI	DITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Gate-Source	2N4856-58			-40		-40	1	- 40		
BVGSS	Breakdown Voltage	2N4859-61	$I_G = -1\mu A$ , $V_{DS} = 0$		-30		- 30		- 30		V
			$V_{GS} = -20V, V_{DS} = 0$			- 250		- 250		- 250	pA
IGSS	Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = -15V, V_{DS} = 0$			- 500		- 500		- 500	nA
	BEET BEET BEET BEET					250		250		250	pA
ID(off)	Drain Cutoff Current	T <sub>A</sub> = 150°C	V <sub>DS</sub> = 15V, V <sub>GS</sub> = -10V			500		500		500	nA
VGS(off)	Gate-Source Cutoff Voltage		$V_{DS} = 15V$ , $I_{D} = 0.5nA$		-4	-10	-2	-6	- 0.8	-4	V
IDSS	Saturation Drain Current (Note 1)		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		50		20	100	8	80	mA
V <sub>DS(on)</sub>	Drain-Source ON Voltage		V <sub>GS</sub> = 0, I <sub>D</sub> = ( )			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)
rds(on)	Drain-Source ON Resistance		$V_{GS} = 0, I_{D} = 0$	f = 1kHz		25	01111	40		60	ohm



#### **ABSOLUTE MAXIMUM RATINGS**

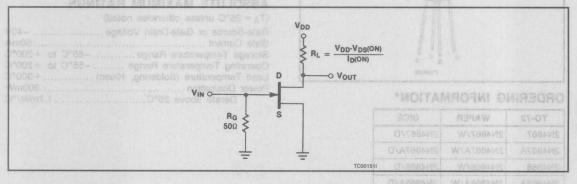
(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage
2N4856–5840V
2N4859-6130V
Gate Current50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +200°C
Led Temperature (Soldering, 10sec)+300°C
Power Dissipation
Derate above 25°C

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

ONAOI		EC ONAO		2N48	56,59		57,60			
SYMBOL	PARAMETER OF OTTO	TEST CONI	DITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Ciss	Common-Source Input Capacitance				18		18	saka	18	3 0
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	$V_{DS} = 0$ , $V_{GS} = -10V$ (Note 2)	f = 1MHz	-	8		8	tile	8	pF
td	Turn-ON Delay Time (Note 2)	$V_{DD} = 10V$ , $R_L = 953Ω$ (2N4856,59) $V_{GS(on)} = 0$ 1910Ω (2N4857,60) $V_{GS(off)} = -10V$ , $I_D = 20$ mA (2N4856,91)			6	1 1-21	6	20.00	10	
t <sub>r</sub>	Rise Time (Note 2)				3	T.	4		10	ns
toff	Turn-OFF Time (Note 2)	$V_{GS(off)} = -6V, I_{D} = 10$ $V_{GS(off)} = -4V, I_{D} = 5r$	mA (2N4857,60) nA (2N4858,61)		25	7.	50		100	

NOTES: 1. Pulse test required, pulse width = 100 µs, duty cycle ≤ 10%.

2. For design reference only, not 100% tested.



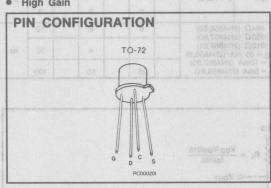
			867 887A					
	XAM	14150		Mint				
								The State of
							Gebe Reverse Current   TA = 190°C	
							Common-Source Forward Transconductance (Note 1)	
					abbit = 1			908
						U+spV,VQS=aqV	Conumon-Source Payarae Transfer Cepacitance (Note 2)	Cres
							Common-Source Input Capacitance (Note 2)	

#### 2N4867/A-2N4869/A N-Channel JFET Low Noise Amplifier



#### **FEATURES**

- Low Noise Voltage
- Low Leakage
- High Gain



#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY NOTE: SUBSTRATE IS GATE DRAIN(2) CT001511

#### ABSOLUTE MAXIMUM RATINGS

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage40V
Gate Current50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +200°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation300mW
Derate above 25°C1.7mW/°C

SYMBOL	PARAMETER	TEST CONDI	TEST CONDITIONS			2N4868 2N4868A		2N4869 2N4869A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
					- 0.25	Nan E	- 0.25		- 0.25	nA
IGSS	Gate Reverse Current T <sub>A</sub> = 150°C	$V_{GS} = -30V, V_{DS} = 0$			- 0.25		- 0.25		- 0.25	μΑ
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A$ , $V_{DS} = 0$		-40		- 40		- 40		
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_{D} = 1\mu A$		-0.7	-2	-1	-3	- 1.8	-5	V
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		0.4	1.2	1	3	2.5	7.5	mA
9fs	Common-Source Forward Transconductance (Note 1)			700	2000	1000	3000	1300	4000	
9os	Common-Source Output Conductance		f = 1kHz		1.5		4		10	μS
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)	$V_{DS} = 20V$ , $V_{GS} = 0$			5		5		5	
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)	f = 1MHz			25		25		25	pF

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	PARAMETE	R	TEST CONDITIONS			2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A	
			FAULISTA	A. 对证明			MIN	MAX	MIN	MAX	AST
ALC: N		ENTERIOR !	C BOTOLIN &	f = 10Hz	Second S	20	olassi.	20	20 20	20	550 0
	Short Circuit Equivalent Input	V <sub>DS</sub> = 10V,	f = 1kHz		10		10	o Hwit	10	nV	
ēn	Noise Voltage		V <sub>GS</sub> = 0	f = 10Hz		10		10	telsa)	10	√Hz
	(Note 2)	A devices	OT SHIP TO	f = 1kHz		5	DITA	5	1914	5	AIR
NF	Spot Noise Figure (No	te 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0 R <sub>gen</sub> = 20K, (2N4867 Series) R <sub>gen</sub> = 5K, (2N4867A Series)	f = 1kHz		1	r-OT	1		1	dB

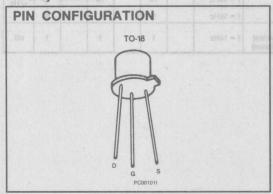
NOTES: 1. Pulse test duration = 2ms.
2. For design reference only, not 100% tested.

DRIDERING INFORMATIONS

KASI											PARAMETER TEST CONDITIONS						
					Cate-Source Breditown Voltag												
				0°687 = 189°0													
					Gata-Source Cutoff Voltage												
			0 = 0, Vas = 0														
			V06 = = 55V V68 = 0														
					Common-Source Reserve Tysin Capacitanos (Note 1)												

#### FEATURES

- Low Insertion Loss
- No Offset or Error Voltages Generated By Closed Switch
- Purely Resistive



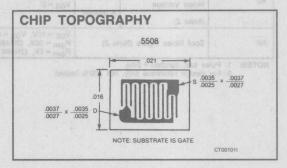
#### **ORDERING INFORMATION\***

TO-18	WAFER	DICE
2N5018	2N5018/W	2N5018/D
2N5019	2N5019/W	2N5019/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **APPLICATIONS**

- Analog Switches
- Commutators
- Choppers



#### **ABSOLUTE MAXIMUM RATINGS**

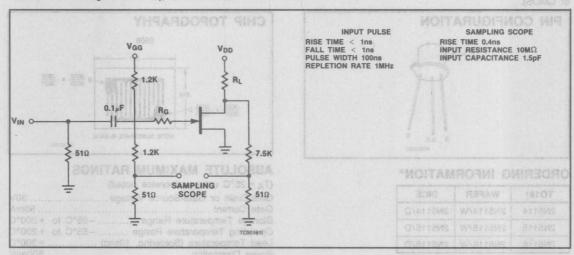
(TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V	1
Gate Current 50mA	
Storage Temperature Range65°C to +200°C	,
Operating Temperature Range55°C to +200°C	,
Lead Temperature (Soldering, 10sec)+300°C	,
Power Dissipation500mW	-
Derate above 25°C3mW/°C	,

average.				2N5	5018	2N5	5019	
SYMBOL	PARAMETER	TEST CONDITIO	NS	MIN	MAX	MIN	MAX	UNIT
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = 1\mu A, V_{DS} = 0$		30		30		V
IGSSR	Gate Reverse Current	V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0			2		2	
THE RESERVE		V <sub>GS</sub> = 12V (2	N5018)		- 10		-10	nA
ID(off)	Drain Cutoff Current T <sub>A</sub> = 150°C	$V_{DS} = -15V$ , $V_{GS} = 7V$ (2N	15019)		-10		-10	μA
Ipgo	Drain Reverse Current	$V_{DG} = -15V$ , $I_{S} = 0$			-2		-2	nA
·bdo	T <sub>A</sub> = 150°C	TDG 107, 15			-3		-3	μΑ
VGS(off)	Gate-Source Cutoff Voltage	$V_{DS} = -15V$ , $I_{D} = -1\mu A$		Market N	10		5	V
IDSS	Saturation Drain Current	$V_{DS} = -20V, V_{GS} = 0$		-10		-5		mA
V <sub>DS(on)</sub>	Drain-Source ON Voltage	$V_{GS} = 0$ , $I_D = -6mA$ (2N5018) $I_D = -3mA$ (2N5019)			-0.5		-0.5	٧
rds(on)	Static Drain-Source ON Resistance	$I_D = -1 \text{mA}, V_{GS} = 0$			75		150	Ω
rds(on)	Drain-Source ON Resistance	I <sub>D</sub> = 0, V <sub>GS</sub> = 0	f = 1kHz		75		150	
Ciss	Common-Source Input Capacitance (Note 1)	$V_{DS} = -15V, V_{GS} = 0$		96.3	45		45	
C <sub>rss</sub>	Common-Source Reserve Transfer Capacitance (Note 1)	V <sub>DS</sub> = 0, V <sub>GS</sub> = 12V (2N5018), V <sub>GS</sub> = 7V (2N5019)	f = 1MHz		10		10	pF

CVMPOI	DADAMETER		TEST CONDITIONS	1	2N5	018	2N5	019	UNIT
SYMBOL	PARAMETER		TEST CONDITIONS	MIN	MAX	MIN	MAX		
td(on)	Turn-ON Delay Time (Note 1)	THE REAL PROPERTY.		NEW THE		15		15	
tr	Rise Time (Note 1)	$V_{DD} = -6$	$V, V_{GS(on)} = 0$			20		75	
	TUMES	EEA	VGS(off) ID(on)	RL I	200	PACIFIC		AHS	HEE
<sup>†</sup> d(off)	Turn-off Delay Time (Note 1)	2N5018	12V -6mA	9100	grida	15	ilrievi	25	ns
tf	Fall Time (Note 1)	2N5019	7V -3mA	1.8kΩ	MA	50	woni i	100	ni est

NOTES: 1. For design reference only, not 100% tested.



SWITCHING CHARACTERISTICS (25°C unless otherwise noted)

JAM TX 2NS116	JAN TX	JAN. TX			PARAMETER
08 1				81	

				2965114		2965114				
	PARAMETER	· · · · · · · · · · · · · · · · · · ·			XAM					
Wass	Gate-Source Dreskdown Volke									
			Ves = 20V. Ves = 0							
	Gate-Source Pinch-Off Vollage						1			

#### 2N5114-2N5116, JAN, JTX, JTXV P-Channel JFET

P-Channel JFET Switch

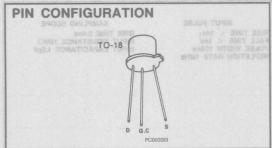


Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and  $\pm 10$ VAC signals can be handled using only + 5V logic (TTL or CMOS).

## **WINTERSIL**

#### **FEATURES**

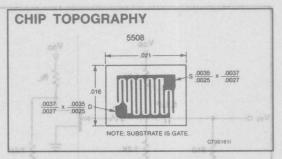
- Low ON Resistance
- ID(off) < 500pA
- Switches directly from TTL Logic



### ORDERING INFORMATION\*

TO18†	WAFER	DICE
2N5114	2N5114/W	2N5114/D
2N5115	2N5115/W	2N5115/D
2N5116	2N5116/W	2N5116/D

\*When ordering wafer/dice refer to Section 10, page 10-1. †add JAN, JTX, JTXV to basic part number to specify these devices.



#### ABSOLUTE MAXIMUM RATINGS

#### SWITCHING CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	UNIT
		MAX	MAX	MAX	MAX	MAX	MAX	
td	Turn-ON Delay Time	6	10	12	6	10	25	
tr	Rise Time (Note 2)	10	20	30	10	20	35	ns
t <sub>off</sub>	Turn-OFF Delay Time (Note 2)	6	8	10	6	8	20	
tf	Fall Time (Note 2)	15	30	50	15	30	60	

SYMBOL				2N5114		2N5115		2N5116		
	PARAME	TEH	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
BVGSS	Gate-Source Breakdown Voltage I <sub>G</sub> = 1μA, V <sub>DS</sub> = 0		$I_{G} = 1\mu A, V_{DS} = 0$	30		30		30		٧
					500		500		500	pA
IGSS	Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = 20V, V_{DS} = 0$		1.0		1.0		1.0	μΑ
			2N5114 = 12V		-500		-500		-500	рА
ID(off)	Drain Cutoff Current	T <sub>A</sub> = 150°C	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 2N5115 = 7V 2N5116 = 5V		-1.0		-1.0		-1.0	μA
Vp	Gate-Source Pinch-Off	Voltage	$V_{DS} = -15V, I_{D} = -1nA$	5	10	3	6	1	4	V

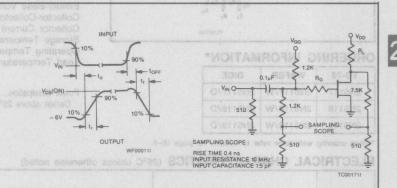
#### 2N5114-2N5116, JAN, JTX, JTXV

### ELECTRICAL CHARACTERISTICS (CONT.)

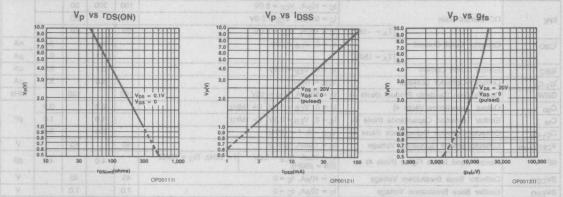
0.44001	PARAMETER         TEST CONDITIONS           Drain Current at Zero Gate Voltage (Note 1)         VGS = 0, VDS = 2N5115 = -15V 2N5116 = -15V		2N	15114 2N5115		5115	2N5116		LIMIT		
SYMBOL			a construction of			MAX	MIN	MAX	MIN	MAX	UNIT
IDSS			V <sub>GS</sub> = 0, V <sub>DS</sub> =	2N5115 = -15V	-30	-90	-15	-60	-5	-25	mA
V <sub>G</sub> S(f)	Forward Gate-Source Voltage		I <sub>G</sub> = -1mA, V <sub>DS</sub> = 0			-1		-1%	Mat	-it b	Goo
V <sub>DS(on)</sub>	Drain-Source ON Voltage	5 oil	V <sub>GS</sub> = 0, I <sub>D</sub> =	2N5114 = -15mA 2N5115 = -7mA 2N5116 = -3mA	Pakis	-1.3	ishi k			-0.6	100000000000000000000000000000000000000
「DS(on)	Static Drain-Source ON Resistance		VGS = 0, ID = -11	mA		75		100		150	and the second second
	Small-Signal Drain-Source	ON .	100			75	OH	100	2114	150	Ω
rds(on)	Resistance	Jan TX only	$V_{GS} = 0$ , $I_{D} = 0$ , $I_{D} = 0$	= 1kHz		75		100		175	
	Common-Source Input					25	1	25		25	
Ciss	Capacitance (Note 2)	Jan TX only	$V_{DS} = -15 \text{ V, V}_{G}$	iS = 0, $f = 1MHz$	800	25		25		27	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (No	ote 2)	V <sub>DS</sub> = 0, V <sub>GS</sub> = f = 1MHz	2N5114 = 12V 2N5115 = 7V 21N5116 = 5V		7	P	87,01		7	pF

NOTES: 1. Pulse test; duration = 2ms.
2. For design reference only, not 100% tested.

	TEST CO	NDITIONS	(I giel
0054 0	2N5114	2N5115	2N5116
V <sub>DD</sub>	-10V	-6V	-6V
VGG	20V	12V	8V
RL	430Ω	910Ω	2ΚΩ
RG	100Ω	220Ω	390Ω
ID(ON)	-15mA	-7mA	-3mA
VIN	-12V	-7V	-5V

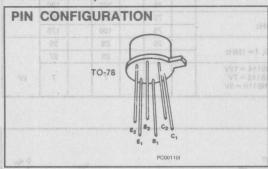


#### TYPICAL PERFORMANCE CHARACTERISTICS



#### FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good hee Match
- Tight VBE Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers



#### **ORDERING INFORMATION\***

TO-78	WAFER	DICE
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### CHIP TOPOGRAPHY

CT001711

#### ABSOLUTE MAXIMUM RATINGS

	ONE SIDE	BOTH SIDES
Power Dissipation	400mW	750mW
Derate above 25°C	2.3mW/°C	4.3mW/°C

SYMBOL	PARAMETER	TEST CONDITIONS	2N5117 2N5118		2N5119		UNIT
		NOT CHARACTERISTICS	MIN	MAX	MIN	MAX	HEVT
		$I_C = 10\mu A$ , $V_{CE} = 5.0V$	100	300	50		
hFE	DC Current Gain	$I_C = 500 \mu A$ , $V_{CE} = 5.0 V$	100	101 av	50		
	$T_A = -55^{\circ}C$	$I_C = 10\mu A$ , $V_{CE} = 5.0V$	30	HILL	20	0.0	
ICBO	Collector Cutoff-Current	I <sub>E</sub> = 0, V <sub>CB</sub> = 30V	-	0.1	-	0.1	nA
	T <sub>A</sub> = 150°C			0.1		0.1	μА
IEBO	Emitter Cutoff Current	I <sub>C</sub> = 0, V <sub>EB</sub> = 5.0V		0.1		0.1	nA
IC1-C2	Collector-Collector Leakage	V <sub>CC</sub> = 100V	17	5.0		5.0	рА
GBW	Current Gain Bandwith Product (Note 4)	$I_{C} = 500\mu A$ , $V_{CE} = 10V$	100		100		MHz
Cob	Output Capacitance (Note 4)	IE = 0, V <sub>CB</sub> = 5.0V, f = 1MHz	7	0.8		0.8	
Cte	Emitter Transition Capacitance (Note 4)	IC = 0, VEB = 0.5V, f = 1MHz		1.0		1.0	pF
CC1-C2	Collector-Collector Capacitance (Note 4)	V <sub>CC</sub> = 0, f = 1MHz		0.8		0.8	
VCEO(sust)	Collector-Emitter Sustaining Voltage	I <sub>C</sub> = 1.0mA, I <sub>B</sub> = 0	45	Hit	45	1 10	V
NF309,001 00	Narrow Band Noise Figure (Note 4)	$I_C = 10 \mu A$ , $V_{CE} = 5.0 V$ $f = 1 kHz$ , $R_G = 10 k\Omega$ $BW = 200 Hz$		4.0	18	4.0	dB
BV <sub>CBO</sub>	Collector Base Breakdown Voltage	$I_C = 10\mu A, I_E = 0$	45		45	11.3	٧
BVEBO	Emitter Base Breakdown Voltage	$I_E = 10\mu A, I_C = 0$	7.0		7.0		V

#### 2N5117-2N5119

#### MATCHING CHARACTERISTICS (25°C unless otherwise noted)

		TEST CONDITIONS		2N5117		2N5118		2N5119		
SYMBOL	PARAMETER			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Eliverniensi	DC Current Gain Ratio	I <sub>C</sub> = 10μA to 500μA, V <sub>CE</sub> = 5V		0.9	1.0					
hFE1/hFE2	(Note 3)	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 5.0V			100	0.85	1.0	0.8	1.0	
	Base-Emitter Voltage	I <sub>C</sub> = 10μA to 500μA, V <sub>CE</sub> = 5V			3.0	annual C	The same		19	mV
V <sub>BE1</sub> -V <sub>BE2</sub>	Differential						5.0		5.0	
I <sub>B1</sub> -I <sub>B2</sub>	Base Current Differential				10.0	110	15	119	40	nA
△(V <sub>BE1</sub> -V <sub>BE2</sub> )/△T	Base Voltage Differential Change with Temperature	$I_{C} = 10\mu A, V_{CE} = 5.0V$	$T_A = -55^{\circ}\text{C to} + 125^{\circ}\text{C}$		3.0		5.0		10	μV/°C
△(I <sub>B1</sub> -I <sub>B2</sub> )/△T	Base-Current Differential Change with Temperature		T <sub>A</sub> = -55°C to + 125°C		0.3		0.5		1.0	nA/°C

NOTES:	1	Por	transistor.

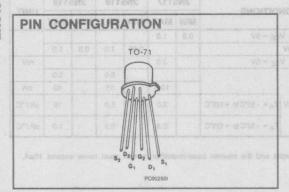
- The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.
   Lower of two h<sub>FE</sub> readings is defined as h<sub>FE1</sub>.
   For design reference only, not 100% tested.

	FY-OT

SYMBOL		TEST CONDI			
				-25	
		Aut003 = cf. V93 = bgV StemiO gnitriegt			

## 2N5196-2N5199 Dual N-Channel JFET General Purpose Amplifier





# CHIP TOPOGRAPHY 6037 023 024 017 017 017 ALL BOND PADS ARE 4 x 4 MIL. CT600701

#### **ORDERING INFORMATION\***

TO-71	WAFER	DICE
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **ABSOLUTE MAXIMUM RATINGS**

(T<sub>A</sub> = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)50V
Gate Current (Note 1)50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C

ONE SIDE BOTH SIDES

Power Dissipation ( $T_A = 85^{\circ}\text{C}$ ) .... 250mW 500mW Derate above 25°C ...... 2.6mW/°C 4.3mW/°C

SYMBOL	PARAMETER	TEST CONDI	TIONS	MIN	MAX	UNIT
lgss	Gate Reverse Current	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0		-25		
	T <sub>A</sub> = 150°C				-50	nA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$		-50		
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA		-0.7	-4	٧
V <sub>G</sub> S	Gate-Source Voltage			-0.2		
lg	Gate Operating Current	$V_{DG} = 20V, I_{D} = 200\mu A$			-15	рА
	T <sub>A</sub> = 125°C				-15	nA
DSS	Saturation Drain Current (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	0.7 7		mA	
9fs	Common-Source Forward Transconductance (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		1000	4000	
9fs	Common-Source Forward Transconductance (Note 2)	$V_{DG} = 20V, I_D = 200\mu A$		700	1600	
9os	Common-Source Output Conductance (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1kHz		50	μs
9os	Common-Source Output Conductance (Note 2)	$V_{DG} = 20V, I_{D} = 200 \mu A$			4	
Ciss	Common-Source Input Capacitance (Note 4)				6	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 4)		f = 1MHz		2	pF
NF	Spot Noise Figure (Note 4)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	$f = 100Hz$ , $R_G = 10M\Omega$		0.5	dB
en	Equivalent Input Noise Voltage (Note 4)		f = 1kHz		20	μηV √Hz

#### 2N5196-2N5199

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

OVERDOL	DADAMETED	00	NOITIONS	2N:	5196	2N!	5197	2N5198		2N	5199	LIMIT
SYMBOL	PARAMETER	TEST CO	NDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
IIG1-IG2	Differential Gate Current	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA	125°C 3H	4508	185(8	so t	0.5	oO) 1	5 1	M S	5 = 6	nA s
I <sub>DSS1</sub> /I <sub>DSS2</sub>	Saturation Drain Current Ratio (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V 0.95		0.95	1 0.9	0.95	1	0.95	150	0.95	dap	wo.J
9fs1/9fs2	Transconductance Ratio (Note 2)		f = 1kHz	0.97	1	0.97	15/	0.95	ARU	0.95	CON	MIS
VGS1-VGS2	Differential Gate-Source Voltage				5		5		10		15	mV
△ V <sub>GS1</sub> =V <sub>GS2</sub>	Gate-Source Differential Voltage	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA	T <sub>A</sub> = 25°C T <sub>B</sub> = 125°C		5		10	17-01	20		40	
ΔΤ	Change with Temperature (Note 3)		$T_A = -55$ °C $T_B = 25$ °C		5		10		20		40	μV/°C
gos1-gos2	Differential Output Conductance		f = 1kHz		1		1		71 -		1	μs

Pulse test required, pulsewidth = 300 μs, duty cycle < 3%.</li>
 Measured at endpoints T<sub>A</sub> and T<sub>B</sub>.
 For design reference only, not 100% tested.

Power Dissipation 200mW
Derate above 25°C .....2.4mW/°C

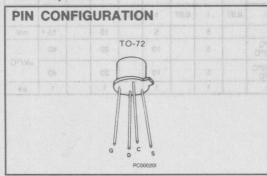
GAZGESIAD S	2N5397
G/aecans	

							8888		
	PARAMETER		поисо теат			XAM		TISSU	
	Gate Revense Current		Ves = -15V, Ves = 0						
	Gara-Source Bresikdown Voltage Voltage C, 19 = -1pA		Vps = 6, 19 + -1ph						
	Gate-Source Outoff Vorlage Vps -		Ant = gl ,V01 = agV						
		0-adV V01 = adV							
200									
1906			Vps = 10V, Vds = 0						

#### mign rrequency Amplitier

#### FEATURES AND MAN MAN MAN MAN MAN MAN

- Gps = 15dB Minimum (Common Gate) at 450MHz
- Low Noise
- Low Capacitance

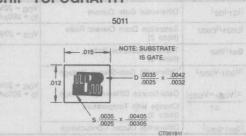


#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
2N5397	2N5397/W	2N5397/D
2N5398	2N5398/W	2N5398/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### CHIP TOPOGRAPHY



#### ABSOLUTE MAXIMUM RATINGS

ADOOLOTE MAXIMOM TATTICO
(T <sub>A</sub> = 25°C unless otherwise noted)
Drain-Gate Voltage
Drain-Source Voltage25V
Continuous Forward Gate Current 10mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation300mW
Derate above 25°C2.4mW/°C

			2N5397		2N!	5398	UNIT	
SYMBOL	PARAMETER	TEST CONDI	TIONS	MIN	MAX	MIN	MAX	nA μA
Igss	Gate Reverse Current	V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0			-0.1		0.1	
1033	$T_A = +150$ °C	*GS 101, 105 0	150°C		-0.1		-0.1	
BVGSS	Gate-Source Breakdown Voltage	$V_{DS} = 0$ , $I_{G} = -1\mu A$		-25		-25		٧
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA		-1.0	-6.0	-1.0	-6.0	
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 10V, V <sub>DS</sub> = 0 10. 30		5	40	mA		
VGS(f)	Gate-Source Forward Voltage	V <sub>DS</sub> = 0, I <sub>G</sub> = 1mA			1		1 V	
	Common-Source Forward	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA		6000	10,000		B 1981	
9fs	Transconductance (Note 1)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0			125	5500	10,000	
DIST. OF	Common-Source Output	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA	f = 1kHz		200			μs
9oss	Conductance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0					400	
	Common-Source Reverse Transfer	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA			1.2			1976
C <sub>rss</sub>	Capacitance (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0				The least of	1.3	
		V <sub>DG</sub> = 10V, I <sub>D</sub> = 10mA	f = 1MHz		5.0		F. (177)	pF
Ciss	Common-Source Input Capacitance (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0					5.5	

OVIMBOL	PARAMETER O TOTAL	MIN TENT COMP	TIONS	ZINO	186	2N0000		UNIT
SYMBOL	PARAMETER	TEST CONDI	TIONS	MIN	MAX	MIN	MAX	UNIT
	Common-Source Input	V <sub>DG</sub> = 10V, I <sub>D</sub> = 10mA			2000	Switch	ineile	e Ex
9iss	Conductance (Note 2)	V <sub>DG</sub> = 10V, V <sub>GS</sub> = 0			ins	TOUR	3000	ol o
	Common-Source Output	V <sub>DG</sub> = 10V, I <sub>D</sub> = 10mA		2/3/65	400	\$ 5 CW \$15	LAPREN.	μs
9oss	Conductance (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0	The state of the	37.0.075	GIR WATER		500	
	Common-Source Forward	V <sub>DG</sub> = 10V, I <sub>D</sub> = 10mA	f = 450MHz	5500	9000			
9fs	Transconductance (Note 1, 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0				5000	10,000	
Gps	Common-Source Power Gain (neutralized)			15				
NF	Common-Source, Spot Noise Figure (neutralized)	V <sub>DG</sub> = 10V, I <sub>D</sub> = 10mA (Note 2)		and the second	3.5			dB

NOTES: 1. Pulse test duration = 2ms

2. For design reference only, not 100% tested.

#### DEDERING INFORMATIONS

WAFER	

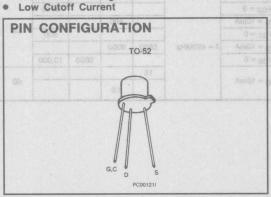
			SMS432				
			MIN		MIDN	insi	
Brish Cutoff Current   TA = 150°C							

#### 2N5432-2N5434 **N-Channel JFET Switch**

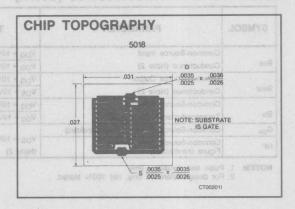


#### **FEATURES**

- Low rds(on)
   Excellent Switching



NAME OF THE REAL PROPERTY.



#### **ORDERING INFORMATION\***

TO-52	WAFER	DICE
2N5432	2N5432/W	2N5432/D
2N5433	2N5433/W	2N5433/D
2N5434	2N5434/W	2N5434/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Source Voltage25V
Gate-Drain Voltage25V
Gate Current100mA
Drain Current400mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation300mW
Derate above 25°C 2.3mW/°C

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

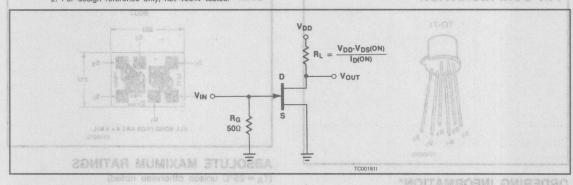
						2N5433		2N5434		
SYMBOL	PARAMETER	TEST COND	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
		PHOTO THE			-200		-200		-200	pA
IGSS	Gate Reverse Current T <sub>A</sub> = 150°C	$V_{GS} = -15V, V_{DS} = 0$		100	-200		-200		-200	nA
BVGSS	Gate Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$		-25		-25		-25		V
			100	200		200		200	pA	
ID(off)	Drain Cutoff Current T <sub>A</sub> = 150°C	$V_{DS} = 5V$ , $V_{GS} = -10V$			200		200		200	nA
V <sub>G</sub> S(off)	Gate-Source Cutoff Voltage	$V_{DS} = 5V$ , $I_D = 3nA$		-4	-10	-3	-9	-1	-4	V
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		150		100		30		mA
rDS(on)	Static Drain-Source ON Resistance			2	5	0=1	7		10	ohm
V <sub>DS(on)</sub>	Drain-Source ON Voltage	$V_{GS} = 0$ , $I_D = 10 \text{mA}$			50		70		100	mV
rds(on)	Drain-Source ON Resistance	$V_{GS} = 0, I_{D} = 0$	f = 1kHz	1	5	100	7		10	ohm
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)				30		30		30	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)	$V_{DS} = 0$ , $V_{GS} = -10V$	f = 1MHz		15		15		15	pF

Dual N-Channel JFET

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL		TOT COMPLIANCE	2N5432		2N5433		2N5434		LINUT
	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>d</sub>	Turn-ON Delay Time (Note 2)	V <sub>DD</sub> = 1.5V,		4		4		4	
tr	Rise Time (Note 2)	VGS(on) = 0,	aulu (	119 His	HEITHO	1014 E	BA FA	1 1	LIBRA
toff	Turn-OFF Delay Time (Note 2)	VGS(off) = -12V	Pants:	6	GIL 02	6	G 12 L 1 L 1	6	ns
tf	Fall Time (Note 2)	I <sub>D(on)</sub> = 10mA	Tod Make	30	nes deserv	30	I break	30	HAVESTARI MATERIAL

NOTES: 1. Pulse test required, pulsewidth 300 µs, duty cycle ≤ 3%.
2. For design reference only, not 100% tested.



Gate-Source or Gete Drain Voltage
(Note 1) -5
Gate Current (Note 1) 50n
Storage Temperature Hange -65°C to +200

Power Disalpation (To = 95°C)... 250mW 500mW
Denato above 25°C ........ 2.9mW/°C 4.3mW/°C

 TO-71
 WAFER
 DIDE

 2N6452
 2N6463/W
 2N5452/D

 2N6453
 2N6453/W
 2N6453/D

 2N6454
 2N5454/W
 2N6484/D

Whan ordering water/dice relar to Sentian 10, page 10-1.

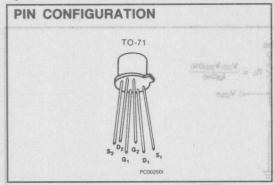
#### ELECTRICAL CHARACTERISTICS (TA - 25°C unless otherwise noted)

				2145	452	453	454	Service in
SYMBOL	PARAMETER	TEST CONOR		94180		XAM		TIMU
and the constitution of the contract of the co								
		Yos = 0, Iq = -1µA						
	Gate-Source Cutoff Voltage							
		0 = agv , vos = agv						
			\$60EF # \$4					
							0.8	
			XI-BA1 == 1					
	Drain-Gate Capacitance (Note 2)				1.5			

2-45

#### GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.



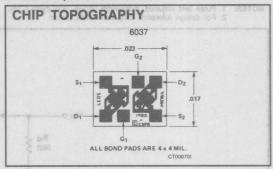
#### ORDERING INFORMATION\*

TO-71	WAFER	DICE
2N5452	2N5452/W	2N5452/D
2N5453	2N5453/W	2N5453/D
2N5454	2N5454/W	2N5454/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **FEATURES**

- Low Offset Voltage
- · Low Drift
- Low Capacitance
- Low Output Conductance



#### **ABSOLUTE MAXIMUM RATINGS**

(T<sub>A</sub> = 25°C unless otherwise noted)

 Gate-Source or Gate Drain Voltage
 -50V

 (Note 1)
 50mA

 Storage Temperature Range
 -65°C to +200°C

 Operating Temperature Range
 -55°C to +150°C

 Lead Temperature (Soldering, 10sec)
 +300°C

ONE SIDE BOTH SIDES

Power Dissipation (T<sub>C</sub> = 85°C) .... 250mW 500mW Derate above 25°C ...... 2.9mW/°C 4.3mW/°C

#### **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise noted)

					2N5	2N5452		2N5453		2N5454	
SYMBOL	PARAMETER	PARAMETER TEST CO				MAX	MIN	MAX	MIN	MAX	UNIT
						-100		-100		-100	рА
IGSS	Gate Reverse Current TA = 150°C		$V_{GS} = -30V, V_{DS} = 0$		1000	-200		-200		-200	nA
BVGSS	Gate-Source Breakdown Voltage	,	$V_{DS} = 0$ , $I_{G} = -1\mu A$		-50		-50		-50		
VGS(off)	Gate-Source Cutoff Voltage	,	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA		-1	-4.5	-1	-4.5	-1	-4.5	٧
V <sub>G</sub> S	Gate-Source Voltage Gate-Source Forward Voltage		$V_{DS} = 20V, I_D = 50\mu A$		-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	
V <sub>G</sub> S(f)			V <sub>DS</sub> = 0, I <sub>G</sub> = 1mA			2		2		2	
IDSS	Saturation Drain Current	1	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		0.5	5.0	0.5	5.0	0.5	5.0	mA
	Common-Source Forward			f = 1kHz	1000	3000	1000	3000	1000	3000	
9fs	Transconductance (Note	2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 100MHz	1000	V.	1000		1000	13676	
	Common-Source Output					3.0		3.0		3.0	μs
9os	Conductance	1	$V_{DS} = 20V, I_{D} = 200\mu A$	f = 1kHz		1.0		1.0		1.0	
Ciss	Common-Source Input Capacitance (Note 2)					4.0		4.0		4.0	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note	5 to 18 18 18 18 18 18 18 18 18 18 18 18 18	$V_{DS} = 20V$ , $V_{GS} = 0$	f = 1MHz		1.2		1.2		1.2	pF
C <sub>dgo</sub>	Drain-Gate Capacitance (Note 2)		$V_{DG} = 1.0V, I_S = 0$			1.5		1.5		1.5	

## 2N5452-2N5454

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

		TEST CONDITIONS			5452	2N5	453	2N5	5454	LIMIT
SYMBOL	PARAMETER				MAX	MIN	MAX	MIN	MAX	UNIT
e <sub>n</sub>	Equivalent Short Circuit Input Noise Voltage	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1kHz		20		20		20	nV √Hz
NF	Common-Source Spot Noise Figure (Note 2)	$V_{DS} = 20V$ , $V_{GS} = 0$ $R_G = 10M\Omega$	f = 100Hz		0.5		0.5		0.5	dB
IDSS1/IDSS2	Drain Saturation Current Ratio	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		0.95	1.0	0.95	1.0	0.95	1.0	
VGS1-VGS2	Differential Gate-Source Voltage				5.0	U.	10.0		15.0	
	Gate-Source Voltage		T = 25°C to -55°C		0.4	71-1-	0.8		2.0	
△IV <sub>GS1</sub> -V <sub>GS2</sub> I	Differential Change with Temperature	$V_{DS} = 20V, I_{D} = 200 \mu A$	T = 25°C to + 125°C		0.5		1.0		2.5	mV
9fs1/9fs2	Transconductance Ratio			0.97	1.0	0.97	1.0	0.95	1.0	
gos1-gos2	Differential Output Conductance		f = 1kHz		0.25	or minutes	0.25		0.25	μs

NOTES: 1. Per transistor.

2. For design reference only, not 100% tested.

	SNE467
PHEASPAW	

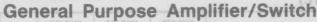
STREET PHADACTEDISTING MINISTER STREET

				MIM		KASA	
	Source Breakdown Volkage			-25			
	Gura Reverse Current						
			Vos = 15V, lp = 100A				
	Forward Transfer Admittance		Vps = 16V, Vps = 0, f = 116tz				
	Noisa Figure (Note 2)						

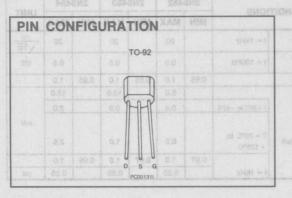
ICTES: 1, Police test required. PW < 630ms, Bully cycle 5 for

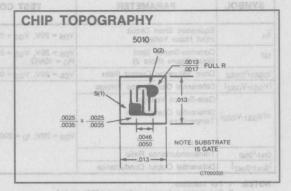
#### 2N5457-2N5459

#### **N-Channel JFET**









#### **ORDERING INFORMATION\***

TO-92	WAFER	DICE
2N5457	2N5457/W	2N5457/D
2N5458	2N5458/W	2N5458/D
2N5459	2N5459/W	2N5459/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **ABSOLUTE MAXIMUM RATINGS**

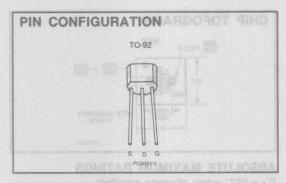
(T <sub>A</sub> = 25°C unless otherwise noted)
Drain-Gate Voltage
Drain-Source Voltage
Continuous Forward Gate Current 10mA
Storage Temperature Range65°C to +150°C
Operating Temperature Range55°C to +135°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation
Derate above 25°C 2.82mW/°C

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BVGSS	Gate-Source Breakdown Voltage		$I_{G} = -10\mu A, V_{DS} = 0$	-25	-60		V
			V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0			-1.0	
IGSS G	Gate Reverse Current		V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0, T <sub>A</sub> = 100°C		.05	-200	nA
	<b>设定的规则和1000000000000000000</b>	2N5457		-0.5		-6.0	
VGS(off)	Gate-Source Cutoff Voltage	2N5458	V <sub>DS</sub> = 15V, I <sub>D</sub> = 10nA	-1.0	TO TRE	-7.0	V
		2N5459		-2.0		-8.0	
		2N5457	V <sub>DS</sub> = 15V, I <sub>D</sub> = 100μA		-2.5		
VGS	Gate-Source Voltage	2N5458	V <sub>DS</sub> = 15V, I <sub>D</sub> = 200μA		-3.5		V
		2N5459	V <sub>DS</sub> = 15V, I <sub>D</sub> = 400μA		-4.5	G TO SERVICE	
		2N5457		1.0	3.0	5.0	NO. THE
IDSS		2N5458	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	2.0	6.0	9.0	mA
	(Note 1)	2N5459		4.0	9.0	16	
		2N5457		1000	3000	5000	μs
ly <sub>fs</sub>	Forward Transfer Admittance	2N5458	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, f = 1kHz	1500	4000	5500	
		2N5459		2000	4500	6000	
yos	Output Admittance		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, f = 1kHz		10	50	μs
Ciss	Input Capacitance (Note 2)		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, f = 1MHz		4.5	7.0	pF
Crss	Reverse Transfer Capacitance (Note	9 2)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, f = 1MHz		1.5	3.0	pF
NF	Noise Figure (Note 2)		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0, R <sub>G</sub> = 1MHz BW = 1Hz, f = 1kHz			3.0	dB

NOTES: 1. Pulse test required. PW ≤ 630ms, duty cycle ≤ 10% 2. For design reference only, not 100% tested.

#### Low Noise Amplifier



#### **ORDERING INFORMATION\***

TO-92	WAFER	DICE -
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY NOTE: SUBSTRATE

#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted) Drain-Gate or Source-Gate Voltage 2N5460 - 2N5462 ..... -40V Storage Temperature Range .....-65°C to +150°C Operating Temperature Range ...... -55°C to +135°C Lead Temperature (Soldering, 10sec) ......+300°C Power Dissipation ......310mW Derate above 25°C ...... 2.82mW/°C

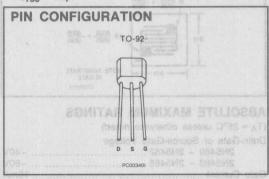
#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

SYMB	BOL	PARAME	TER	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
	-		2N5460, 2N5461, 2N5462	-	gain attache and the sail	40		and pro-	entransport (miles)
BVGSS		Gate-Source Breakdown Voltage	2N5463, 2N5464, 2N5465	$I_G = 10\mu A, V_C$	os = 0	60			V
THREE		Charles and the second	2N5460, 2N5463	41	Re.	0.75		6.0	SHELL
VGS(off)		Gate-Source Cutoff Voltage	2N5461, 2N5464	$V_{DS} = -15V$	$I_D = 1.0 \mu A$	1.0		7.5	V
		0.1-	2N5462, 2N5465	Umrs w Sixt		1.8	manufacture Co. and	9.0	
E ( E ( S )	NAME OF		2N5460, 2N5461, 2N5462	$V_{DS} = 0$	VGS = 20V			5.0	
		Gate Reverse Current	2N5463, 2N5464, 2N5465	NY AND - a of	V <sub>GS</sub> = 30V	GONESSES.		5.0	nA/
IGSS		0.2- 0.4- 0.0- 00- 8.0-	2N5460, 2N5461, 2N5462	el var - agv	V <sub>GS</sub> = 20V	V. Masure	emene of	1.0	Mosov
		08 07 0A TA = 100°C	2N5463, 2N5464, 2N5465	V <sub>OZ</sub> m 16V. V <sub>I</sub>	V <sub>GS</sub> = 30V	entil ner	a noneiu	1.0	μΑ
	0000	2000 5000 2000 2000 4000	2N5460, 2N5463	THE PARTY OF THE P	tres	-1.0	a2-nornii	-5.0	
loss		Zero-Gate Voltage Drain Current	2N5461, 2N5464			-2.0	automorphic and a second	-9.0	mA
		00 00	2N5462, 2N5465	$V_{DS} = -15V$	VGS = 0	-4.0	-16	200	
		Total Total	2N5460, 2N5463		ID = 0.1mA	0.5	n Panners	4.0	
VGS		Gate-Source Voltage	2N5461, 2N5464		$I_D = -0.2 \text{mA}$	0.8	neconduct	4.5	V
			2N5462, 2N5465		$I_D = -0.4 \text{mA}$	1.5	nenem-Se	6.0	
	661	100 C	2N5460, 2N5463	West - 15W. Was		1000	CONTROLOGICA	4000	(6176)
9fs		Forward Transadmittance	2N5461, 2N5464			1500	CONTRACTOR AND A	5000	μs
			2N5462, 2N5465			2000	of norm	6000	
9os	6.0	Output Admittance		$V_{DS} = -15V$	f = 1.0kHz	(S. micki)	eangillage	75	μS
Ciss		Input Capacitance (Note 1)		V <sub>GS</sub> = 0V	901	over Feve	5.0	0 7	pF
Crss	9.1	Reverse Transfer Capacitance (No	te 1)		f = 1MHz	abnatios	1.0 an	2.0	pF
NF	1000	Common-Source Noise Figure (Not	e 1)		f = 100Hz	CRUST ASSE	1.0	2.5	DB
ē <sub>n</sub>		Equivalent Short-Circuit Input Noise Voltage (Note 1)			BW = 1.0Hz $R_G = 1.0M\Omega$	(5. (80)4)	60	115	nV/ √Hz

NOTE 1: For design reference only, not 100% tested.

#### **FEATURES**

- Up to 400MHz Operation
- Economy Packaging
- Cres < 1.0pF



#### **ORDERING INFORMATION\***

TO-92	WAFER	DICE
2N5484	2N5484/W	2N5484/D
2N5485	2N5485/W	2N5485/D
2N5486	2N5486/W	2N5486/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY 5000 0035 0025 FULL R 5000 0035 0025 0025 NOTE: SUBSTRATE IS GATE CT002211

#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise specified) Drain-Gate Voltage	
Drain-Gate Voltage	25V
Source Gate Voltage	25V
Drain Current3	OmA
Forward Gate Current1	0mA
Storage Temperature Range65°C to +15	50°C
Operating Temperature Range55°C to +13	35°C
Lead Temperature (Soldering, 10sec)+30	OooC
Power Dissipation310	WmC
Derate above 25°C 2.82mV	V/°C
A THE PARTY OF THE	

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

V		00 000	N. Andrea of Bases	, sasav	\$N5463. 2	2N5	484	2N5	5485	2N5	5486	820V8
SYMBOL		PARAMETER	TEST CONDITIONS			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Igss	0.0	Gate Reverse Current T <sub>A</sub> = 100°C	$V_{GS} = -20V, V_{DS} = 0$	NSARS	CNEASO, C		-1.0 -200		-1.0 -200		-1.0 200	nA
BVGSS	Q.	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A$ , $V_{DS} = 0$	1808	E PALADE	-25	- In	-25	adreson.	-25		
V <sub>G</sub> S(off)	0.1	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 10nA	2 - 10.747	PK 1991-2049	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0	V
IDSS	0.1	Saturation Drain Current	VDS = 15V, VGS = 0 (No	te 1)	S COLEME	1.0	5.0	4.0	10	8.0	20	mA
9fs -	5.0	Common-Source Forward Transconductance		C81/31/	2 Davides 2	3000	6000	3500	7000	4000	8000	
9os	81	Common-Source Output Conductance	V67 16V		f = 1kHz		50		60		75	8880
Re(yfs)	6.0	Common-Source Forward Transconductance (Note 2)			f = 100MHz f = 400MHz	2500		3000	Bonsis	3500		20
Re <sub>(yos)</sub>	0.6	Common-Source Output Conductance (Note 2)			f = 100MHz f = 400MHz		75		100		100	μs
Re <sub>(yis)</sub>	cos	Common-Source Input Conductance (Note 2)	$V_{DS} = 15V, V_{GS} = 0$		f = 100MHz f = 400MHz		100	Smirae	1000	-	1000	41
Ciss	000	Common-Source Input Capacitance (Note 2)			13070015		5.0	9068	5.0	Surgial)	5.0	piol
14	1	Common-Source Reverse	V0 = 88V				avoid.	95/15	Nosan	) turq		201
Crss		Transfer Capacitance (Note 2)			f = 1MHz	n man	1.0		1.0	anover	1.0	pF
Coss	2.5	Common-Source Output Capacitance (Note 2)			(1 jele	D Page	2.0	ald est	2.0	aterisco)	2.0	

#### **BINTERSIL**

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	DADAMETED	TEST COMPLETO				2N5	5485	2N5	5486	LINUT
	PARAMETER	OT ONE	TEST CONDITIONS		MAX	MIN	MAX	MIN	MAX	UNIT
		$V_{DS} = 15V$ , $V_{GS} = 0$ , $R_G = 1M\Omega$	f = 1kHz		2.5	and the	2.5	a contract	2.5	Sent'S
	(A3-0522HS) 9100	$V_{DS} = 15V$ , $V_{D} = 1mA$ , $R_{G} = 1k\Omega$			3.0		9	tonin	538 te	iger iger
NF	Noise Figure		f = 100MHz	230	radio	THE THE	2.0	Dillin		Billi Non
	(Note 2)	V <sub>DS</sub> = 15V, I <sub>D</sub> = 4mA,			-					4500
	(Note 2)	$R_G = 1k\Omega$	f = 400MHz		MO	FTA	4.0	好物的	4.0	PIN
Gps	No contract of the contract of	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1mA		16	25					dB
	Common-Source Power Gain	A STATE OF THE STA	f = 100MHz		17	18	30	18	30	
	(Note 2)	V <sub>DS</sub> = 15V, I <sub>D</sub> = 4mA	f = 400MHz		-	10	20	10	20	

**NOTES:** 1. Pulse test required. Pulse width =  $300\mu$ s, duty cycle  $\leq$  3%. 2. For design reference only, not 100% tested.

SOUTTAS MUNICAM STUTOSSA

Gate-Source or Gate-Drain Voltage ...... - 40V

Operating Temperature Range ......-55°C to +150°C
Operating Temperature Range .....-55°C to +150°C
Lead Temperature (Soldering, 10sec) .....

Power Dissipation (TA = 85°C) ... 250mW 875mW

to blancid and GTOR

	SNEETZZW	
2N6519/D		
		osaaus

1-43 albit on unidoes of philip enduring Suppose House.

ELECTRICAL CRARACTERISTICS (25°C unless otnerwise noted)

		поисо теат	SHOU			
315						
	Common-Source Playartes Transler Capacitanos (Note S)					

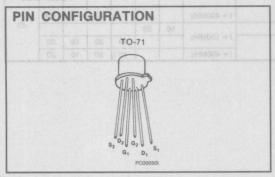
### 2N5515-2N5524

#### **Dual N-Channel JFET** Low Noise Amplifier



#### FEATURES XAM HIM XAM HIM

- Tight Temperature Tracking
- **Tight Matching**
- High Common Mode Rejection
- Low Noise



#### ORDERING INFORMATION\*

OLIDPLIA	O HAI OIL	IAILAIIAIA
TO-72	WAFER	DICE
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520		
2N5521		
2N5522		
2N5523		
2N5524		

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY ALL BOND PADS ARE 4 x 4 MIL. CT005711

#### **ABSOLUTE MAXIMUM RATINGS**

Power Dissipation (TA = 85°C) .... 250mW 375mW 3.0mW/°C Derate above 25°C ...... 2.0mW/°C

NOTE: Per transistor.

**ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

#### MIN SYMBOL PARAMETER **TEST CONDITIONS** MAX UNIT - 250 pA Gate Reverse Current $V_{GS} = -30V, V_{DS} = 0$ IGSS T<sub>A</sub> = 150°C - 250 nA BVGSS Gate-Source Breakdown Voltage $I_G = -1 \mu A$ , $V_{DS} = 0$ -40 V VP Gate-Source Pinch-Off Voltage $V_{DS} = 20V$ , $I_D = 1nA$ -0.7 -4 Drain Current at Zero Gate Voltage (Note 1) 0.5 7.5 mA IDSS Common-Source Forward Transconductance 1000 4000 9fs f = 1kHzUS Common-Source Output Conductance 10 goss V<sub>DS</sub> = 20V, V<sub>GS</sub> = 0 Common-Source Reverse Transfer 5 Crss Capacitance (Note 3) f = 1MHz pF Ciss Common-Source Input Capacitance (Note 3) 25

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

2N5515-2N5524 ELECTRICAL CHARACTERISTICS (CONT.)							
SYMBOL	SYMBOL PARAMETER		TEST CONDITIO	TEST CONDITIONS		MAX	UNIT
	1 7 2 7 7 7 1 1 1 1 1 1 1	2N5515-19				30	W. W. W. W. W.
e <sub>n</sub>	Equivalent Input Noise Voltage	2N5520-24		f = 10Hz	STREET, MARKET	15	nV/√Hz
	(Note 3)	2N5515-24	95/8	f = 1kHz	Aman 2	10	turn 1 S
	THE RESTRICTED STREET TODAY OF THE PROPERTY OF		Service of the Libert Colonia Colonia Colonia Colonia	STATE OF STREET OF STREET		- 100	pA
IG	Gate Current	T <sub>A</sub> = 125°C	$V_{DG} = 20V, I_D = 200\mu A$	MOTTAF	WOL	-100	nA
Vgs	Gate Source Voltage				-0.2	-3.8	V
9fs	Common-Source Forward Transconductance (Note 1)			f = 1kHz	500	1000	μs
goss	Common-Source Output Conductar	nce			BENN	1	μs

#### MATCHING CHARACTERISTICS (25°C unless otherwise noted)

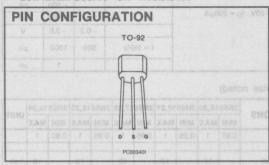
OVERDO OF	PARAMETER	TOT CONDITIONS	2N55	15,20	2N55	16,21	2N55	17,22	2N55	18,23	2N55	19,24	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
IDSS1/IDSS2	Drain Current Ratio at Zero Gate Voltage (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	0.95	1	0.95	1	0.95	10	0.95	1	0.90	1	
G1 -   G2	Differential Gate Current (+125°C)	$V_{DG} = 20V, I_D = 200 \mu A$	2000.000	10	100000	10	TUMO!	10		10	son exists	10	nA
9fs1/9fs2	Transconductance Ratio (Note 1)	$V_{DG} = 20V$ , $I_{D} = 200 \mu A$ f = 1kHz	0.97	1	0.97	111	0,95	H	0.95	/1	0.90	4.11	
Igoss1 - goss2	Differential Output Conductance	$V_{DG} = 20V, I_D = 200\mu A$ f = 1kHz		0.1		0.1	CHE	0.1	Mar.	0.1		0.1	μs
IVGS1 - VGS2	Differential Gate-Source Voltage	$V_{DG} = 20V, I_D = 200\mu A$		5		5	isaai	10	W/65	15		15	mV
$\frac{\Delta  V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (TA = -55°C to +125°C)	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA		5	site it	10	15641 568	20	N/Ot	40	L J	80	μV/ °C
CMRR	Common Mode Rejection Ratio (Note 2, 3)	V <sub>DD</sub> = 10 to 20V, I <sub>D</sub> = 200µA	100	80	100	HALB	90	AFRE	Hio	14	Olf	rro	dB

TIME	3.	CMR For d	R = 2	20 log- referer	nce on	J/ΔIVO ly, not	luring test. GS1- VGS2I, (ΔVDD 100% tested.				REYEMARAS	
								() ze -	ny Audit - mai		Gate Raverse Bresidown	
								0 = 0	Vac = 15V Ve			
								= - 12V (28	VDS = 15V, VGs VGS = -8V (2N	0°001 = AT	Drain Outed Gurent	
									VGS = 0. 10 = 12 20 = 0 Ama = 01		Orain-Gourda ON Vollage	
											Static Dayn-Source ON Re	
					08		116H # 1		Vos = 0, lo = 0			
					10						Common-Source Input Capacitance (Note 2)	
			0.48		4.0		f= tMHz		Vos= -12V, Vi	retenevi		
							(BEGGMS) Ams		Vor = mov			
					6.0		(BEBUMS) Ami	# (mg)(3)	Vosten) * 0			
										(S. P.		
			OS.		10						Fail Time (Note 2)	

MOYES: 1. Pulse test PW 5 300us, duty cycle 5 3.0%. 2. For design releasance only, not 100% feeled.

#### **FEATURES**

- Economy Packaging
- **Fast Switching**
- Low Drain-Source 'ON' Resistance



#### ORDERING INFORMATION\*

TO-92	WAFER	DICE
2N5638	2N5638/W	2N5638/D
2N5639	2N5639/W	2N5639/D
2N5640	2N5640/W	2N5640/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY 5001 0072 NOTE SUBSTRATE IS GATE

#### ABSOLUTE MAXIMUM RATINGS

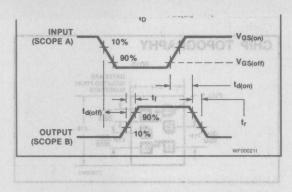
(TA = 25°C unless otherwise specified) Drain-Source Voltage.......30V Source-Gate Voltage ...... 30V Storage Temperature Range ..... -65°C to +150°C Operating Temperature Range ...... -55°C to +135°C Lead Temperature (Soldering, 10sec) .....+300°C Power Dissipation ......310mW Derate above 25°C ...... 2.82mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

OVIMBOL				poY44 AssoY -re	2N5	638	2N5	639	2N5	640	111721
SYMBOL	PARAMETER		TEST CONDI	TIONS areal arous	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
BVGSS	Gate Reverse Breakdown Vo	oltage	$I_{G} = -10\mu A$ , $V_{DS} = 0$		- 30		-30		- 30		V
Igss	Gate Reverse Current	T <sub>A</sub> = 100°C	V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0			- 1.0 - 1.0		-1.0 -1.0		- 1.0 - 1.0	-
I <sub>D(off)</sub>	Drain Cutoff Current	Γ <sub>A</sub> = 100°C	V <sub>DS</sub> = 15V, V <sub>GS</sub> = -12V (2) V <sub>GS</sub> = -8V (2N5639), V <sub>GS</sub>	N5638) = -6V (2N5640)		1.0		1.0		1.0	nA μA
IDSS	Saturation Drain Current		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 (Note 1	1)	50		25		5.0		mA
V <sub>DS(on)</sub>	Drain-Source ON Voltage		$V_{GS} = 0$ , $I_D = 12mA$ (2N563 $I_D = 6mA$ (2N5639), $I_D = 3m$			0.5		0.5		0.5	٧
rDS(on)	Static Drain-Source ON Resi	istance	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0			30		60		100	
rds(on)	Drain-Source ON Resistance		V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1kHz		30		60		100	Ω
C <sub>iss</sub>	Common-Source Input Capacitance (Note 2)					10		10		10	
C <sub>rss</sub>	Common-Source Reverse Tra Capacitance (Note 2)	ansfer	$V_{GS} = -12V, V_{DS} = 0$	f = 1MHz		4.0		4.0		4.0	pF
td(on)	Turn-On Delay Time (Note 2	2)	V 10V	Om A (ONECOO)		4.0		6.0		8.0	
tr	Rise Time (Note 2)		$V_{DD} = 10V$ $I_{D(on)} = 1$ $V_{GS(on)} = 0$ $I_{D(on)} = 0$	2mA (2N5638) 6mA (2N5639)		5.0		8.0		10	
td	Turn-OFF Delay Time (Note	2)	$V_{GS(off)} = -10V I_{D(on)} = 3$	3mA (2N5640)		5.0	N S	10		15	ns
tf	Fall Time (Note 2)		$R_G = 50\Omega$ (Note 2)			10		20		30	

NOTES: 1. Pulse test; PW ≤ 300 µs, duty cycle ≤ 3.0%.

2. For design reference only, not 100% tested.



#### ABSOLUTE MAXIMUM PATINGS

(Ty = 25°C unless otherwise specified)

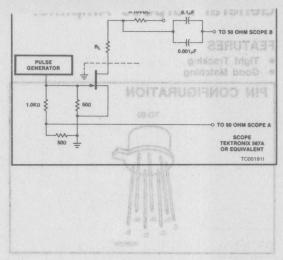
Cate Course Temporary

Spending Temperature Range .....+55°C to +150°C sed Temperature (Soldering, 10sec) .........+300°C

ONE SIDE BOTH SIDES

 'owier Dissipation
 367mW
 500mW

 Oerste stove 25°C
 3mW/°C
 4mW/°C



	WAFER	
	SNEBOSAW	SNRBOS
ZNSBOBAT		
2N69077D		
	ZNEDOB/W	
	WNeeeeMS	

<sup>1-01</sup> dead of military to later to Samina 10 dead 10-1

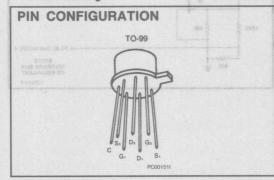
#### ELECTRICAL CHARACTERISTICS (25°C unless observice noted)

		REMS			eavis:			
		Miss	MIN	XAM			PARAMETER	
								rezo    case
08						1A = 25°C 1B + 125°C		

#### 2N5902-2N5909 **Dual N-Channel JFET General Purpose Amplifier**

#### **FEATURES**

- Tight Tracking
- Good Matching

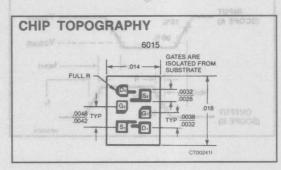


#### **ORDERING INFORMATION\***

TO-99	WAFER	DICE
2N5902	2N5902/W	2N5902/D
2N5903	2N5903/W	2N5903/D
2N5904	2N5904/W	2N5904/D
2N5905	2N5905/W	2N5905/D
2N5906	2N5906/W	2N5906/D
2N5907	2N5907/W	2N5907/D
2N5908	2N5908/W	2N5908/D
2N5909	2N5909/W	2N5909/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## 



#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise specified)

Gate-Drain or Gate-Source	
Voltage (Note 1)	40V
Gate Current (Note 1)	10mA
Storage Temperature Range65°C to	+200°C
Operating Temperature Range55°C to	+150°C
Lead Temperature (Soldering, 10sec)	+300°C

ONE SIDE BOTH SIDES

Power Dissipation	367mW	500mW
Derate above 25°C	3mW/°C	4mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

				2N59	902-6	2N5	903-7	2N5	904-8	2N5	905-9	
SYMBOL	PARAMETER	TEST CO	NDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		V <sub>DG</sub> = 10V,	2N5902-5		2.0		2.0		2.0		2.0	
I IG1-IG2	Differential Gate Current	$I_D = 30\mu A$ , $T_A = 125^{\circ}C$	2N5906-9		0.2		0.2		0.2	1	0.2	nA
I <sub>DSS1</sub> I <sub>DSS2</sub>	Saturation Drain Current Ratio	V <sub>DS</sub> = 10V, V	GS = 0	0.95	1	0.95	1	0.95	1	0.95	1	
9fs1 9fs2	Transconductance Ratio		f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	
VGS1-VGS2	Differential Gate-Source Voltage				5		5		10		15	mV
ΔIV <sub>BS1</sub> -V <sub>GS2</sub>	Gate-Source Voltage Differential	$V_{DG} = 10V,$ $I_{D} = 30\mu A$	T <sub>A</sub> = 25°C T <sub>B</sub> = 125°C		5		10		20		40	
ΔΤ	Drift (Measured at end points TA and TB)		$T_A = -55$ °C $T_B = 25$ °C		5		10		20		40	μV/°C
gos1-gos2	Differential Output Conductance		f = 1kHz	24.3	0.2		0.2		0.2		0.2	μs

# 2N5902-2N5909 - SAS THERES

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

			1376	2N5	902-5	2N59	906-9	SHE
SYMBOL	PARAMETER	TEST CONDITI	ONS	MIN	MAX	MIN	MAX	TINU
					-5		-2	рА
IGSS	Gate Reverse Current TA = 125°C	$V_{GS} = -20V, V_{DS} = 0$			-10	2	-5	nA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A$ , $V_{DS} = 0$		- 40		-40		-
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA		-0.6	-4.5	-0.6	-4.5	V
V <sub>G</sub> S	Gate Source Voltage				-4	/ FELSES	-4	MADAIL
	Sin tons 19 4 Various Land				-3	State of	- 1	pA
IG (P	Gate Operating Current T <sub>A</sub> = 125°C	$V_{DG} = 10V, I_D = 30\mu A$		LAFTE	-3	BETA BURN	003	nA
IDSS	Saturation Drain Current			30	500	30	500	μΑ
9fs	Common-Source Forward Transconductance		f = 1kHz	70	250	70	250	μs
gos	Common-Source Output Conductance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0			5		5	
Ciss	Common-Source Input Capacitance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		63	3	and I	3	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	(Note 1)	f = 1MHz		1.5	10	1.5	pF
9fs	Common-Source Forward Transconductance	V <sub>DG</sub> = 10V, I <sub>D</sub> = 30μA		50	150	50	150	μs
gos	Common-Source Output Conductance	G-stsD	f = 1kHz		1	Hill .	1	1
ē <sub>n</sub> and of	Equivalent Short Circuit Input Noise Voltage (Note 1)	Gate C Storage		16	0.2	100	0.1	$\frac{\mu V}{\sqrt{Hz}}$
NEC 1		V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0	f = 100Hz $R_G = 10M\Omega$		3		1	dB

NOTE 1: For design reference only, not 100% tested.

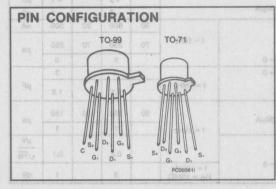
	89-07	10-71
	2192012	steatt

	MARKET				SYMBOL
		Vgs = -15V, Vgs = 0			
		0 = agV ,Aut - = a		e Reverge Streekdown Voltage	
				( Noise Figure (Note 1)	

### Dual N-Channel JFET High Frequency Amplifier

#### **FEATURES**

- Tight Tracking
- Low Insertion Loss
- Good Matching



#### 

#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	25V
Gate Current	
Storage Temperature Range65°C	to +200°C
Operating Temperature Range55°C	to +150°C
Lead Temperature (Soldering, 10sec)	+ 300°C
Storage Temperature Range65°C Operating Temperature Range55°C	to +200°C to +150°C

#### **ORDERING INFORMATION\***

TO-71	TO-99	WAFER	DICE
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### TO-71 who something TO-99 ONE BOTH ONE BOTH SIDE SIDES SIDE SIDES Power Dissipation..... 200mW 400mW 367mW 500mW Derate above 25°C ..... 1.6mW/°C 3.2mW/°C 3.0mW/°C 4.0mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER		TEST CONE	OITIONS	MIN	MAX	UNIT
TENLET DE						- 100	рА
IGSS	Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = -15V, V_{DS} = 0$			- 250	nA
BVGSS	Gate Reverse Breakdown Voltage		$I_{G} = -1\mu A, V_{DS} = 0$		- 25		
VGS(off)	Gate-Source Cutoff Voltage		V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA		-1	-5	٧
VGS	Gate-Source Voltage		V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA		-0.3	-4	
						- 100	рА
IG	Gate Operating Current	$T_A = 125^{\circ}C$				-100	nA
IDSS	Saturation Drain Current (Pulsewidth duty cycle ≤ 3%)	300μs,	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V		7	40	mA
gf <sub>S</sub>	Common-Source Forward Transcond	luctance		f = 1kHz	5000	10,000	
gfs	Common-Source Forward Transcond (Note 1)	luctance		f = 100MHz 5000	5000	10,000	
gos	Common-Source Output Conductance	e			100	μs	
9oss .	Common-Source Output Conductance	e (Note 1)		f = 100MHz		150	
Ciss	Common-Source Input Capacitance	(Note 1)	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA			5	
C <sub>rss</sub>	Common-Source Reverse Transfer (Note 1)	Capacitance		f = 1MHz		1.2	pF
ē <sub>n</sub>	Equivalent Short Circuit Input Noise (Note 1)	Voltage		f = 10kHz		20	nV √Hz
NF	Spot Noise Figure (Note 1)			f = 10kHz $R_G = 100k\Omega$		1	dB

#### 2N5911, 2N5912 IT5911, IT5912

**ELECTRICAL CHARACTERISTICS (CONT.)** 

	VINLABOAROT O	HO TEST CON	IT, 2	IT, 2N5911		IT, 2N5912		
SYMBOL	PARAMETER	TEST CON	MIN	MAX	MIN	MAX	UNIT	
IIG1-IG2	Differential Gate Current	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA	125°C		20	州的	20	nA
I <sub>DSS1</sub> I <sub>DSS2</sub>	Saturation Drain Current Ratio	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0 (Pulsewidth 300μs, duty	cycle ≤ 3%)	0.95	1	0.95	17 16 1	97 s
VGS1-VGS2	Differential Gate-Source Voltage			H Salt I a	10	ALC: SE	15	mV
ΔIV <sub>GS1</sub> -V <sub>GS2</sub>	Gate-Source Voltage Differential		T <sub>A</sub> = 25°C T <sub>B</sub> = 125°C	17-OT	20		40	
ΔT (653)	Drift (Measured at end points, TA and TB)	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA	T <sub>A</sub> = -55°C T <sub>B</sub> = 25°C		20	40	μV/°C	
gfs1 gfs2	Transconductance Ratio	LOGA	f = 1kHz	0.95	1	0.95	.1	

NOTE	1:	For	design	reference	only.	not	100%	tested

Lead Temperature (Soldering, 10sed) + 800°C	

	11-01
ZN64837W	
2N64847W	2N6484
WYSBERNS	

Dual N-Channel JFET Low Noise Ampililer

	PONTRIPRITOR DA	ELECTRICAL CH

	MAN			
		Ves = 20V, Vps = 0		
		0 = goV ,Aut - = pl		
Am		Vps + 20V. Vps + 0		
			Common-Source Forward Transconductance (Note 2)	
				anoli
				Ciss
		Vps = 20V, Vos = 0, f = 1MHz (Note 6)		
		to atom Appoint of 1995 with the contract of		
		Augus = gl .Vus = ggV	Gate Source Voltage	
		VDG = 20V, 1g = 200pA, 1 = 11312	Common-Scurge Forward Transponductance	
			Common Souce Orugus Conductance	
			Equivalent Input Noisa Voltage (Note 6)	

QTES; 1. Per transistor.
2. Prise test required; pulse width - 2m

2

#### 2N6483-2N6485 **Dual N-Channel JFET** Low Noise Amplifier



#### **FEATURES**

- Ultra Low Noise
- High CMRR
- . Low Offset
- Tight Tracking

## PIN CONFIGURATION TO-71 D,

#### **ORDERING INFORMATION\***

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### CHIP TOPOGRAPHY Si 0035 x 0080 0025 x 0070 TYP: 2 PLACES - G2 Dz .0035 x .0035 .0025 X .0025 TYP. 2 PLACES Amil = gl , V01 = gg/

#### ABSOLUTE MAXIMUM RATINGS

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Source or Gate-Drain Voltage (Note 1)50V
Gate-Gate Voltage±50V
Gate Current (Note 1) 50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +175°C
Lead Temperature (Soldering, 10sec) +300°C

ONE SIDE **BOTH SIDES** 

Power Dissipation ..... 400mW 250mW Derate above 25°C..... 1.7mW/°C 2.7mW/°C

#### **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
				-200	pA	
IGSS	Gate Reverse Current T <sub>A</sub> = 150°C	$V_{GS} = -30V, V_{DS} = 0$		-200	nA	
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$	-50			
Vp	Gate-Source Pinch Off Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	-0.7	-4.0	V	
IDSS	Drain Current at Zero Gate Voltage (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	0.5	7.5	mA	
9fs	Common-Source Forward Transconductance (Note 2)		1000	4000		
9oss	Common-Source Output Conductance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0, f = 1kHz (Note 6)			μs	
Ciss	Common-Source Input Capacitance			20		
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0, f = 1MHz (Note 6)		3.5	pF	
				100	pA	
IG	Gate Current T <sub>A</sub> = 150°C	$V_{GD} = 20V$ , $I_D = 200\mu A$ (Note 6)		100	nA	
VGS	Gate Source Voltage	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA	0.2	3.8	V	
9fs	Common-Source Forward Transconductance	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA, f = 1kHz	500	1500		
gos	Common-Source Output Conductance	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA		1	1 µs	
		$V_{DS} = 20V$ , $I_{D} = 200 \mu A$ , $f = 10Hz$		10		
en	Equivalent Input Noise Voltage (Note 6)	$V_{DS} = 20V$ , $I_{D} = 200 \mu A$ , $f = 1 kHz$	5		nV/VF	

NOTES: 1. Per transistor.

2. Pulse test required; pulse width = 2ms.

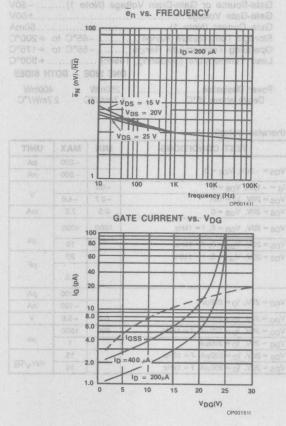
#### MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

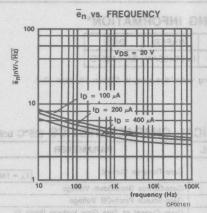
	PARAMETER		2N6483		2N6484		2N6485		111117
SYMBOL		TEST CONDITIONS	MIN	MAX	MIN MAX		MIN MA	MAX	UNIT
IDSS1 IDSS2	Drain Current Ratio at Zero Gate Voltage	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 (Note 4)	0.95	is phis	0.95	objenu upen a	0.95	N-Pha	eidT ion wo
I <sub>G1</sub> - I <sub>G2</sub>	Differential Gate Current	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA T <sub>A</sub> = +125°C	ni edl	10	iriz an vice id	10	etema	10	nA
9fs1 9gs2	Transconductance Ratio	$V_{DG}=20V, I_{D}=200\mu A, f=1kHz (Note 4)$	0.97	inique.	0.97	isune	0.95	onqup	off wo
gos1 - gos2	Differential Output Conductance (Note 6)	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}, f = 1 \text{kHz}$		0.1	214,34	0.1	A-78 87	0.1	μs
V <sub>GS1</sub> - V <sub>GS2</sub>	Differential Gate-Source Voltage	$V_{DG} = 20V, I_D = 200\mu A$		5	0-71	10		15	mV
ΔI V <sub>GS1</sub> - V <sub>GS2</sub>   ΔT	Gate-Source Voltage Differential Drift	$V_{DG} = 20V$ , $I_{D} = 200\mu A$ $T_{A} = -55^{\circ}C$ to $+125^{\circ}C$		5	to	10		25	μV/°C
CMRR	Common Mode Rejection Ratio (Note 6)	V <sub>DD</sub> = 10 to 20V, I <sub>D</sub> = 200μA (Note 5)	100		100		90		dB

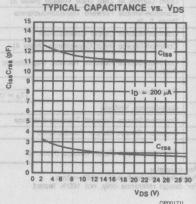
NOTES: 3. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

Pulse duration of 2ms used during test.
 CMRR = 20Log<sub>10</sub>ΔV<sub>DD</sub>/Δ| V<sub>GS1</sub>-V<sub>GS2</sub>|, (ΔV<sub>DD</sub> = 10V), not included in JEDEC registration.
 For design reference only, not 100% tested.

#### TYPICAL PERFORMANCE CHARACTERISTICS

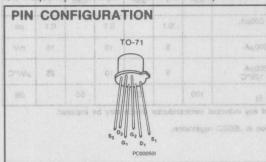






#### GENERAL DESCRIPTION

This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10Hz and 1000Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.



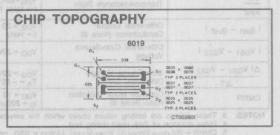
#### **ORDERING INFORMATION\***

TO-71	WAFER	DICE	
IMF6485	IMF6485/W	IMF6485/D	1

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **FEATURES**

- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking



#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise n	oted)	TYPICAL
Gate-Source or Gate-Drain Vo Gate-Gate Voltage	-65° -55° 10sec)	1)50V ±50V 50mA °C to +200°C °C to +175°C
Power Dissipation	250mW 1.7mW/°C	400mW 2.7mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
				-200	pA
IGSS	Gate Reverse Current T <sub>A</sub> = 150°C	$V_{GS} = -30V, V_{DS} = 0$	1	-200	nA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A$ , $V_{DS} = 0$	-50		
Vp	Gate-Source Pinch-Off Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	-0.7	-4.0	V
IDSS	Drain Current at Zero Gate Voltage (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	0.5	7.5	mA
9fs .	Common-Source Forward Transconductance (Note 2, 3)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0, f = 1kHz	1000	4000	
9oss .	Common-Source Output Conductance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0, f = 1kHz	10		μs
Ciss	Common-Source Input Capacitance (Note 4)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0, f = 1MHz		20	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 4)			3.5	pF
	production of the second secon			-100	pA
IG	Gate Current T <sub>A</sub> = 150°C	$V_{GD} = 20V, I_D = 200\mu A$		-100	nA
V <sub>G</sub> S	Gate-Source Voltage	$V_{DG} = 20V, I_D = 200\mu A$	0.2	-3.8	V
9fs	Common-Source Forward Transconductance	$V_{DG} = 20V$ , $I_{D} = 200\mu A$ , $f = 1kHz$	500	1500	
9os	Common Source Output Conductance	$V_{DG} = 20V, I_D = 200\mu A$	Control Co	1	μs
	Tue TITLEFT!	$V_{DS} = 20V$ , $I_{D} = 200 \mu A$ , $f = 10 Hz$	Sec. I	15	
en	Equivalent Input Noise Voltage (Note 4)	$V_{DS} = 20V$ , $I_{D} = 200\mu A$ , $f = 1kHz$		10	nV/√F

NOTES: 1. Per transistor.

2. Pulse test required; pulse width = 2ms.

3. For design reference only, not 100% tested.

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	87	04	

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I <sub>DSS1</sub>	Drain Current Ratio at Zero Gate Voltage	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 (Note 2)	0.95	1	THE
I <sub>G1</sub> - I <sub>G2</sub>	Differential Gate Current 11 91 14 2	$V_{DG} = 20V$ , $I_D = 200\mu A$ $T_A = +125^{\circ}C$		10	nA
9fs1 9gs2	Transconductance Ratio	V <sub>DG</sub> = 20V, 1 <sub>D</sub> = 200 μA, f = 1kHz (Note 2)	0.95	co.i-eu ve.i-eu velloo	Chai Squa Distr
gos1 - gos2	Differential Output Conductance (Note 4)	$V_{DG} = 20V$ , $I_D = 200\mu A$ , $f = 1kHz$	t Subs	0.1	μs
VGS1 - VGS2	Differential Gate-Source Voltage	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA	oseno	25	mV
$\frac{\Delta  V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift	V <sub>CG</sub> = 20V, I <sub>D</sub> = 200μA T <sub>A</sub> = -55°C to + 125°C	e to C	40	μV/°C
CMRR	Common Mode Rejection Ratio (Note 3, 4)	V <sub>DD</sub> = 10 to 20V, I <sub>D</sub> = 200μA	90		dB

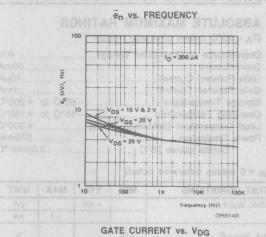
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

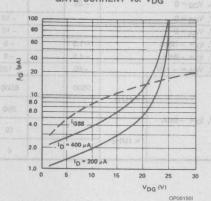
2. Pulse duration of 2ms used during test.

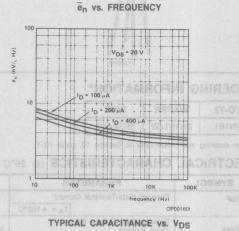
3. CMRR =  $20\text{Log}_{10}\Delta\text{V}_{DD}$  / $\Delta\text{I}$  V<sub>GS1</sub> + V<sub>GS2</sub> |, ( $\Delta\text{V}_{DD}$  = 10V )

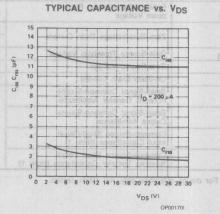
4. For design reference only, not 100% tested.

#### TYPICAL PERFORMANCE CHARACTERISTICS









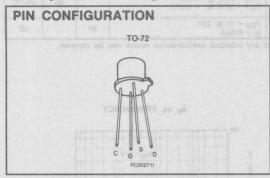
#### 3N161

#### Diode Protected P-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch



#### **FEATURES**

- Channel Cut Off With Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces
   Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate From Damage Due to Overvoltage



#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
3N161	3N161/W	3N161/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# CHIP TOPOGRAPHY 1507Z 25 MIL G B 27 MIL ARABA ARABA CTOO272L

#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage	40V
Drain Current	50mA
Gate Forward Current	
Gate Reverse Current	1mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	375mW
Derate above 25°C	3.0mW/°C

#### ELECTRICAL CHARACTERISTICS (@ 25°C and VBS = 0 unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIO	ONS	MIN	TYP	MAX	UNIT
IGSSF	Forward Gate-Terminal Current V <sub>GS</sub> = -25V, V <sub>DS</sub> = 0			-100		pA	
	T <sub>A</sub> = +100°C	0419090				-1	nA
BVGSS	Forward Gate-Source Break- down Voltage	IG = -0.1mA, V <sub>DS</sub> = 0	A TABLE AND A STATE OF THE STAT	- 25	(0)		٧
	An extended the decided department of the control o	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0			resolven CDR	-10	nA
IDSS	Zero-Gate-Voltage Drain Current	V <sub>DS</sub> = -25V, V <sub>GS</sub> = 0			TO	-10	μΑ
V <sub>G</sub> S(th)	Gate-Source Threshold Voltage	$V_{DS} = -15V$ , $I_{D} = -10\mu A$		-1.5	200	-5	
VGS	Gate-Source Voltage	V <sub>DS</sub> = -15V, I <sub>D</sub> = -8mA		-4.5		-8	V
ID(on)	On-State Drain Current	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -15V		- 40	25	- 120	mA
lyfs	Small-Signal Common-Source Forward Transfer Admittance		X-1	3500		6500	
lyosl	Small-Signal Common-Source Output Admittance		f = 1kHz		0.0	250	μs
Ciss	Common-Source Short-Circuit Input Capacitance (Note 1)	$V_{DS} = -15V$ , $I_{D} = -8mA$		NO.	- 0.0 No.	10	
C <sub>rss</sub>	Common-Source Short Circuit Reverse Transfer Capacitance (Note 1)		f = 1MHz	100	0.5	4	pF

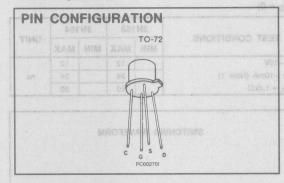
NOTE 1: For design reference only, not 100% tested.

#### 3N163, 3N164 P-Channel Enhancement Mode **MOSFET General Purpose Amplifier** Switch



#### **FEATURES**

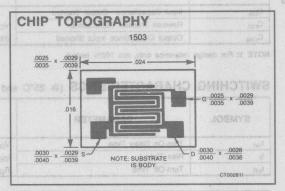
- Very High Input Impedance
- High Gate Breakdown
- **Fast Switching**
- Low Capacitance



#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
3N163	3N163/W	3N163/D
3N164	3N164/W	3N164/D

\*When ordering wafer/dice refer to Section 10, page 10-1.



#### ABSOLUTE MAXIMUM RATINGS (Note 1)

(TA = 25°C unless otherwise noted) Drain-Source or Drain-Gate Voltage

314 103404
3N16430V
Static Gate-Source Voltage
3N163±40V
3N164±30V
Transient Gate-Source Voltage (Note 2) ±125V
Drain Current
Storage Temperature65°C to +200°C

#### Operating Temperature ..... -55°C to +150°C Lead Temperature (Soldering, 10sec) ......+300°C Derate above +25°C ...............3.0mW/°C

#### NOTES:

- 1. See handling precautions on 3N170 data sheet.
- 2. Devices must not be tested at ±125V more than once, nor for longer than 300ms.

#### ELECTRICAL CHARACTERISTICS (@ 25°C and VBS = 0 unless noted)

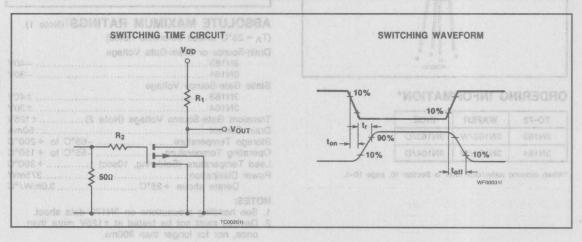
			3N163		3N164		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
IGSSR	Gate Reverse Leakage Current			10		10	
IGSSF	Gate Forward Current	V <sub>GS</sub> = -40V (3N163) V <sub>GS</sub> = -30V (3N164)		-10		-10	рА
GSSF	$T_A = +125^{\circ}C$	1 '43		-25		-25	
BVDSS	Drain-Source Breakdown Voltage	$I_D = -10\mu A$ , $V_{GS} = 0$	-40		-30		
BV <sub>SDS</sub>	Source-Drain Breakdown Voltage	$I_S = -10\mu A$ , $V_{GD} = 0$ , $V_{DS} = 0$	-40		-30		
V <sub>G</sub> S(th)	Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -10\mu A$	-2.0	-5.0	-2.0	-5.0	V
V <sub>G</sub> S(th)	Threshold Voltage	$V_{DS} = -15V$ , $I_{D} = -10\mu A$	-2.0	-5.0	-2.0	-5.0	
VGS	Gate Source Voltage	$V_{DS} = -15V$ , $I_{D} = -0.5mA$	-3.0	-6.5	-3.0	-6.5	
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0		200		400	
ISDS	Source Drain Current	V <sub>SD</sub> = 15V, V <sub>GS</sub> = V <sub>DB</sub> = 0		400		800	pA
rDS(on)	Drain-Source on Resistance	$V_{GS} = -20V$ , $I_{D} = -100 \mu A$		250		300	ohms
ID(on)	On Drain Current	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V	-5.0	-30.0	-3.0	-30.0	mA
9fs	Forward Transconductance		2000	4000	1000	4000	
9os .	Output Admittance	$V_{DS} = -15V$ , $I_{D} = -10$ mA, $f = 1$ kHz		250		250	μs

	101	minus sanding	3N	163	3N	164	(less 2
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
Ciss	Input Capacitance—Output Shorted			2.5		2.5	name in woman
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = -15V$ , $I_{D} = -10$ mA, $f = 1$ MHz		0.7		0.7	pF
Coss	Output Capacitance Input Shorted	(Note 1)	some b	3.0	uoni	3.0	

NOTE 1: For design reference only, not 100% tested.

#### SWITCHING CHARACTERISTICS (@ 25°C and VBS = 0)

SYMBOL	PARAMETER	TEST CONDITIONS	3N	163	3N	164	LIMIT	
STMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MAX UNIT	
ton	Turn-On Delay Time	V <sub>DD</sub> = -15V		12		12		
tr 8000 0000	Rise Time	I <sub>D(on)</sub> = -10mA (Note 1)		24	WE T	24	ns	
t <sub>off</sub>	Turn-Off Time	$R_G = R_L = 1.4k\Omega$	A SUR	50		50		



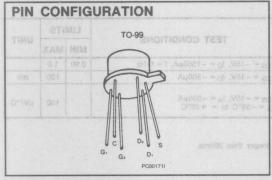
				ME			
TIMU	XAM	MARK	MASH				
							(dipeo)
				0.8-			
			400		Vsg = 18V, Vgs = Vps = 0		
						Drein-Source on Resistance	

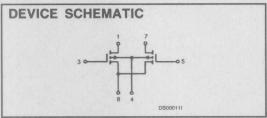
SYMBOL

#### Elliancement wode woore! **General Purpose Amplifier**

#### **FEATURES**

- Very High Impedance
- High Gate Breakdown Andrew gl Wat wagy
- Low Capacitance





#### CHIP TOPOGRAPHY NOTE: SUBSTRATE IS BODY. S/D 2 S/D 2 S/D 1 GATE 1-BODY S/D 1-

#### ABSOLUTE MAXIMUM RATINGS (Note 1)

(TA = 25°C unless otherwise specified)

Drain-Source or Drain-Gate Voltage (Note 2)	
3N165	40V
3N1653N166	30V
Transient Gate-Source Voltage (Note 3)	±125
Gate-Gate Voltage	±80V
Drain Current (Note 2)	50mA
Storage Temperature65°C to	+200°C
Operating Temperature55°C to	+150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	
One Side	.300mW
Both Sides	525mW

Total Derating above 25°C ...... 4.2mW/°C

#### **ORDERING INFORMATION\***

TO-99	WAFER	DICE
3N165	3N165/W	3N165/D
3N166	3N166/W	3N166/D

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

#### ELECTRICAL CHARACTERISTICS (@ 25°C and VBS = 0 unless noted)

avana.		TEST COMPLETIONS	LIN	IITS	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
IGSSR	Gate Reverse Leakage Current	V <sub>GS</sub> = 40V		10	
IGSSF	Gate Forward Leakage Current			-10	
	$T_A = +125^{\circ}C$	V <sub>GS</sub> = -40V		-25	pA
IDSS	Drain to Source Leakage Current	V <sub>DS</sub> = -20V		-200	
ISDS	Source to Drain Leakage Current	$V_{SD} = -20, V_{DB} = 0$		-400	
ID(on)	On Drain Current	$V_{DS} = -15V$ , $V_{GS} = -10V$	-5	-30	mA
V <sub>G</sub> S(th)	Gate Source Threshold Voltage	$V_{DS} = -15V$ , $I_{D} = -10\mu A$	-2	-5	
V <sub>GS(th)</sub>	Gate Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -10\mu A$	-2	-5	V
「DS(on)	Drain Source ON Resistance	$V_{GS} = -20V$ , $I_{D} = -100\mu A$		300	ohms
9fs	Forward Transconductance		1500	3000	
gos	Output Admittance	$V_{DS} = -15V$ , $I_{D} = -10mA$ , $f = 1kHz$		300	μs

#### 3N165, 3N166

#### **ELECTRICAL CHARACTERISTICS (CONT.)**



SYMBOL	PARAMETER	TEST CONDITIONS	304 3	MAX	UNIT
Ciss	Input Capacitance			3.0	
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA, f = 1MHz	-	0.7	pF
Coss	Output Capacitance	(Note 4)	edicit i	3.0	ToV 1
RE(Yfs)	Common Source Forward Transconductance	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA, f = 100MHz (Note 4	) 1200	NEEK I	μs

#### 3N165 MATCHING CHARACTERISTICS

OVIIDO:	s os Telegraphia	10-90-01	LIN	IITS	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Y <sub>fs1</sub> /Y <sub>fs2</sub>	Forward Transconductance Ratio	$V_{DS} = -15V$ , $I_{D} = -1500\mu A$ , $f = 1kHz$	0.90	1.0	
V <sub>GS1-2</sub>	Gate Source Threshold Voltage Differential	$V_{DS} = -15V$ , $I_D = -500\mu A$		100	mV
$\frac{\Delta V_{\text{GS1-2}}}{\Delta T} \text{old})  3.04$	Gate Source Threshold Voltage Differential Change with Temperature	$V_{DS} = -15V$ , $I_A = -500\mu A$ $T_A = -55^{\circ}C$ to $= +25^{\circ}C$		100	μV/°C

NOTES 1. See handling precautions on 3N170 data sheet.

2. Per transistor.
 3. Devices must not be tested at ±125V more than once, nor for longer than 300ms.
 4. For design reference only, not 100% tested.

Transient Catre-Source Voltage (Note 3) #125 Gain-Gate Voltage #80V Drain Current (Note 2) #80mA

	BOIG		
		SN165/W	
L	SM166/D		

	MU			
		TEST CONDITIONS	PARAMETER	
		V08 = 80V		nean
		V <sub>DB</sub> = -26V		
			Source to Drain Loskage Current	
		Au01 - = gl ,V81 - = agV	Cate Source Threshold Voltage	
		V <sub>GS</sub> = -20V, Ig = -100µA		
			Forward Transponductance	
		sHNr = 1 ,Am0r = - or ,Var = + eqv		

#### FEATURES

- Low Switching Voltages
- Fast Switching Times
- Low Drain-Source Resistance MADE = 1 VOE = PURCH

PIN CONFIGURATION

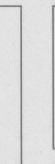
TO-72

Low Reverse Transfer Capacitance

#### HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

- 1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
- 2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
- 3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.



#### ORDERING INFORMATION\*

TO-72	WAFER	DICE
3N170	3N170/W	3N170/D
3N171	3N171/W	3N171/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY 1003 .0025 x .0029

#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Drain-Gate Voltage	±35V
Drain-Source Voltage	25V
Gate-Source Voltage	±35V
Drain Current	30mA
Storage Temperature Range65°C	to +200°C
Operating Temperature Range55°C	to +150°C
Lead Temperature (Soldering, 10sec)	+ 300°C
Power Dissipation	300mW
Derate above 25°C	2.4mW/°C

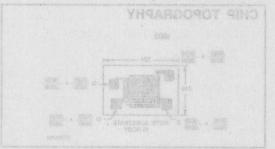
#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

	PARAMETER  Drain-Source Breakdown Voltage			LIN	IITS	UNIT
SYMBOL			TEST CONDITIONS	MIN	MAX	
BVDSS			$I_D = 10 \mu A, V_{GS} = 0$	25	-	٧
			$V_{GS} = -35V, V_{DS} = 0$		10	
IGSS	Gate Leakage Current	T <sub>A</sub> = 125°C			100	pA
IDSS	Zero-Gate-Voltage Drain Current		V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		10	nA
		T <sub>A</sub> = 125°C			1.0	μΑ
V <sub>GS(th)</sub>	Gate-Source 3N170		$V_{DS} = 10V, I_{D} = 10\mu A$	1.0	2.0	V
	Threshold Voltage	3N171		1.5	3.0	
I <sub>D(on)</sub>	"ON" Drain Current		V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	10		mA
V <sub>DS(on)</sub>	Drain-Source "ON" Voltage	е	I <sub>D</sub> = 10mA, V <sub>GS</sub> = 10V		2.0	V
rds(on)	Drain-Source ON Resistance	се	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0, f = 1.0kHz		200	Ω
Yfs	Forward Transfer Admittance		V <sub>DS</sub> = 10V, I <sub>D</sub> = 2.0mA, f = 1.0kHz	1000		μs

SYMBOL		\$ 2 CUT S 2 CUT S CUT S CUT S CUT S		LIMITS	
	PARAMETER SMOOTHLANDS OF THE PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Crss	Reverse Transfer Capacitance (Note 1)	V <sub>DS</sub> = 0, V <sub>GS</sub> = 0, f = 1.0MHz V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0, f = 1.0MHz		1.3	
Ciss	Input Capacitance (Note 1)			5.0	pF
C <sub>d(sub)</sub>	Drain-Substrate Capacitance (Note 1)	V <sub>D(SUB)</sub> = 10V, f = 1.0MHz	08-m	5.0	ro.J r
td(on)	Turn-On Delay Time (Note 1)	Transfer Capacitance	98791	3.0	(O.) P
tr	Rise Time (Note 1)	$V_{DD} = 10V, I_{D(on)} = 10mA,$ $V_{GS(on)} = 10V, V_{GS(off)} = 0,$		10	ns
td(off)	Turn-Off Delay Time (Note 1)			3.0	
thing semelor peu	Fall Time (Note 1) $R_G = 50\Omega$			15	

NOTE 1: For design reference only, not 100% tested.

Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.



#### ABSOLUTE MAXIMUM RATINGS

1A = 20 C emisses dinerwise frowd)	136V
Drain-Sate Voltage	25V
Drain-Source Voltage	25V
Gate-Source Voltage	136V
Drain Current	30mn
Storage Temperature Range	-55°C to +200°C
Coperating Temperature Range	-55°C to +300°C
Lead Temperature Soldering, 10sec)	200mw
Lead Temperature Soldering, 10sec)	200mw
Power Dissipation	200mw
Destite above 25°C	2.4mW/°C

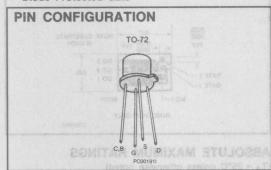


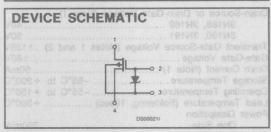
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

					CHANGE	
TOEWAS			TEST CONDITIONS		XAM	TINU
	Drain-Source Breakdown V	agaño	I to e tops, vag = 0			
	Zero-Gere-Voltage Drain Current Vps = 10V, Vqs		Vps = 10V, Vqs = 0			
			Augt = of .VGt = agV			
					2.0	

#### **FEATURES**

- High Input Impedance
- **Diode Protected Gate**





### CHIP TOPOGRAPHY 1503Z somi Sugar noth your B Zener Protec x \_.0029 S CT003111

#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted) Drain-Source or Drain-Gate Voltage 3N172...... 40V 3N173......30V Drain Current......50mA Gate Forward Current......10μΑ

Gate Reverse Current ......1mA Storage Temperature.....-65°C to +200°C Operating Temperature .....-55°C to +150°C Lead Temperature (Soldering, 10sec) ......+300°C Power Dissipation ......375mW Derate above 25°C......3.0mW/°C

#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
3N172	3N172/W	3N172/D
3N173	3N173/W	3N173/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### ELECTRICAL CHARACTERISTICS (@ 25°C and VBS = 0 unless noted)

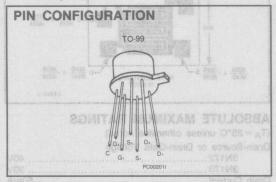
SYMBOL		005-		3N172		3N173		HOSE
		PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
Igss	Gate Reverse Current	V <sub>GS</sub> = -20V	MI GREEK	-200	IS OF	-500	pA	
1033		T <sub>A</sub> = +125°C	with 21 onestev much	Another 1	-0.5	FOS I	-1.0	μΑ
BVGSS	03-10	Gate Breakdown Voltage I <sub>D</sub> = -10μA		-40	-125	-30	-125	
BVDSS	0.8-10	Drain-Source Breakdown Voltage	$I_D = -10\mu A$	-40		-30		
BVSDS	aa- 10	Source-Drain Breakdown Voltage	$I_S = -10\mu A$ , $V_{DB} = 0$	-40	Source	-30		V
V <sub>GS(th)</sub>	- 200	Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = -10\mu A$	-2.0	-5.0	-2.0	-5.0	
* G5(III)		1004-	$V_{DS} = -15V$ , $I_{D} = -10\mu A$	-2.0	-5.0	-2.0	-5.0	
VGS	900	Gate Source Voltage	$V_{DS} = -15V$ , $I_{D} = -500\mu A$	-3.0	-6.5	-2.5	-6.5	
IDSS	0.00- 0	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0	Transa	-0.4	100	-10	
ISDS		Zero Gate Voltage Source Current	$V_{SD} = -15V$ , $V_{DB} = 0$ , $V_{GD} = 0$		-0.4		-10	nA
rDS(on)	I THE STATE OF	Drain Source On Resistance	$V_{GS} = -20V, I_D = -100\mu A$		250		350	ohms
ID(on)	THE ROLL	On Drain Current	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V	-5.0	-30	-5.0	-30	mA

#### 3N188-3N191 Dual P-Channel **Enhancement Mode MOSFET** General Purpose Amplifier Switch and January Island



#### **FEATURES**

- Very High Input Impedance
- High Gate Breakdown 3N190-3N191
- Zener Protected Gate 3N188-3N189
- Low Capacitance



#### ORDERING INFORMATION\*

TO-99	WAFER	DICE
3N188	0°88	
3N189		Sokieming, T
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### CHIP TOPOGRAPHY 2506 onabeqmi fuent rigiti NOTE: SUBSTRATE - 0025 - 0035 TYP IS BODY. TYP S/D 2 S/D 2 GATE 2 S/D 1 GATE 1-S/D 1-BODY 3N190, 3N191 ONLY CT003211

#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage (Note 1) 3N188, 3N189
3N188, 3N189 40V
3N190, 3N191 30V
Transient Gate-Source Voltage (Notes 1 and 2) ±125V
Gate-Gate Voltage±80V
Drain Current (Note 1)
Storage Temperature65°C to +200°C
Operating Temperature55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation
One Side300mW
Both Sides525mW
Total Derating above 25°C

#### ELECTRICAL CHARACTERISTICS (25°C and V<sub>BS</sub> = 0 unless otherwise noted)

SYMBOL		PARAMETER	TEST CONDITIONS		3N188 3N189		190 191	TIMU
		thefon easing 0	RISTICS (a 25°C and Vas.	MIN	MIN MAX MIN MAX		LECT	
IGSSR		Gate Reverse Current	V <sub>GS</sub> = 40V	and the same of the		and the second	10	
IGSSF	6.41	Gate Forward Current	VGS = -40V	ran-	-200		-10	рА
Goor	XARE	T <sub>A</sub> = 125°C	763		-200		-25	
BVDSS	1-508-1	Drain-Source Breakdown Voltage	$I_D = -10\mu A$	-40		-40		
BVSDS	10.1-1	Source-Drain Breakdown Voltage	$I_S = -10\mu A$ , $V_{BD} = 0$	-40		-40		388
	last-	06-   251-   08-	$V_{DS} = -15V$ , $I_D = -10\mu A$	-2.0	-5.0	-2.0	-5.0	V
VGS(th)		Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = -10\mu A$	-2.0	-5.0	-2.0	-5.0	PSGVI
VGS		Gate Source Voltage	$V_{DS} = -15V$ , $I_{D} = -500\mu A$	-3.0	-6.5	-3.0	-6.5	SCISA
IDSS	100-1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -15V	spatiely	-200	err .	-200	(m)8(0))
ISDS	0.6-	Source Drain Current	V <sub>SD</sub> = -15V, V <sub>DB</sub> = 0		-400		-400	pA
rDS(on)	9.8-	Drain-Source on Resistance	$V_{DS} = -20V$ , $I_{D} = -100\mu A$	BOY 93	300	- mid-e-	300	ohms
ID(on)		On Drain Current	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V	-5.0	-30.0	-5.0	-30.0	mA
amile	350	08 Au001 - = ot	Penichange Von = 20V	ACT OF	CARL OF	90	4	RCE

#### 3N188-3N191

NOYE is For design reference only, not 100% tosted

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

3N188-3N191  ELECTRICAL CHARACTERISTICS (CONT.)						2 - AND EL		
SYMBOL	PARAMETER AND A SHAPE	TEST CONDITIO	TEST CONDITIONS		3N188 3N189		190 191	UNIT
0.1111202			lisub ointils a extreme	MIN	MAX	MIN	MAX	Med for u
9fs	Forward Transconductance (Note 3)	es distribution	so agairre	1500	4000	1500	4000	currents
Yos	Output Admittance	and protection	f = 1kHz	ms gr	300	signa	300	μs μs
Ciss	Input Capacitance Output Shorted (Note 5)	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA	FIRST CONSTR	1819111	4.5	SQBX	4.5	SINU 10
Crss	Reverse Transfer Capacitance (Note 5)		f = 1MHz		1.5		1.0	pF
Coss	Output Capacitance Input Shorted (Note 5)			3/1/13	3.0	16317	3.0	14141

#### SWITCHING CHARACTERISTICS (@ 25°C and VBS = 0 unless noted)

SYMBOL		TEST CONDITIONS	LIN		
	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>d</sub> (on)	Turn On Delay Time	V <sub>DD</sub> = -15V, I <sub>D</sub> = -10mA	GMD	15	
t <sub>r</sub>	Rise Time	$R_G = R_L = 1.4k\Omega$ (Note 5)		30	ns
toff HEROTE	Turn Off Time	一		50	

#### MATCHING CHARACTERISTICS (@ 25°C and VBS = 0 unless noted) 3N188 and 3N190

SYMBOL	(TA = 25°C unless otherwise noted)		LIN		
	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Yfs1/Yfs2	Forward Transconductance Ratio	$V_{DS} = -15V$ , $I_D = -500\mu A$ , $f = 1kHz$	0.85	1.0	Series e
VGS1-2	Gate Source Threshold Voltage Differential	$V_{DS} = -15V$ , $I_D = -500\mu A$		100	mV
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	$V_{DS} = -15V$ , $I_{D} = -500 \mu A$ , $T = -55^{\circ}C$ to $+25^{\circ}C$	17	100	μV/°C
ΔVGS1-2	Gate Source Threshold Voltage Differential	$V_{DS} = -15V$ , $I_{D} = -500\mu A$	OL.	90	t Gi
$\Delta V_{GS1-2}$ $\Delta T$	Change with Temperature (Note 4)	$T = +25^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}$	water	100	μV/°C

NOTES: 1. Per transistor.

1. For datissured.

2. Approximately doubles for every 10°C increase in T<sub>A</sub>.

3. Pulse test duration = 300 µs; duty cycle ≤ 3%.

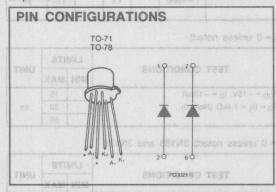
4. Measured at end points, T<sub>A</sub> and T<sub>B</sub>.

5. For design reference only, not 100% tested.



#### GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.



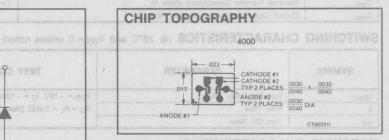
#### **ORDERING INFORMATION\***

T078	T071	WAFER	CHIP		
ID100	ID101	ID100/W	ID100/D		

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **FEATURES**

- IR = 0.1pA (Typical)
- BVR > 30V
- C<sub>rss</sub> = 0.75pF (Typical)



#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

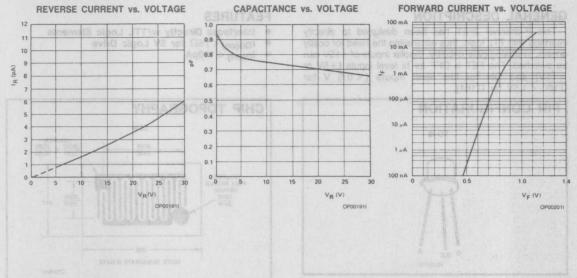
Diode Reverse Voltage 30V
Diode to Diode Voltage±50V
Forward Current
Reverse Current
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec) +300°C
Power Dissipation
Derate above 25°C2.4mW/°C

#### ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		tion = 300 us duty avois 5 3%.				
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VF	Forward Voltage Drop	I <sub>F</sub> = 10mA	0.8		1.1	V
BVR	Reverse Breakdown Voltage	$I_R = 1\mu A$				
IR	Reverse Leakage Current	V <sub>R</sub> = 1V		0.1		рА
'n	Tiovoiso Loakago outron			2.0	10	pri
	T <sub>A</sub> = 125°C	V <sub>R</sub> = 10V			10	nA
II <sub>R1</sub> -I <sub>R2</sub> I	Differential Leakage Current				3	рА
Crss	Total Reverse Capacitance	V <sub>R</sub> = 10V, f = 1MHz (Note 1)		0.75	1	pF

NOTE 1: For design reference only, not 100% tested.

#### TYPICAL PERFORMANCE CHARACTERISTICS



ABSOLUTE MAXIMUM RATINGS

TO-18 WAFER BICE 17:00 17:00/W 17:00/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

AX BEIN BEAK UNIT		xAm	TEST COMPITIONS	PARAMETER	JOBNY8 .	
					Drein Gureix	885
					Crain (OFF) Loakage	
				(1 srow) 0 = apy V03 - = apy		

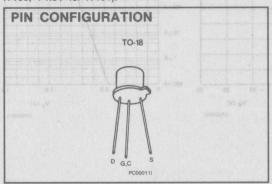
2-75

#### IT100, IT101 P-Channel JFET Switch



#### GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with TTL logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of  $\pm\,15V$  can be switched. The FET is OFF for hi level inputs (+5V or +15V) and ON for low level inputs (<0.5 V for IT100, <1.5V for IT101).



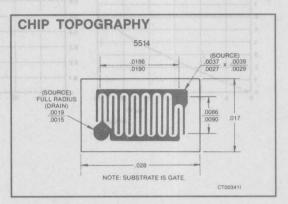
#### **ORDERING INFORMATION\***

TO-18	WAFER	DICE
IT100	IT100/W	IT100/D
IT101	IT101/W	IT101/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **FEATURES**

- Interfaces Directly w/TTL Logic Elements
- $r_{DS(on)} < 75\Omega$  for 5V Logic Drive
- ID(off) < 100pA



#### **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Source Voltage
Gate-Drain Voltage
Gate Current50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation
Derate above 25°C 2.4mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			IT	100	IT			
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT	
IDSS	Drain Current	V <sub>GS</sub> = 0, V <sub>DS</sub> = -15V	-10		-20		mA .	
Vp	Pinch Off Voltage	I <sub>D</sub> = 1nA, V <sub>DS</sub> = -15V	2	4.5	4	10		
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = 1\mu A, V_{DS} = 0$	35		35	HAT !	V	
IGSS	Gate Reverse Current	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0		200		200	рА	
9fs	Transconductance		8		8			
9os	Output Conductance	$V_{GS} = 0, V_{DS} = -15V$		1		1	mS	
ID(off)	Drain (OFF) Leakage	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 15V		-100		-100	рА	
rDS(on)	Drain-Source "ON" Resistance	$V_{GS} = 0$ , $V_{DS} = -0.1V$		75		60	Ω	
Ciss	Input Capacitance	V <sub>DG</sub> = -20V, V <sub>GS</sub> = 0 (Note 1)		35		35		
Crss	Reverse Transfer Capacitance	$V_{DG} = -10V$ , $I_{S} = 0$ (Note 1)		12	S all	12	pF	

NOTE 1: For design reference only, not 100% tested.

## IT120, IT122 Dual NPN

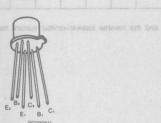
#### General Purpose Amplifier

#### FEATURES M XAM MIN XAM MIN XAM MIN XAM

- High he at Low Current
- Low Output Capacitance
- Good Matching
- Tight VBE Tracking

#### PIN CONFIGURATION

TO-71 TO-78



#### **ORDERING INFORMATION\***

ſ	TO-78	TO-71	WAFER	DICE
T	IT120	IT120-TO71	IT120/W	IT120/D
T	IT121	IT121-T071	IT121/W	IT121/D
T	IT122	IT122-TO71	IT122/W	IT122/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

## CHIP TOPOGRAPHY .0045 x .0045 .0035 x .0035 BASE #2 TYP 2 PLACES .0040 .0030 DIAMETER

EMITTER #2 TYP 2 PLACES .0030 DIAMETER

#### ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted)

BASE #1-

EMITTER#1-

[14] 사용하는 [1] 내용하는 사람이 내용하는 사람들이 되는 것이 되었다면 하는 사람들이 되었다면 하는 사람들이 되었다면 하는데 그렇게 되었다면 그렇게	
Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	. 50mA
Collector-Collector Voltage	60V
Storage Temperature Range65°C to +	-200°C
Operating Temperature Range55°C to +	
Lead Temperature (Soldering, 10sec)	-300°C

	ТО	-78	TO	-71
	ONE	BOTH SIDES	ONE	BOTH SIDES
Power Dissipation	250mW	500mW	200mW	400mW

25°C ...... 1.7mW/°C 3.3mW/°C 1.3mW/°C 2.7mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL		TEST CONDITIONS		IT120A		IT120		IT121		IT122		
	PARAMETER			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		$I_C = 10\mu A$ , $V_C$	E = 5.0V	200		200		80		80		2 6
hFE	DC Current Gain	I <sub>C</sub> = 1.0mA, V	CE = 5.0V	225		225	7	100		100	12.00	
	$T_{A} = -55^{\circ}C$	$I_C = 10\mu A, V_{CE} = 5.0V$		75		75		30		30		William.
V <sub>BE</sub> (ON)	Emitter-Base On Voltage				0.7		0.7	11/15	0.7		0.7	
V <sub>CE</sub> (SAT)	Collector Saturation Voltage	I <sub>C</sub> = 0.5mA, I <sub>B</sub> = 0.05mA			0.5	14	0.5	100	0.5		0.5	V
СВО	Collector Cutoff Current				1.0		1.0		1.0	NEW W	1.0	nA
	$T_A = +150$ °C	$I_E = 0$ , $V_{CB} = 45V$			10		10		10	1000	10	μΑ
IEBO	Emitter Cutoff Current	I <sub>C</sub> = 0, V <sub>EB</sub> =	5.0V		1.0		1.0		1.0		1.0	nA
C <sub>obo</sub>	Output Capacitance	I <sub>E</sub> = 0, V <sub>CB</sub> = 5.0V	f = 1MHz		2.0		2.0		2.0		2.0	
C <sub>te</sub>	Emitter Transition Capacitance	I <sub>C</sub> = 0, V <sub>EB</sub> = 0.5V	(Note 3)		2.5		2.5		2.5		2.5	pF
C <sub>C1</sub> ,C <sub>2</sub>	Collector to Collector Capacitance	V <sub>CC</sub> = 0			4.0		4.0		4.0		4.0	
I <sub>C1,C2</sub>	Collector to Collector Leakage Current	V <sub>CC</sub> = ±60V (Note 3)			10		10		10		10	nA

SYMBOL	PARAMETER	TEST CONDITIONS	IT120A		IT120		IT121		IT122		UNIT
	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CEO</sub> (SUST)	Collector to Emitter Sustaining Voltage	I <sub>C</sub> = 1.0mA, I <sub>B</sub> = 0	45		45	1	45	O WHO	45	इन्ते ।	٧
GBW	Current Gain Bandwidth Product (Note 3)	$I_C = 10 \mu A$ , $V_{CE} = 5V$ $I_C = 1 mA$ , $V_{CE} = 5V$	10 220		10 220		7 180	apac	7 180	DUD old da	MHz
IV <sub>BE1</sub> -V <sub>BE2</sub> I	Base Emitter Voltage Differential	I <sub>C</sub> = 10μA, V <sub>CF</sub> = 5.0V		1		2		3	81T ;	5	mV
11 <sub>B1</sub> -1 <sub>B2</sub> 1	Base Current Differential			2.5		5	MOTO !	25	0121	25	nA
$\frac{\Delta(V_{BE_1}-V_{BE_2})}{\Delta T}$	Base-Emitter Voltage Differential Change with Temperature	(Note 3) $T_A = -55^{\circ}C$ to +125°C $I_C = 10\mu A$ , $V_{CE} = 5.0V$		3		5		10		20	μV/°C

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 µA.

3. For design reference only, not 100% tested.

(T<sub>A</sub> = 25°C unless otherwise noted)

Collector-Base Voltage (Note 1) 45V
Collector-Entiter Voltage (Note 1) 45V
Collector-Current (Note 1) 57V
Collector-Collector Voltage (Note 1) 57V
Collector-Collector Voltage 65V
Storage Temperature Range 55°C to +200°C
Coperating Temperature Range 55°C to +200°C
Lead Temperature (Soldering 10sec) +300°C
Lead Temperature (Soldering 10sec) 70-78

TO-78 T0-78

CNE BOTH ONE BOTH
SIDE SIDES SIDE SIDES

TO-V8 TO-V1 WARER DICE

17120 17120-Y071 17120/W 17120/D

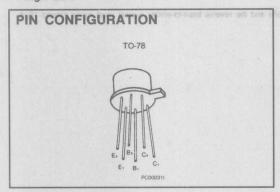
17121 17121-T0/1 17121/W 17121/D

17122 17122-Y071 17122/W 17122/D

ELECTRICAL CHARACTERISTICS (25°C unless cinemise noted)

	теят сомытлома				051TE						
							MIN				
		= 0.05mA									٧

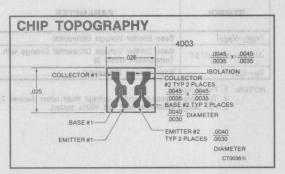
- Very High Gain
- Low Output Capacitance
- Tight VBE Matching
- High GBW



#### **ORDERING INFORMATION\***

TO-78	WAFER	DICE
IT124	IT124/W	IT124/D

\*When ordering wafer/dice refer to Section 10, page 10-1.



#### ABSOLUTE MAXIMUM RATINGS

ABOULD IL III/MIIIIOIII TITTITICO
(T <sub>A</sub> = 25°C unless otherwise noted)
Collector-Base Voltage (Note 1)2V
Collector-Emitter Voltage (Note 1)2V
Emitter-Base Voltage (Notes 1 and 2)7V
Collector-Current (Note 1)
Collector-Collector Voltage100V
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C
TO-78

ONE SIDE BOTH SIDES

 Power Dissipation
 300mW
 500mW

 Derate above 25°C
 2.4mW/°C
 4.0mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL				LIN			
	PARAME	TER	TEST CON	MIN	MAX	UNIT	
			$I_C = 1\mu A$ , $V_{CE} = 1V$	1500			
	DC Current Gain				1500		
		$T_A = -55$ °C	$I_{C} = 10 \mu A$ , $V_{CE} = 1 V$		600		
V <sub>BE</sub> (ON)	Emitter-Base "ON" Voltage	е				0.7	
V <sub>CE</sub> (SAT)	Collector Saturation Voltag	Collector Saturation Voltage		I <sub>C</sub> = 1mA, I <sub>B</sub> = 0.1mA			٧
Ісво	Collector Cutoff Current		I <sub>E</sub> = 0, V <sub>CB</sub> = 1V			100	pA
	$T_A = +150^{\circ}C$					100	nA
IEBO	Emitter Cutoff Current		$I_{C} = 0$ , $V_{EB} = 5V$			100	рА
Cobo	Output Capacitance (Note 3)  Emitter Transition Capacitance (Note 3)		I <sub>E</sub> = 0, V <sub>CB</sub> = 1V			0.8	pF
Cte			$I_{C} = 0$ , $V_{EB} = 0.5V$	f = 1MHz		1.0	
CC1C2	Collector to Collector Capacitance (Note 3)		$V_{CC} = 0$			0.8	
IC <sub>1</sub> C <sub>2</sub>	Collector to Collector Leakage Current		V <sub>CC</sub> = ±50V		250	pA	
GBW			$I_{C} = 10 \mu A$ , $V_{CE} = 1 V$	10		MHz	
	Current Gain Bandwidth Pr	roduct (Note 3)	$I_{C} = 100 \mu A, V_{CE} = 1 V$	100			
NF	Narrow Band Noise Figure (Note 3)		$I_C = 10\mu$ A, $V_{CE} = 3V$ , $f = 1$ kHz, $R_G = 10$ k $\Omega$ BW = 200Hz			3	dB
BVCBO	Collector-Base Breakdown	Voltage	$I_{C} = 10\mu A, I_{E} = 0$				v
BVEBO (Note 2)	Emitter-Base Breakdown Voltage		$I_E = 10 \mu A$ , $I_C = 0$	7			
V <sub>CEO</sub> (SUST)	Collector-Emitter Sustaining	Voltage	I <sub>C</sub> = 1mA, I <sub>B</sub> = 0				

2

# MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIN	IITS	UNIT
	VH9ARDOGOT GIHO	TEST CONDITIONS	TYP	MAX	
IV <sub>BE1</sub> -V <sub>BE2</sub> I	Base Emitter Voltage Differential	I <sub>C</sub> = 10μA, V <sub>CE</sub> = 1V	2	5	mV
$\Delta I(V_{\text{BE1}}-V_{\text{BE2}})I/\Delta T$	Base Emitter Voltage Differential Change with Temperature (Note 3)	I <sub>C</sub> = 10µA, V <sub>CE</sub> = 1V T = -55°C to +125°C	5	15	μV/°C
II <sub>B1</sub> -I <sub>B2</sub> If	Base Current Differential	$T_{C} = 10\mu A$ , $V_{CE} = 1V$	1 3 miles	.6	nA

NOTES:	4	Dor	transistor.
NUIES.		rei	transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 µA.

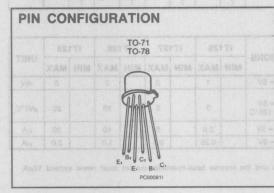
3. For design reference only, not 100% tested.

Collector to Collector Capacitance (						
Harrow Bland Noise Figure (Note 3)		IQ = 10μΑ, VCE = 2V,  1 = 1842, RG = 10κΩ  8W = 200Hz				

# IT126-IT129 Dual NPN General Purpose Amplifier

# **FEATURES**

- High Gain at Low Current
- Low Output Capacitance
- Tight IB Match
- Tight VBE Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers



### **ORDERING INFORMATION\***

TO78	TO-71	WAFER	DICE
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-T071	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT129/W	IT129/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# CHIP TOPOGRAPHY 4001 EMITTER .0033 .0039 .0039 TYP 2 PLACES .0030 x .0030 .0040 .0040 TYP 2 PLACES .0040 .004

#### **ABSOLUTE MAXIMUM RATINGS**

 (TA = 25°C unless otherwise specified)

 Collector-Base Voltage (Note 1)

 IT126, IT127
 60V

 IT128
 55V

 IT129
 45V

 Collector-Emitter Voltage (Note 1)
 60V

 IT126, IT127
 60V

 IT128
 55V

 IT129
 45V

 Emitter-Base Voltage (Notes 1 and 2)
 7.0V

 Collector Current (Note 1)
 100mA

 Collector-Collector Voltage
 70V

 Storage Temperature Range
 -65°C to +175°C

 Operating Temperature Range
 -55°C to +175°C

 Lead Temperature (Soldering, 10sec)
 +300°C

 T071
 T078

Power Dissipation	ONE	BOTH SIDES	ONE	BOTH SIDES
Total Dissipation at 25°C	200mW	400mW 2.7	250mW	500mW 3.3
Derating Factor	mW/°C	mW/°C	mW/°C	mW/°C

# ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			IT	126	IT	127	IT128		IT129		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		$I_{C} = 10 \mu A$ , $V_{CE} = 5V$	150		150		100		70		
		I <sub>C</sub> = 1.0mA, V <sub>CE</sub> = 5V	200	800	200	800	150	800	100		
h <sub>FE</sub>	DC Current Gain	I <sub>C</sub> = 10mA, V <sub>CE</sub> = 5V	230		230		170		115		
		I <sub>C</sub> = 50mA, V <sub>CE</sub> = 5V	100		100		75		50		
	$T_A = -55^{\circ}C$	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V	75		75		60		40		
V <sub>BE(on)</sub>	Emitter-Base On Voltage	I <sub>C</sub> = 10mA, V <sub>CE</sub> = 5V		0.9		0.9		0.9		0.9	
		I <sub>C</sub> = 50mA, V <sub>CE</sub> = 5V		1.0		1.0		1.0		1.0	٧
VCE(sat)	Collector Saturation Voltage	I <sub>C</sub> = 10mA, I <sub>B</sub> = 1mA		0.3	DO.	0.3		0.3		0.3	
		I <sub>C</sub> = 50mA, I <sub>B</sub> = 5mA		1.0		1.0		1.0		1.0	
СВО	Collector Cutoff Current	I <sub>E</sub> = 0, V <sub>CB</sub> = 45V, 30V*		0.1		0.1		0.1		0.1*	nA
	$T_A = +150^{\circ}C$			0.1		0.1		0.1		0.1*	μΑ
IEBO	Emitter Cutoff Current	I <sub>C</sub> = 0, V <sub>EB</sub> = 5V		0.1		0.1		0.1		0.1	nA

SYMBOL	DADAMETER	TEST CONDITIONS	IT126		IT127		IT128		IT129		UNIT
	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNI
C <sub>obo</sub>	Output Capacitance (Note 3)	I <sub>E</sub> = 0, V <sub>CB</sub> = 20V		3		3		3		3	pF
BVC <sub>1</sub> C <sub>2</sub>	Collector to Collector Breakdown Voltage	$I_C = \pm 1 \mu A$	±100		±100	#E15	±100	Spract Spract	±100	no n	For
VCEO(sust)	Collector to Emitter Sustaining Voltage	I <sub>C</sub> = 1mA, I <sub>B</sub> = 0	60		60		55	n didne	45	al in	V
BVCBO	Collector Base Breakdown Voltage	$I_C = 10\mu A, I_E = 0$	60	ot ani	60	Maria	55	Islosi	45	intos	
BVEBO	Emitter Base Breakdown Voltage	$I_{\rm E} = 10 \mu A, I_{\rm C} = 0$	7		7		7		7		

# MATCHING CHARACTERISTICS

CVMPOL	DADAMETED	TEST CONDITIONS	IT126		IT127		IT128		IT129		UNIT
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNII
IV <sub>BE1</sub> -V <sub>BE2</sub> I	Base Emitter Voltage Differential	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V		1		2		3		5	mV
$\frac{\Delta( V_{BE_1}-V_{BE_2} )}{\Delta T}$	Base Emitter Voltage Differential Change with Temperature (Note 3)	$I_C = 1$ mA, $V_{CE} = 5$ V $T_A = -55$ °C to $+125$ °C		3		5		10		20	μV/°C
I <sub>B1</sub> -I <sub>B2</sub>	Base Current Differential	$I_{C} = 10 \mu A, V_{CE} = 5V$		2.5	Ellis I	5	HILL	10		20	nA
26	GS:	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V		0.25		0.5	1 1 1 1	1.0		2.0	μΑ

NOTES: 1. Per transistor

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10µA.

3. For design reference only, not 100% tested.

ORDERING INFORMATION\*

	WAFER		
		17126-7071	FT126
		PARTITION !	
	WYSTTI		

ELECTRICAL CHARACTERISTICS (25°C notes officewee noted

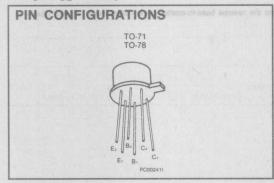
						(29		
PARAMETER			MISS		MBN			
	7.5							

# 2

# IT130-IT132 Dual PNP General Purpose Amplifier

# FEATURES XAM MIM XAM MIM XAM MIM

- High he at Low Current
- Low Output Capacitance
- Tight IB Match
- Tight VBE Tracking



#### **ORDERING INFORMATION\***

TO-78	TO-71	WAFER	DICE
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-T071	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# 

# **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise specified)	
Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	.7V
Collector Current (Note 1) 50	mA
Collector-Collector Voltage	60V
Storage Temperature Range65°C to +17	5°C
Operating Temperature Range55°C to +17	5°C
Lead Temperature (Soldering, 10sec)+30	0°C
TO-71 TO-78	

ONE	вотн	ONE	вотн
SIDE	SIDES	SIDE	SIDES

200mW 400mW 250mW 500mW

Power Dissipation ....... 1.3mW/°C 2.7mW/°C 1.7mW/°C 3.3mW/°C tunless otherwise noted)

			IT1	30A	IT	130	IT	131	IT	132	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		$I_C = 10 \mu A$ , $V_{CE} = 5.0 V$	200		200		80		80		
hFE	DC Current Gain	I <sub>C</sub> = 1.0mA, V <sub>CE</sub> = 5.0V	225		225		100		100		
	T <sub>A</sub> = -55°C	$I_C = 10 \mu A$ , $V_{CE} = 5.0 V$	75		75	100	30		30		
V <sub>BE</sub> (ON)	Emitter-Base On Voltage	$I_{C} = 10 \mu A$ , $V_{CE} = 5.0 V$		0.7	1	0.7		0.7		0.7	
V <sub>CE</sub> (SAT)	Collector Saturation Voltage	I <sub>C</sub> = 0.5mA, I <sub>B</sub> = 0.05mA		0.5		0.5		0.5		0.5	٧
ICBO	Collector Cutoff Current	IF = 0. VCB = 45V		-1.0	1,970	-1.0	1	-1.0		-1.0	nA
	$T_A = +150^{\circ}C$	E 0, 10B 401		-10		-10		-10		-10	μΑ
IEBO	Emitter Cutoff Current	I <sub>C</sub> = 0, V <sub>EB</sub> = 5.0V		-1.0		-1.0		-1.0		-1.0	nA
Cob (Note 3)	Output Capacitance	I <sub>E</sub> = 0, V <sub>CB</sub> = 5.0V		2.0		2.0		2.0	District of	2.0	
Cte (Note 3)	Emitter Transition Capacitance	I <sub>C</sub> = 0, V <sub>EB</sub> = 0.5V		2.5		2.5		2.5		2.5	\ pF
C <sub>C1-C2</sub> (Note 3)	Collector to Collector Capacitance	V <sub>CC</sub> = 0		4.0		4.0		4.0		4.0	
IC1-C2	Collector to Collector Leakage Current	V <sub>CC</sub> = ±60V		10		10		10		10	nA
V <sub>CEO</sub> (SUST)	Collector to Emitter Sustaining Voltage	I <sub>C</sub> = 1.0mA, I <sub>B</sub> = 0	-45		-45		-45		-45		V
GBW	Current Gain	$I_{C} = 10 \mu A$ , $V_{CE} = 5 V$	5		5		4		4		
GBW	Bandwidth Product (Note 3)	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V	110		110		90	BILL	90		MHz
IV <sub>BE1</sub> -V <sub>BE2</sub> I	Base Emitter Voltage Differential	$I_C = 10\mu A$ , $V_{CE} = 5.0V$		1		2		3 -		5	mV

# IT130-IT132

# **WINTERSIL**

# **ELECTRICAL CHARACTERISTICS (CONT.)**

ovuno.	DADAMETER	TEST COMPLETIONS	IT1	30A	IT	130	IT:	131	IT	132	111117
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
<sub>B1</sub> -  <sub>B2</sub>	Base Current Differential	$I_C = 10 \mu A$ , $V_{CE} = 5.0 V$		2.5		5	install.	25	1 900	25	nA
$\Delta (V_{BE_1} - V_{BE_2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature (Note 3)	$T_A = -55^{\circ}\text{C to } + 125^{\circ}\text{C}$ $I_C = 10\mu\text{A}, \ V_{CE} = 5.0\text{V}$		3		5	aneli	10	) ing sistif	20	μV/°C

NOTES: 1. Per transistor.

1. Per transistor. 2. The reverse base-to-emitter voltage must never exceed 7.0V, and the reverse base-to-emitter current must never exceed 10µA. 3. For design reference only, not 100% tested.



	17-07	

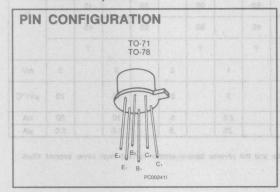
				181	182	
SYMBOL					XAM	
						39/

# IT136-IT139 Dual PNP General Purpose Amplifier

# **BINTERSIL**

# FEATURES MAN MAN MAN MAN MAN MAN MAN

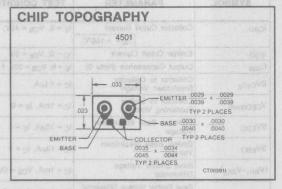
- High Gain at Low Current
- Low Output Capacitance
- Tight I<sub>B</sub> Match
- Tight VBE Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers



## **ORDERING INFORMATION\***

TO-78	TO-71	WAFER	DICE
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-T071	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

\*When ordering wafer/dice refer to Section 10, page 10-1.



# ABSOLUTE MAXIMUM RATINGS

 (TA = 25°C unless otherwise noted)

 Collector-Base Voltage (Note 1)

 IT136, IT137
 60V

 IT138
 55V

 IT139
 45V

 Collector-Emitter Voltage (Note 1)
 60V

 IT 138
 55V

 IT139
 45V

 Emitter Base Voltage (Notes 1 and 2)
 7V

 Collector Current (Note 1)
 100mA

 Collector-Collector Voltage
 70V

 Storage Temperature Range
 -65°C to +175°C

 Operating Temperature Range
 -55°C to +175°C

 Lead Temperature (Soldering, 10sec)
 +300°C

ONE	BOTH	ONE	BOTH
SIDE	SIDES	SIDE	SIDES
000 141	100 111	050 111	F00 -14/

TO-78

Power Dissipation ....... 200mW 400mW 250mW 500mW Derate above 25°C ... 1.3mW/°C 2.7mW/°C 1.7mW/°C 3.3mW/°C

TO-71

# ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

				IT	136	IT	137	IT	138	IT	139		
SYMBOL	PARA	METER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
			$I_{C} = 10 \mu A, V_{CE} = 5V$	150		150		100 70					
			I <sub>C</sub> = 1.0mA, V <sub>CE</sub> = 5V	150	800	150	800	100	800	800 70 800			
hFE	DC Current Ga	in	I <sub>C</sub> = 10mA, V <sub>CE</sub> = 5V	125	- 1	125	i de la	80		50			
			I <sub>C</sub> = 50mA, V <sub>CE</sub> = 5V	65		60		40		25			
		T <sub>A</sub> = 55°C	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V	75		75		60		40			
V <sub>BE(on)</sub>	Emitter-Base O	n Voltage	I <sub>C</sub> = 10mA, V <sub>CE</sub> = 5V		.9		.9		.9	MY	40 .9		
			IC = 50mA, VCE = 5V	5.77	1.0		1.0		1.0		1.0	V	
VCE(sat)	Collector Satura	ation Voltage	I <sub>C</sub> = 1mA, I <sub>B</sub> = .1mA		.3		.3		.3		.3		
			I <sub>C</sub> = 10mA, I <sub>B</sub> = 1mA		.6		.6	B 247	.6	S. Jan	.6		

		l I	**	100	11	101		100	- 11	100	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Ісво	Collector Cutoff Current	I <sub>E</sub> = 0, V <sub>CB</sub> = 45V, 30V*		0.1		0.1		0.1		0.1*	nA
	$T_A = +150^{\circ}C$			0.1		0.1	FIS III	0.1	3 368	0.1*	μΑ
IEBO	Emitter Cutoff Current	I <sub>C</sub> = 0, V <sub>EB</sub> = 5V		0.1		0.1	- SUPPLY S	0.1	alackak	0.1	nA
Cobo	Output Capacitance (Note 3)	IE = 0, VCB = 20V, f = 1MHz		3		3		3	rupu Y	3	pF
BV <sub>C1</sub> C <sub>2</sub>	Collector to Collector Breakdown Voltage	$I_C = \pm 1 \mu A$	±100	101	±100	tred	±100	elslo	±100	potrio	IsiQ .
VCEO(sust)	Collector to Emitter Sustaining Voltage	I <sub>C</sub> = 1mA, I <sub>B</sub> = 0	60	roomin series	60		55	Marine Marine	45		V
BV <sub>CBO</sub>	Collector Base Breakdown Voltage	$I_C = 10\mu A, I_E = 0$	60		60		55	Am.	45	116,35,3	N.V.
BVEBO	Emitter Base Breakdown Voltage	I <sub>E</sub> = 10μA, I <sub>C</sub> = 0	7		7		7.0		7		
IV <sub>BE1</sub> -V <sub>BE2</sub> I	Base Emitter Voltage Differential	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V		1		2	-	3		5	mV
ΔI(V <sub>BE1</sub> -V <sub>BE2</sub> )I/ΔT	Base Emitter Voltage Differential Change with Temperature (Note 3)	I <sub>C</sub> = 1mA, V <sub>CE</sub> = 5V T <sub>A</sub> = -55°C to + 125°C		3		5		10		20	μV/°C
II <sub>B1</sub> -I <sub>B2</sub> I	Base Current Differential	$I_{C} = 10 \mu A$ , $V_{CE} = 5V$		2.5		5	HI	10		20	nA
	Voltage (Note 1)	IC = 1mA, VCE = 5V		.25		.5	111 11	1.0	18.0	2.0	μΑ

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 µA.

3. For design reference only, not 100% tested.

DEDERING INFORMATION\*

11136/W	

TAY OF THE STORES CLARET

# ELECTRICAL CHARACTERISTICS (@ 25°C infless ofherwise noted)

				TI	881	TI.	
	50150		XA38				

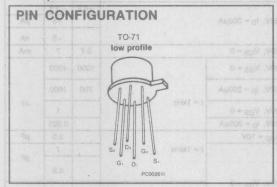
# IT500-IT505

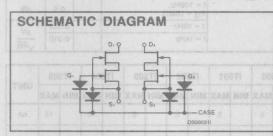
# Dual Cascoded N-Channel JFET General Purpose Amplifier



# GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low  $I_{\rm G}$  at high voltage levels, while giving high transconductance and very high common, mode rejection ratio.





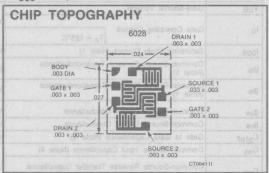
# ORDERING INFORMATION\*

TO-71	WAFER	DICE
IT500	IT500/W	IT500/D
IT501	IT501/W	IT501/D
IT502	IT502/W	IT502/D
IT503	IT503/W	IT503/D
IT504	IT504/W	IT504/D
IT505	IT505/W	IT505/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **FEATURES**

- C<sub>MRR</sub> > 120dB
- IG < 5pA @ 50VpG
- Crss < 0.5pF
- gos > .025μs



# ABSOLUTE MAXIMUM RATINGS

	ONE SIDE	BOTH SIDE
Power Dissipation (Note 3)	250mW	500mW
Derate above 25°C	3.8mW/°C	7.7mW/°C

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

NOTE 3. @ 85°C free air temp.

2-87

# IT500-IT505



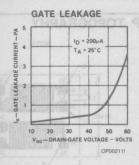
# ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

			LIN		
SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	MAX	UNIT
	Figure County	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0	Seed	-100	pA
IGSS	Gate Reverse Current T <sub>A</sub> = 125°C	$V_{GS} = -20V$ , $V_{DS} = 0$	amoo	-5	nA
BVGSS	Gate-Source Breakdown Voltage	$I_G = -1\mu A$ , $V_{DS} = 0$	-60	iri pai	in allriv
VGS(off)	Gate-Source Cutoff Voltage	$V_{DS} = 20V$ , $I_D = 1nA$	-0.7	-4	1 eVon
VGS	Gate-Source Voltage	RATION	-0.2	-3.8	5 25 S 455
	THANDON'S MIG	$V_{DG} = 50V$ , $I_{D} = 200\mu A$	PEGER I	-5	pA
IG	Gate Operating Current  TA = 125°C	10-71		-5	nA
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	0.7	7	mA
9fs	Common-Source Forward Transconductance (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	1000	4000	
9fs	Common-Source Forward Transconductance (Note 1)	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA	700	1600	
9os	Common-Source Output Conductance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		1	μs
9os	Common-Source Output Conductance	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA		0.025	
Cg1g2	Gate to Gate Capacitance (Note 4)	V <sub>G1</sub> = V <sub>G2</sub> = 10V		3.5	pF
Ciss	Common-Source Input Capacitance (Note 4)	f = 1MHz		7	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 3, 4)	4 6 -0 noseco4		0.5	pF
NF	Spot Noise Figure (Note 4)	$V_{DS} = 20V$ , $V_{GS} = 0$ $f = 100Hz$ , $R_G = 10M\Omega$		0.5	dB
	train-Source and Drain-Gate		W11	0.035	μV
ēn	Equivalent Input Noise Voltage (Note 4)	f = 1kHz		0.010	√Hz

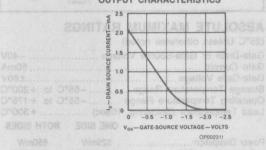
700S + 61 C		TEST CONDITIONS		IT500		IT501		IT502		IT	IT503		IT504		IT505	
SYMBOL	CHARACTERISTICS			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
IG1-IG2	Differential Gate Current	V <sub>DG</sub> = 20V, I <sub>D</sub> = 200μA	+ 125°C		5		5	(AD	5		5		10		15	nA
IDSS1	Saturation Drain Current Ratio (Note 1)	V <sub>DS</sub> = 20V, V	GS = 0V	0.95	1	0.95	1	0.95	19	0.95	A148	0.9	11/1	0.85	MB.	GRO
9fs1/9fs2	Transconductance Ratio (Note 1)	notalement to rion aint of se	f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1	DT
V <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate-Source Voltage	in ment Ofes wi	a e grou		5		5		10	15:00	15	-NA!	25		50	mV
ΔV <sub>GS1</sub> -V <sub>GS2</sub>	Gate-Source Differential Voltage	$V_{DG} = 20V$ $I_{D} = 200 \mu A$	T <sub>A</sub> = 25°C T <sub>B</sub> = 125°C		5		10		20	NSO	40	W	100		200	TI F
ΔΤ	Change with Temp. (Note 2, 4)		$T_A = -55$ °C $T_B = 25$ °C		5		10		20	1/80	40	, Vy	100		200	μ\/°(
C <sub>MRR</sub> **	Common Mode Rejection Ratio (Note 4)	Δ V <sub>DD</sub> = 10V	, I <sub>D</sub> = 200μA	120		120		120		120	m	120	2081	120	508	dB

<sup>\*\*</sup>  $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{gs1} - V_{gs2}], \ \Delta V_{DD} = 10 / -20 V_{gs1} / 20 V_{gs2}$ 

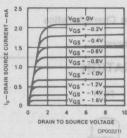
NOTES: 1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, T<sub>A</sub> and T<sub>B</sub>.
3. With case guarded C<sub>rss</sub> is typically < 0.15pF.
4. For design reference only, not 100% tested.



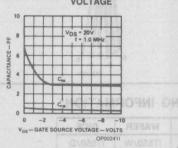




**OUTPUT CHARACTERISTICS** 



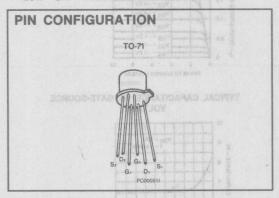
# TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE



2

# **FEATURES**

- Specified Matching Characteristics
- High Gain
- Low "ON" Resistance



# **ORDERING INFORMATION\***

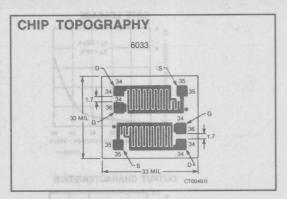
TO-71	WAFER	DICE
IT550	IT550/W	IT550/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS (25°C unless otherwise noted)

			LIN	IITS	UNIT	
SYMBOL	PARAMETER	TEST CO	MIN	MAX		
IGSSR	Gate-Reverse Current	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0		-100	рА	
	T <sub>A</sub> = 150°C				-200	mA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$		-40		
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1nA V <sub>DS</sub> = 0V, I <sub>G</sub> = 2mA		-0.5	-3	V
V <sub>GS(f)</sub>	Gate-Source Voltage				1.0	
Ipss	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		5	30	mA
rDS(on)	Static Drain Source ON Resistance	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0			100	Ω
9fs	Common-Source Forward		f = 1kHz	7500	12,500	
	Transconductance (Note 1)		f = 100MHz (Note 4)	7000		μs
9os	Common-Source Output Conductance		f = 1kHz		45	Maly
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	V <sub>DG</sub> = 15V, I <sub>D</sub> = 2mA	f = 1MHz		3	
Ciss	Common-Source Input Capacitance		(Note 4)		12	pF
NF	Spot Noise Figure (Note 4)		f = 10Hz, R <sub>g</sub> = 1M		1.0	dB
e <sub>n</sub>	Equivalent Short Circuit Input Noise Voltage (Note 4)		f = 10Hz		50	nV √Hz
I <sub>DSS1</sub>	Saturation Drain Current Ratio (Notes 1, 2)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0		0.95	1	_



# ABSOLUTE MAXIMUM RATINGS

ADOCEOTE MAXIMOM	115411114016	
(25°C Unless otherwise noted)		
Gate-Drain or Gate-Source Vol Gate Current		
Gate-Gate Voltage		±80V
Storage Temperature Range	65	°C to +200°C
Operating Temperature Range Lead Temperature (Soldering,		
Wiley - Souther Vertice - Vertic	ONE SIDE	BOTH SIDES
Power Dissipation		650mW 4.3mW/°C

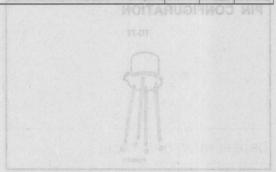
		The second control of	LIN	35 7 E Fast	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
IV <sub>GS1</sub> -V <sub>GS2</sub> I	Differential Gate-Source Voltage	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA		50	mV
ΔIV <sub>GS1</sub> -V <sub>GS2</sub> I ΔT	Gate-Source Voltage Differential Drift (Note 3)	$(T_A = -55^{\circ}C \text{ to } + 125^{\circ}C)$	onulais Voitage	100	μV/°C
9fs1 9fs2	Transconductance Ratio (Notes 1, 2)	V <sub>DS</sub> = 15V, I <sub>D</sub> = 2mA f = 1kHz	0.90	Input	

NOTES:	1.	Pulse	test	required:	pulse	width	300 us.	duty	cycle ≤ 3%.

2. Assumes smaller value in numerator.

Measured at end points T<sub>A</sub> and T<sub>B</sub>.
 For design reference only, not 100% tested.

20 , 200 Q - 313 5120 S 370 W - 2 800 V 000



# SEPHIAM MUMIAMER STUJUGGA

ORDERING. INFORMATION\*
TO-72 WAFER DICE
IT1700 IT1700/W IT1700/D

LECTRICAL CHARACTERISTICS gas otherwise noted. Vac = 0 unless otherwise noted

XAM	TEST CONDITIONS		
	Vos = -15V, ID = 0 I = 1MHz (Note 3)		

\*\*Control must not be tested at 1 (25V more than once nor longer than 300ms.
 \*\*Actual gate current is emmeasurable. Package suppliers are required to guarantee a package teckage of 10pA. External package teakage is one command more which is sensitive to both standard and datage environment, which cannot be guaranteed.

2

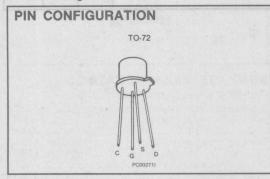
# P-Channel

# **Enhancement Mode MOSFET General Purpose Amplifier**



#### **FEATURES**

- Low ON-Resistance
- High Gain
- Low Noise Voltage
- High Input Impedance
- Low Leakage



#### **ORDERING INFORMATION\***

TO-72	WAFER	DICE
IT1700	IT1700/W	IT1700/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# CHIP TOPOGRAPHY NOTE: SUBSTRATE IS BODY CT004211

# **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Drain-Source and Gate-Source Voltage	-40V
Peak Gate-Source Voltage (Note 1)	125V
Drain Current	50mA
Storage Temperature65°C to +	200°C
Operating Temperature Range55°C to +	150°C
Lead Temperature (Soldering, 10sec)+	300°C
Power Dissipation3	75mW
Derate above 25°C	W/°C

# ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), VBS = 0 unless otherwise noted.

			LIN	IITS	110.000	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
BVDSS	Drain to Source Breakdown Voltage	$V_{GS} = 0$ , $I_D = -10\mu A$	-40		٧	
BV <sub>SDS</sub>	Source to Drain Breakdown Voltage	$V_{GS} = 0$ , $I_{D} = -10\mu A$	-40	22.8	٧	
Igss	Gate Leakage Current		(	See not	e 2)	
IDSS	Drain to Source Leakage Current			200	рА	
IDSS (150°C)	Drain to Source Leakage Current	V <sub>GS</sub> = 0, V <sub>DS</sub> = -20V		0.4	μΑ	
ISDS	Source to Drain Leakage Current			400	pA	
I <sub>SDS</sub> (150°C)	Source to Drain Leakage Current			0.8	μΑ	
V <sub>GS</sub> (th)	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -10\mu A$	-2	-5	٧	
rDS(on)	Static Drain to Source "on" Resistance	V <sub>GS</sub> = -10V, V <sub>DS</sub> = 0		400	ohms	
I <sub>DS</sub> (on)	Drain to Source "on" Current	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -15V	2		mA	
9fs	Forward Transconductance Common Source	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA f = 1kHz	2000	4000	μs	
C <sub>iss</sub>	Small Signal, Short Circuit, Common Source, Input Capacitance	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA f = 1MHz (Note 3)		5	pF	
C <sub>rss</sub>	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance	V <sub>DG</sub> = -15V, I <sub>D</sub> = 0 f = 1MHz (Note 3)		1.2	pF	
Coss	Small Signal, Short Circuit, Common Source, Output Capacitance	V <sub>DS</sub> = -15V, I <sub>D</sub> = -10mA f = 1MHz (Note 3)		3.5	pF	

NOTES: 1. Device must not be tested at ±125V more than once nor longer than 300ms.

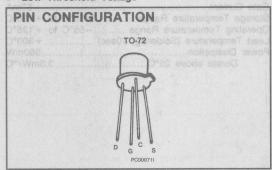
2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

3. For design reference only, not 100% tested.



#### **FEATURES**

- Low ON Resistance
   AMARIXAM STUROSTA
- Low Cdg
- High Gain
- Low Threshold Voltage



# **ORDERING INFORMATION\***

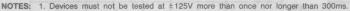
TO-72	WAFER	DICE
IT1750	IT1750/W	IT1750/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

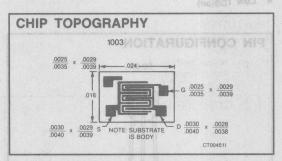
#### **ELECTRICAL CHARACTERISTICS**

(TA = 25°C, Body connected to Source and VBS = 0 unless otherwise noted)

A.H.O	CONTRACTOR AND A STATE OF THE S	a control	LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>G</sub> S(th)	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 10\mu A$	0.50	1.5	3.0	٧
IDSS	Drain Leakage Current	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		0.1	10	nA
IGSS	Gate Leakage Current	See note 2				
BVDSS	Drain Breakdown Voltage	$I_D = 10 \mu A$ , $V_{GS} = 0$	25	(5) (0) (-)	MI	V
rDS(on)	Drain To Source on Resistance	V <sub>GS</sub> = 20V	1000	25	50	ohms
ID(on)	Drain Current	V <sub>DS</sub> = V <sub>GS</sub> = 10V	10	50	150	mA
Yfs	Forward Transadmittance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA, f = 1kHz	3,000	islande de Ceta	afil an	μs
Ciss	Total Gate Input Capacitance	I <sub>D</sub> = 10mA, V <sub>DS</sub> = 10V, f = 1MHz (Note 3)		5.0	6.0	pF
Cdg	Gate to Drain Capacitance	V <sub>DG</sub> = 10V, f = 1MHz (Note 3)	110 e	1.3	1.6	pF



- 2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
- 3. For design reference only, not 100% tested.



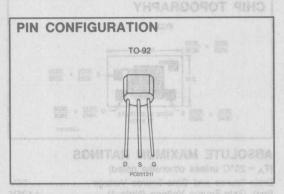
# **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)	
Drain-Source and Gate-Source Voltage	25V
Peak Gate-Source Voltage (Note 1)	±125V
Drain Current	100mA
Storage Temperature Range65°C to	+200°C
Operating Temperature Range55°C to	+150°C
Lead Temperature (Soldering, 10sec)	
Power Dissipation	.375mW
Derate above 25°C	3mW/°C

2

#### **FEATURES**

· Low rps(on)



#### **ORDERING INFORMATION\***

J105	TO-92 only
J106	TO-92 only
J107	TO-92 only

\*When ordering wafer/dice refer to Section 10, page 10-1.

# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted

average.		Chaton	astronitio	saein	J105			J106		J107			LIMIT
SYMBOL	PARAMETER	TEST CON	TEST CONDITIONS			MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Igss	Gate-Reverse Current (Note 1)	V <sub>DS</sub> = 0V, V <sub>GS</sub> =			-3	P	BYRM	-3			-3	nA	
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 5V, I <sub>D</sub> = 1	1μΑ	-4.5		-10	-2		-6	-0.5	And the second	-4.5	( constitute)
BVGSS	Gate-Source Breakdown Voltage	V <sub>DS</sub> = 0V, I <sub>G</sub> =	-25	gV		-25		Inensi	-25	ou one		٧	
IDSS	Drain Saturation Current (Note 2)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V		500			200		Inema	100	ed sie		mA
ID(off)	Drain Cutoff Current (Note 1)	V <sub>DS</sub> = 5V, V <sub>GS</sub> :	= -10V	705 × g	ev	3		prietris	30	Sound	oT class	3	nA
rDS(on)	Drain source ON Resistance	V <sub>DS</sub> ≤ 0.1V, V <sub>GS</sub>	S = 0V	Will to g	GW I	3			6	Injen	A RIST	8	Ω
Cdg(off)	Drain Gate OFF Capacitance	V <sub>DS</sub> = 0V,	Vor Fagy,	Amilit -		35		sonst	35	ugal ea	elai Ga	35	2.0
C <sub>sg(off)</sub>	Source Gate OFF Capacitance	V <sub>GS</sub> = -10V (Note 3)	1 1 1 1 1 1	/01 = g	ovi	35		901	35	Digin 4	of otea	35	pF
C <sub>dg(on)</sub> + C <sub>sg(on)</sub>	Drain Gate plus Source Gate ON Capacitance	(Note 3) V <sub>DS</sub> = V <sub>GS</sub> = 0V	f = 1MHz	of war a or she i ound oth	igna na indingua id at e	160	isav ista. Pa inioh ia	tu be mustern e otrom	160	on tea a current the det	vicos n tual gos kiego le	160	8970
t <sub>d</sub> (on)	Turn On Delay Time	Switching Time- Conditions (Note	3)		15	L LUCIO		15	110 501	digital	15	17.6	4
tr	Rise Time	J105			20			20			20		
t <sub>d</sub> (off)	Turn Off Delay Time		1.5V 1.5V -7V -5V		15			15	The Ja		15		ns
t <sub>f</sub>	Fall Time	R <sub>L</sub> 50Ω 50Ω 50Ω			20	17,117		20			20		

NOTES: 1. Approximately doubles for every 10°C increase in TA.

Pulse test duration = 300 µs; duty cycle ≤ 3%.
 For design reference only, not 100% tested.

# APPLICATIONS

- Analog Switches
- Choppers
- Commutators

# ABSOLUTE MAXIMUM RATINGS

(T <sub>A</sub> = 25°C unless otherwise noted)	initi e
Gate-Drain or Gate-Source Voltage	25V
Gate Current	50mA
Storage Temperature Range55°C to -	+ 150°C
Operating Temperature Range55°C to -	
Lead Temperature (Soldering, 10sec)	
Power Dissination	

Derate above 25°C......3.3mW/°C

2-94

# J111-J113 N-Channel JFET Switch

# **BINTERSIL**

# FEATURES

- . Low Cost TYT MIM XAM SYT MIM XAM SYT MIM
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltage Generated By Closed Switch
  - Purely Resistive
  - High Isolation Resistance From Driver
- Fast Switching
- Short Sample and Hold Aperture Time

# PIN CONFIGURATION TO-92 PEDDI S G PC001311

## **ORDERING INFORMATION\***

TO-92	WAFER	DICE
J111	J111/W	J111/D
J112	J112/W	J112/D
J113	J113/W	J113/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

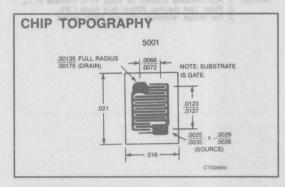
# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted

		TEST CONDITIONS		J111			J112			J113			UNIT
SYMBOL	PARAMETER	TEST CO	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
IGSSR	Gate Reverse Current (Note 1)	se Current $V_{DS} = 0V$ , $V_{GS} = -15V$				-1			-1			-1	nA
VGS(off)	Gate Source Cutoff Voltage	V <sub>DS</sub> = 5V, I <sub>D</sub> =	1μΑ΄.	-3		-10	-1		-5	-0.5		-3	
BVGSS	Gate Source Breakdown Voltage	VDS = OV, IG =	-35			-35			-35			٧	
IDSS	Drain Saturation Current (Note 2)	V <sub>DS</sub> = 15V, V <sub>G</sub>	20			5			2			mA	
ID(off)	Drain Cutoff Current (Note 1)	V <sub>DS</sub> = 5V, V <sub>GS</sub>			1			1			1	nA	
rDS(on)	Drain Source ON Resistance	V <sub>DS</sub> = 0.1V, V <sub>0</sub>	GS = OV			30			50			100	Ω
C <sub>dg(off)</sub>	Drain Gate OFF Capacitance	V <sub>DS</sub> = 0V,				5			5			5	
C <sub>sg(off)</sub>	Source Gate OFF Capacitance	V <sub>GS</sub> = -10V (Note 3)				5			5			5	pF
C <sub>dg(on)</sub> + C <sub>sg(on)</sub>	Drain Gate Plus Source Gate ON Capacitance	V <sub>DS</sub> = V <sub>GS</sub> = 0 (Note 3)			28			28			28		

# **APPLICATIONS**

- Analog Switches
- Choppers
- Commutators



## ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage35V
Gate Current 50mA
Storage Temperature Range55°C to +150°C
Operating Temperature Range55°C to +135°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation360mW
Derate Above 25°C

# J111-J113



# **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL		PLACETAGE IDELA		J111			J112			J113		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t <sub>d(on)</sub>	Turn On Delay Time	Switching Time Test Conditions (Note 3)		7			7	Pack	DECLINE	7	BERN A	NIA
tr	Rise Time	J111 J112 J113		6	VB. 0	elate	6	paliol	1071	6	eatto	old
td(off)	Turn Off Delay Time	V <sub>DD</sub> 10V 10V 10V	The first	20			20		4503	20	1101	ns
tf	Fall Time	$V_{GS(off)} -12V -7V -5V$ $R_L 0.8kΩ 1.6kΩ 3.2kΩ$		15	101	n Ort	15	onate	89FL	15	gir ts	H- 3

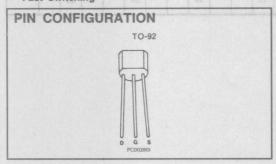
Approximately doubles for every 10°C increase in T<sub>A</sub>.
 Pulse Test duration 300µs; duty cycle ≤ 3%.
 For design reference only, not 100% tested.



							Vps = 5V, Vps = -10V			
								Diam, Source ON Resistance		

# **FEATURES**

- Low Insertion Loss
- No Offset or Error Generated By Closed Switch
   Purely Resistive
- High Isolation Resistance From Driver
- Short Sample and Hold Aperture Time
- Fast Switching



#### **ORDERING INFORMATION\***

TO-92	WAFER	DICE
J17X	J17X/W	J17X/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

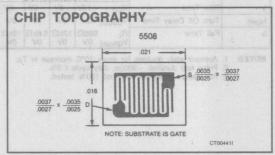
### **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted

CVMDOL	DADAMETER	TEST 00	NDITIONS		J174			J175			J176			J177		UNIT
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Igss	Gate Reverse Current (Note 1)	V <sub>DS</sub> = 0, V <sub>GS</sub> = 2			1			1			1			1	nA	
V <sub>GS(off)</sub>	Gate Source Cutoff Voltage	V <sub>DS</sub> = -15V, I <sub>D</sub> =	$V_{DS} = -15V, I_{D} = -10nA$			10	3		6	1		4	0.8		2.25	
BVGSS	Gate Source Breakdown Voltage	$V_{DS} = 0$ , $I_{G} = 1 \mu a$	30			30			30			30			V	
IDSS	Drain Saturation Current (Note 2)	$V_{DS} = -15V, V_{GS}$	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	
I <sub>D(off)</sub>	Drain Cutoff Current (Note 1)	$V_{DS} = -15V$ , $V_{GS}$			-1			-1			-1			-1	nA	
「DS(on)	Drain-Source ON Resistance	V <sub>GS</sub> = 0, V <sub>DS</sub> = -	-0.1V			85			125			250			300	Ω
C <sub>dg(off)</sub>	Drain-Gate OFF Capacitance				5.5			5.5			5.5			5.5		
C <sub>sg(off)</sub>	Source-Gate OFF Capacitance	V <sub>DS</sub> = 0, V <sub>GS</sub> = 10V			5.5			5.5			5.5			5.5		
C <sub>dg(on)</sub> + C <sub>sg(on)</sub>	Drain-Gate Plus Source Gate ON Capacitance	$V_{DS} = V_{GS} = 0$	f = 1MHz (Note 3)		40			40			40			40		pF

# **APPLICATIONS**

- Analog Switches
- Choppers
- Commutators



# **ABSOLUTE MAXIMUM RATINGS**

 $(T_A = 25$ °C unless otherwise noted)

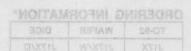
Gate-Drain or Gate-Source Voltage			30V
Gate Current			50mA
Storage Temperature Range!	55°C	to	+150°C
Operating Temperature Range!			
Lead Temperature (Soldering, 10sec)			300°C
Power Dissipation			.350mW
Derate above 25°C		3.	3mW/°C

l avarage		-	- DIMPORTADA DE DES				0114 0110					J1/0			Liker			
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
td(on)	Turn On Delay Time	Switching Time					2	BWB	bea	5	1 By	elst	15	2 10	1	20	effo	014 4
		(Note 3) J174 J	11/5	11/6	J177		11111							9	Ville	1900	reity	19
tr	Rise Time	VDD -10V -	-6V	-6V	-6V		5			10	SHOY	<b>19</b> 90	20	Sas R	noi	25	ring	ns
td(off)	Turn Off Delay Time	VGS(off) 12V	8V	3V-	3V	us si	5			10	531/3	negá	15	H 13	18 0	20	3 77	aug a
tf	Fall Time ease	R <sub>L</sub> 560Ω 1 V <sub>GS(on)</sub> 0V	0V	5.6kΩ 0V	10kΩ 0V		10			20	n per constant	and processing the	20		50	25	1 24	e Fau

NOTES: 1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration -300μs; duty cycle ≤ 3%.
3. For design reference only, not 100% tested.





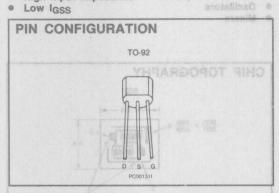


			ATTL		9111		1176			
PARAMETER			SYT					KAM	TYP	
Gate Reverse Gurrent (Note-1)										
		8				8				
								260		
							6.8			
					a.a					

# **General Purpose Amplifier**

#### **FEATURES**

- High Input Impedance
- · Low Igss



\* VHF/UHF Amplifiers

# ORDERING INFORMATION\*

TO-92	WAFER	DICE
J201	J201/W	J201/D
J202	J202/W	J202/D
J203	J203/W	J203/D
J204	J204/W	J204/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

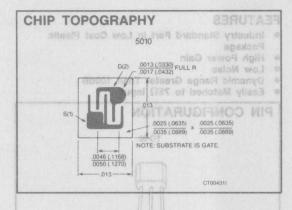
# ELECTRICAL CHARACTERISTICS

			NIDITION O		J201			J202			J203	3		J204		
SYMBOL	PARAMETER	TEST CO	TEST CONDITIONS			MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
IGSS	Gate Reverse Current (Note 1)	V <sub>DS</sub> = 0, V <sub>GS</sub>	= -20V			-100	igdor.	peli	-100	38	lens	-100	rRIFE:	DITK	-100	pA
V <sub>GS(off)</sub>	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub>	= 10nA 8006	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	-0.3		-2.0	110000000
BVGSS	Gate-Source Breakdown Voltage	V <sub>DS</sub> = 0, I <sub>G</sub> =	1µAM SYT	-40		MUN I	-40	2 11		-40	Hall	.380.54	-25		aca	V
IDSS	Saturation Drain Current (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		0.2		1.0	0.9	JAIRT CI	4.5	4.0	BODN.	20	0.2	1.2	3.0	mA
lg	Gate Current (Note 1)	VDG = 20V, ID	$V_{DG} = 20V, I_D = 200 \mu A$				100	-3.5	# 8DY		-3.5	3O 683	aven	-3.5		рА
9fs	Common-Source Forward Transconductance (Note 2)	V <sub>DS</sub> = 20V,	f = 1kHz	500			1,000	104	= anV	1,500	S? ==	AII.	500	1,500		118
9os	Common Source Output Conductance	V <sub>GS</sub> = 0	E.5 (M.)		- 1			3.5	P = G		10	nexiO	notio	2.5		μs
Ciss	Common-Source Input Capacitance	18			4		-	4	Yas P		4	- 100	()	4		880
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	000.00	f = 1MHz (Note 3)	050	1			Am	1 - 01	bi	1	eshpo	G-non	adoV		pF
ē <sub>n</sub>	Equivalent Short-Circuit Input Noise Voltage	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0	f = 1kHz (Note 3)		5			5	= enV		5	egrupe	E-mon	10		nV √Hz

NOTES: 1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration = 2ms.

3. For design reference only, not 100% tested.





#### ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage40V
Gate Current50mA
Storage Temperature Range55°C to +150°C
Operating Temperature Range55°C to +135°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation
Derate above 25°C 3.3mW/°C

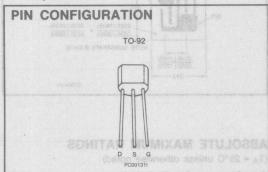
# J308-J310 N-Channel JFET High Frequency Amplifier

# **BINITERSIL**

e High Input Impedance

# FEATURES YHPARDOPOT 91HO

- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater Than 100dB
- Easily Matched to 75Ω Input



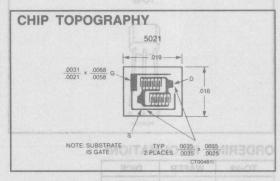
# **ORDERING INFORMATION\***

TO-92	WAFER	DICE
J30X	J30X/W	J30X/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# **APPLICATIONS**

- VHF/UHF Amplifiers
- Oscillators
- Mixers



### ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted)

Drain-Gate Voltage	25V
Drain-Source Voltage	
Continuous Forward Gate Current	10mA
Storage Temperature Range55°C to	+150°C
Operating Temperature Range55°C to	+135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	.360mW
Derate above 25°C	7mW/°C

# ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

0.9-	2.0 10.01 0.5	0.34 9.04 8	E.0-	J308	Astill =		rolucy is	080 00V	UNIT				
SYMBOL	PARAMETER	TEST CONDIT	IONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
BVGSS	Gate-Source Breakdown Voltage	$I_G = -1\mu A$ , $V_{DS} = 0$	0.5	-25		0 = 86	-25	= agV	tners.	-25	noffen	Sat	٧
Igss	Gate Reverse Current	$V_{GS} = -15V$ ,			A	-1.0	WEST IN	L real	-1.0	(fels) to	emo C	-1.0	nA
	T <sub>A</sub> = 125°C	V <sub>DS</sub> = 0				-1.0	North Co.		-1.0	R Soule	3-1000	-1.0	μΑ
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA		-1.0		-6.5	-1.0		-4.0	-2.0	a mome	-6.5	٧
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		12		60	12		30	24	ernetruis 2-nema	60	mA
VGS(f)	Gate-Source Forward Voltage	V <sub>DS</sub> = 0, I <sub>G</sub> = 1mA			10	1.0			1.0	2	O Annual	1.0	٧
9fs	Common-Source Forward Transconductance			8,000		20,000	10,000		20,000	8,000	O replan	18,000	9201
gos	Common-Source Output Conductance	V <sub>DS</sub> = 10V			- 14	200	, von	# 80 Y	200	gatloV	Resold is	200	
9fg	Common-Gate Forward Transconductance	I <sub>D</sub> = 10mA	= 1kHz		13,000	oanuous kon	9 0°01	13,000	of seld	200 Vist observed observed	12,000	1. Apl 2. Put 3. Ro	μs
9og	Common Gate Output Conductance	(Note 2)			150			150			150		

# **ELECTRICAL CHARACTERISTICS (CONT.)**

ovumo:		OOM	DITIONIO		J308		WE # 5 5	J309		100	J310		
SYMBOL	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Cgd	Gate-Drain Capacitance	V <sub>DS</sub> = 10V,			1.8	2.5		1.8	2.5		1.8	2.5	- A
Cgs	Gate-Source Capacitance	$V_{GS} = -10V$	f = 1MHz (Note 2)		4.3	5.0	is no	4.3	5.0	no b	4.3	5.0	pF
e <sub>n</sub>	Equivalent Short-Circuit Input Noise Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA	f = 100Hz (Note 2)		10	Prigit y	iemai vansv		possi Forti	riekse v cost	10	nd sta tching	nV √Hz
Re(Vfs)	Common-Source Forward Transconductance	thing Guaran	A Made		12	mon	pull )	12	mimile	laun	12	etino".	otoelko laal w
Re(Vfg)	Common-Gate Input Conductance	型600t く到			14	TWO	pland	14	of vine	ming i	14	ob rigs	
Re <sub>(Vis)</sub>	Common-Source Input Conductance		f = 105MHz		0.4	office of The	en se ensim	0.4	(Ones)	ishisha gh-frei	0.4	is Assume	μs
Re(Vos)	Common-Source Output Conductance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA			0.15	tolos Uisa s	A COL	0.15	Stage	000 E	0.15	ond rui edico	
Gpg	Common-Gate Power Gain at Noise Match	(Note 2)			16	BOASA	logeo	16	ohasiid	ncal o	16	ourse st. SV	oloeiko Roja,
NF	Noise Figure			10 6 2 6	1.5	- mining	II IZ YOU I WAR	1.5		in a second	1.5		
G <sub>pg</sub>	Common-Gate Power Gain at Noise Match	TOPOGE	f = 450MHz		11			11	PELLIF	PETER	11	TUU	dB
NF	Noise Figure				2.7	F 12 7/4 1		2.7	11.2		2.7		

NOTES: 1. Pulse test PW 300 µs, duty cycle ≤ 3%.

2. For design reference only, not 100% tested.

ABSOLUTE MAXIMUM RATINGS

celector-crankin Voltage (1)
celector-Collector Voltage
oritter-Base Voltage (1)

Operating Temperature Range ... -55°C to + 150°C
Lead Temperature (Soldering, 10sep) ... + 300°C
Power Diseignation (To - 25°C) ... 800m/M

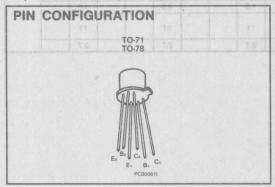
SERING INFORMATION\*

ELECTRICAL CHARACTERISTICS (NOTE 2)

# GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with  $10\mu\mathrm{A}$  collector current. Typical collector-base capacitance is only 1.6 pF at 5V.



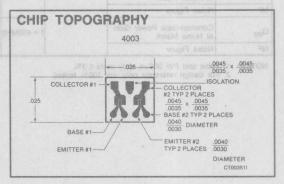
#### ORDERING INFORMATION\*

TO-71	TO-78	WAFER	DICE
LM114	LM114H	LM114/W	LM114/D
LM114A	LM114AH		

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **FEATURES**

- Low Offset Voltage
- · Low Drift
- High Current Gain Hugh Pode Included
- Tight Beta Match
- High Breakdown Voltage
- Matching Guaranteed Over A 0V to 45V Collector-Base Voltage Range
- · CMRR > 100dB



# **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Collector-Base Voltage (1)
Collector-Emitter Voltage (1)
Collector-Collector Voltage
Emitter-Base Voltage (1)
Collector Current (1)
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation (T <sub>C</sub> = 25°C)800mW
Derate above 25°C14mW/°C

# **ELECTRICAL CHARACTERISTICS (NOTE 2)**

		PARAMETER TEST CONDITIONS    MAXIMUM   LM114A, AH   AH	I LIMITS		
SYMBOL	PARAMETER		The second secon	LM114, H	UNIT
V <sub>BE1-2</sub>	Offset Voltage	$1\mu A \le I_C \le 100\mu A$	0.5	2.0	mV
I <sub>B-2</sub>	Offset Current	$I_C = 10\mu A$	2.0	10	nA
		$I_C = 1\mu A$	0.5		
	Bias Current	$I_C = 10\mu A$	20	40	nA.
		$I_C = 1\mu A$	3.0		
ΔV <sub>BE</sub> /V	Offset Voltage Change	$0V \le V_{CB} \le V_{MAX}$ , $I_C = 10\mu A$	0.2	1.5	mV
ΔV <sub>BE</sub> /V	Offset Current Change		1.0	4.0	nA

# LM114/H, LM114A/AH

# BINTERSIL

# **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL		Amplifier	MAXIMUM LIMITS		APPEND OF
	PARAMETER	TEST CONDITIONS	LM114A, AH	LM114,	UNIT
ΔV <sub>BE</sub> /ΔΤ	Offset Voltage Drift		2.0	10	μV/°C
$\Delta I_{B1-2}/\Delta T$	Offset Current	$-55^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}, \text{ I}_{\text{C}} = 10\mu\text{A}$	12	50	807
ΔΙΒ/ΔΤ	Bias Current	flate Protection	60	150	nA
Ісво	Collector-Base Leakage Current	V <sub>CB</sub> = V <sub>MAX</sub>	10	50	pA
	T <sub>A</sub> = 125°C (Note 3)		10	50	nA
ICEO 8000	Collector-Emitter Leakage Current	V <sub>CE</sub> = V <sub>MAX</sub> , V <sub>EB</sub> = 0V	50	200	pA
	T <sub>A</sub> = 125°C (Note 3)		50	200	nA
C1-C2	Collector-Collector Leakage Current	V <sub>CC</sub> = V <sub>MAX</sub>	100	300	pA
	T <sub>A</sub> = 125°C (Note 3)		100	300	nA

NOTES: 1: Per transistor	OTES: 1: Per t	ransistor
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<sup>2:</sup> These specifications apply for  $T_A = +25^{\circ}C$  and  $0V \le V_{CB} \le V_{MAX}$ , unless otherwise specified. For the LM114 and LM114A,  $V_{CMY} = 30V$ 

TO-72 WAFER DIGE
M116 M116rW M116r/D
\*When ardwing water/doc reject to Section 10, gage 10-1.

When artiaring water/disc rates to Section 19, page 10-1.

DEVICE SCHEMATIC

<sup>3.</sup> For design reference only, not 100% tested.

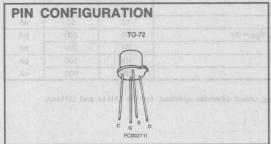
# M116

# Diode Protected N-Channel Enhancement Mode MOSFET General Purpose Amplifier



#### **FEATURES**

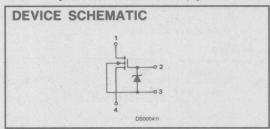
- · Log IGSS
- Integrated Zener Clamp for Gate Protection



# **ORDERING INFORMATION\***

TO-72	WAFER	DICE
M116	M116/W	M116/D

\*When ordering wafer/dice refer to Section 10, page 10-1.



# CHIP TOPOGRAPHY 1003 0025 x 0029 0035 x 0029 0040 x 0029 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 0039 s NOTE: SUBSTRATE D 0030 x 0028 0040 x 00

# **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Drain to Source Voltage	
Gate to Drain Voltage	30V
Drain Current	50mA
Gate Zener Current	±0.1mA
Storage Temperature Range65°C to	
Operating Temperature Range55°C to	+150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	.225mW
Derate above 25°C2	2mW/°C

# ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted, VBS = 0)

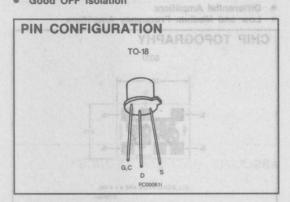
OVERDOL	DARAMETER	TEST CONDITIONS	M116		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
		$V_{GS} = 20V$ , $I_D = 100 \mu A$ , $V_{BS} = 0$		100	
「DS(on)	Drain Source ON Resistance	$V_{GS} = 10V$ , $I_D = 100 \mu A$ , $V_{BS} = 0$		200	Ω
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 10 \mu A, V_{BS} = 0$	1	5	1
BVDSS	Drain-Source Breakdown Voltage	$I_D = 1 \mu A, \ V_{GS} = V_{BS} = 0$	30		٧
BV <sub>SDS</sub>	Source-Drain Breakdown Voltage	$I_{S} = 1\mu A$ , $V_{GD} = V_{BD} = 0$	30		
BVGBS	Gate-Body Breakdown Voltage	$I_{G} = 10 \mu A$ , $V_{SB} = V_{DB} = 0$	30	60	
I <sub>D(OFF)</sub>	Drain Cutoff Current	V <sub>DS</sub> = 20V, V <sub>GS</sub> = V <sub>BS</sub> = 0		10	nA
Is(OFF)	Source Cutoff Current	$V_{SD} = 20V, \ V_{GD} = V_{BD} = 0$		10	
IGSS	Gate-Body Leakage	V <sub>GS</sub> = 20V, V <sub>DS</sub> = V <sub>BS</sub> = 0		100	рА
Cgs	Gate-Source (Note 1)	$V_{GB} = V_{DB} = V_{SB} = 0$ , $f = 1MHz$		2.5	
Cgd	Gate-Drain Capacitance (Note 1)	Body Guarded		2.5	
C <sub>db</sub>	Drain-Body Capacitance (Note 1)	V <sub>GB</sub> = 0, V <sub>DB</sub> = 10V, f = 1MHz		7	pF
Ciss	Input Capacitance (Note 1)	V <sub>GB</sub> = 0, V <sub>DB</sub> = 10V, V <sub>BS</sub> = 0, f = 1MHz		10	

NOTE 1: For design reference only, not 100% tested.

e Good Matching Characteristics

#### **FEATURES**

- Low Insertion Loss
- Good OFF Isolation



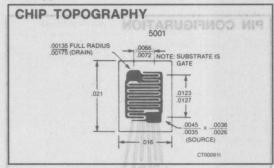
# **ORDERING INFORMATION\***

TO-18	WAFER	DICE
U200	U200/W	U200/D
U201	U201/W	U201/D
U202	U202/W	U202/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# **APPLICATIONS**

- **Analog Switches**
- Commutators
- Choppers



# **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	30V
Gate Current	50mA
Storage Temperature Range65°C	to +200°C
Operating Temperature Range55°C	to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Total Device Dissipation (T <sub>C</sub> = 25°C)	1.8W
Derate above 25°C	10mW/°C

# ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

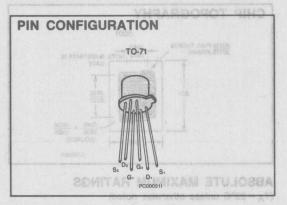
SYMBOL		PARAMETER TEST CONDITI			U200		U201		U202		ELECT
				CONDITIONS		MAX	MIN	MAX	MIN	MAX	UNIT
Igss	-	Gate Reverse Current	V <sub>GSS</sub> = 20V, V <sub>DS</sub> = 0	A STATE OF STREET		-1	- Paramon	-1		-1	nA
		T <sub>A</sub> = 150°C	TEST		AB	re <del>n</del> tas	PAI	-1		abs	μΑ
BVGSS	医海绵	Gate-Source Breakdown Voltage	$I_{G} = -1 \mu A$ , $V_{DS} = 0$		-30		-30		-30		
VGS(off)	0014	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 10nA		-0.5	-3	-1.5	-5	-3.5	-10	٧
ID(off)	00e -	Drain Cutoff Current	V <sub>DS</sub> = 10V, V <sub>GS</sub> = -	12V	AF	1	OTHER DESIGNATION	1	HBEI	1	nA
		T <sub>A</sub> = 150°C	0 * gqV ,Aur = gl		- 600	101	ELEGIKO.	00 Ho	1800	1	μΑ
IDSS	0.6-	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		3	25	15	75	30	150	mA
rds(on)	10.4	Drain-Source ON Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1kHz		150	phenon	75	dan	50	ohm
C <sub>iss</sub>	-00	Common-Source Input Capacitance (Note 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 1MHz		30	ng Curt	30	Gab	30	pF
C <sub>rss</sub>	086-	Common-Source Reverse Transfer Capacitance (Note 2)	V <sub>DS</sub> = 0, V <sub>GS</sub> = -12V		AT	8		8		8	Pi

NOTES: 1: Pulse test required, pulsewidth = 300 µs, duty cycle ≤ 3%. 2. For design reference only, not 100% tested.

2-105

#### **FEATURES**

Good Matching Characteristics



P Analog Switches

● Consentators

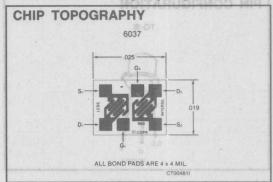
## ORDERING INFORMATION\*

TO-71	WAFER	DICE
U23X	U23X/W	U23X/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### **APPLICATIONS**

- Differential Amplifiers
- Low and Medium Frequency Amplifiers



## ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = 25°C unless otherwise noted) Gate-Source or Gate-Drain Voltage (Note 1) ...... -50V

Storage Temperature Range .....-65°C to +200°C Operating Temperature Range ...... -55°C to +200°C Lead Temperature (Soldering, 10sec) ...... +300°C Power Dissipation ......300mW

# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted.

SYMBOL		PARAMET	ED	TEST CONDITIONS			IITS	1088
STME	BUL	PARAMET	06-	0 = agv Aut - = pl epsi	MIN	MAX	UNIT	
	01-1	-1.5 - 3- B-	8.0-		ource Culoft Voltage	Garia-S	-100	рА
IGSS		Gate Reverse Current	T <sub>A</sub> = 150°C	$V_{GS} = -30V, V_{DS} = 0$		Calauci	-500	nA
BVGSS		Gate-Source Breakdown Vol	tage	$I_G = 1\mu A$ , $V_{DS} = 0$	To a T	-50		
VGS(off)	180	Gate-Source Cutoff Voltage		V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	on Orsin Clurrent (Note	-0.5	-4.5	V
VGS	na I	Gate-Source Voltage	elast - 1			-0.3	-4.0	
					least source treat	Consum	-50	рА
IG		Gate Operating Current		$V_{DG} = 20V, I_D = 200\mu A$		Capaci		0.00
	8		T <sub>A</sub> = 125°C	Vgs = 0.		Commit	-250	nA
IDSS		Saturation Drain Current (No	ote 2)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		0.5	5.0	mA
		Common-Source Forward Transconductance (Note 1)		SBOJUS, duty bydle 5 3 %.	f = 1kHz	1000	3000	:8310
9fs				V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	f = 100MHz (Note 4)	1000	10.1	
9fs 9os 9os		Common-Source Forward Transconductance (Note 1)  Common-Source Output Capacitance		$V_{DG} = 20V, I_D = 200 \mu A$		600	1600	μs
				V <sub>DS</sub> =20V, V <sub>GS</sub> = 0			35	
		Common-Source Output Cor	nductance	$V_{DG} = 20V, I_D = 200\mu A$			10	
C <sub>iss</sub> C <sub>rss</sub>		Common-Source Input Capa	Common-Source Input Capacitance				6	To The State of th
		Common-Source Reverse Transfer Capacitance  Equivalent Short Circuit Input Noise Voltage		f = 1MHz			2	pF
				V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0 (Note 4)	f = 100Hz		80	nV √Hz

SYMBOL	MATCHING CHARACTERISTICS	TEST CONDITIONS			100000000000000000000000000000000000000	10000 CO.	13.00	U235 MAX	UNIT
ll <sub>G1</sub> -l <sub>G2</sub> l	Differential Gate Current (Note 4)	$V_{DG} = 20V, I_D = 200\mu A$	125°C	10	10	10	10	1010	nA
(I <sub>DSS1</sub> - I <sub>DSS2</sub> ) I <sub>DSS1</sub>	Saturation Drain Current Match (Note 2, 4)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0		5	5	5	10	15	%
IVGS1-VGS2I	Differential Gate-Source Voltage		T <sub>A</sub> = 25°C	5	10	15	20	25	mV
ΔIV <sub>GS1</sub> -V <sub>GS2</sub> I ΔT	Gate-Source Voltage Differential Drift (Note 3)		$T_A = 25^{\circ}C$ $T_B = 125^{\circ}C$	10	25	50	75	100	μV/°C
1630		$V_{DG} = 20V, I_D = 200\mu A$	$T_A = -55$ °C $T_B = 25$ °C	10	25	50	75	100	
(9fs1-9fs2) 9fs1	Transconductance Match (Note 2)		f = 1kHz	3	5	5	10	15	%
Igos1-gos2	Differential Output Conductance	SEA.		5	5	5	5	5	μs

NOTES: 1. Per transistor.

2. Pulse test required, pulse width =  $300\mu s$ , duty cycle  $\leq 3\%$ .

3. Measured at end points, T<sub>A</sub> and T<sub>B</sub>
4. For design reference only, not 100% tested.

High Frequency Amplifier

	Common-Source Output Conductance				
200					
raedi sead		V <sub>OS</sub> = 10V, V <sub>OS</sub> = 0			
t and Sand					
			(= 1kHz		

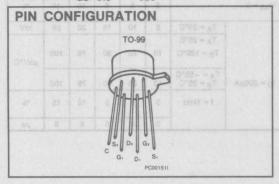
# U257

# **Dual N-Channel JFET High Frequency Amplifier**



#### FEATURES AND XAM XAM XAM

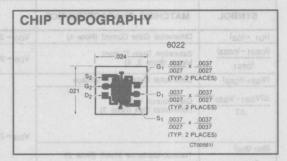
- gfs > 5000μs From DC to 100MHz
- Matched VGS, gfs and gos



# **ORDERING INFORMATION\***

TO-99	WAFER	DICE
U257	U257/W	U257/D

\*When ordering wafer/dice refer to Section 10, page 10-1.



# **ABSOLUTE MAXIMUM RATINGS**

(TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1)	
Gate Current (Note 1)	50mA
Storage Temperature Range65°C to +	200°C
Operating Temperature Range55°C to +	150°C
Lead Temperature (Soldering, 10sec)+	300°C

ONE SIDE BOTH SIDES

Power Dissipation (T<sub>A</sub> = 85°C) ..... 250mW Derate above 25°C ...... 3.8mW/°C

500mW 7.7mW/°C

# ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

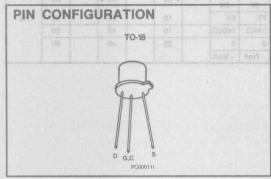
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
IGSSR	Gate Reverse Current	V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0			-100	рА
doon	T <sub>A</sub> = 150°C	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			-250	nA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1 \mu A, V_{DS} = 0$		-25		
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA		-1	-5	٧
IDSS	Saturation Drain Current (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		5	40	mA
9fs	Common-Source Forward Transconductance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 5mA	f = 1kHz	5000	10,000	
9fs	Common-Source Forward Transconductance	$V_{DG} = 10V$ , $I_D = 5mA$	OG = 10V, ID = 5mA   f = 100MHz (Note 3)		10,000	
9os	Common-Source Output Conductance	non-Source Output Conductance non-Source Input Capacitance non-Source Reverse Transfer Capacitance  VDG = 10V, ID = 5mA  f = 100MHz  f = 10MHz			150	μs
9oss .	Common-Source Output Conductance				150	
C <sub>iss</sub>	Common-Source Input Capacitance			13.00	5	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance				1.2	pF
<del>e</del> n	Equivalent Input Noise Voltage				30	nV √Hz
I <sub>DSS1</sub> I <sub>DSS2</sub>	Drain Current Ratio at Zero Gate Voltage (Note 2)	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0		0.85	1	
VGS1-VGS2	Differential Gate-Source Voltage				100	mV
9fs1 9fs2	Transconductance Ratio	$V_{DG} = 10V$ , $I_D = 5mA$		0.85	1	
gos1-gos2	Differential Output Conductance		f = 1kHz		20	μs

1. Per transistor.

2. Pulse test required, pulse width =  $300\mu s$ , duty cycle  $\leq$  3%. 3. For design reference only, not 100% tested.

# **FEATURES**

- Low ON Resistance
- I<sub>D(off)</sub> < 500pA Switches directly from TTL Logic (U306)



# **ORDERING INFORMATION\***

TO-18	WAFER	DICE
U304	U304/W	U304/D
U305	U305/W	U305/D
U306	U306/W	U306/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

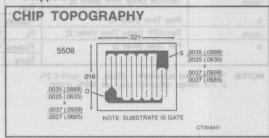
# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted.

		TEST CONDITIONS  Vos = 20V. Vos = 0		U304		U305		U306		
SYMBOL	PARAMETER			MIN	MIN MAX MIN	MAX	MIN	MAX	UNIT	
IGSSR	Gate Reverse Current				500	7	500		500	рА
	T <sub>A</sub> = 150°C				1.0		1.0		1.0	μΑ
BVGSS	Gate-Source Breakdown Voltage	$I_G = 1\mu A$ , $V_{DS} = 0$		30		30		30		
VGS(off)	Gate-Source Cutoff Voltage	$V_{DS} = -15V$ , $I_{D} = -1$	μА	5	10	3	6	1	4	V
V <sub>DS(on)</sub>	Drain-Source ON Voltage	$V_{GS} = 0$ , $I_D = -15$ mA (U304), $I_D = -7$ mA (U305), $I_D = -3$ mA (U306)			-1.3		-0.8		-0.6	V
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0		-30	-90	-15	-60	-5	-25	mA
ID(off)	Drain Cutoff Current	$V_{DS} = -15V$ , $V_{GS} = 12V$ (U304) $V_{GS} = 7V$ (U305)			-500		-500		-500	рА
B(OII)	T <sub>A</sub> = 150°C		5V (U306)		-1.0		-1.0	Be 6	-1.0	μΑ
「DS(on)	Static Drain-Source ON Resistance	VGS = 0V, ID = -1mA	4		85		110		175	Ω
rds(on)	Drain-Source ON Resistance	$V_{GS} = 0V, I_{D} = 0$	f = 1kHz		85		110		175	Ω
Ciss	Common-Source Input Capacitance (Note 2)	$V_{DS} = -15V,$ $V_{GS} = 0$			27		27		27	
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 2)	V <sub>DS</sub> = 0, V <sub>GS</sub> = 12V (U304) V <sub>GS</sub> = 7V (U305), V <sub>GS</sub> = 5V (U306)	f = 1MHz	4	7		7		7	pF

# APPLICATIONS

- **Analog Switches**
- Commutators
- Choppers



# ABSOLUTE MAXIMUM RATINGS

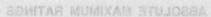
(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current50mA
Storage Temperature Range65°C to +200°C
Operating Temperature Range55°C to +150°C
Lead Temperature (Soldering, 10sec)300°C
Power Dissipation350mW
Derate above 25°C

m
m
m
m
m
m
1000
100g
100

CVMDOL	PARAMETER OF ACT	U	504	U	505	U	306	UNIT				
SYMBOL	PARAMETER TEST CONDITIONS							MIN	MAX	MIN	MAX	
	210187971	MSO S	U304	U305	U306					Aqq	起 > (7	o)G0
<sup>†</sup> d(on)	Turn-ON Delay Time (Note 2)	V	-10V	-6V	-6V	EU) a	20	ITT n	25	direct	25	BMS .
	VARAGIONANT	VDD				DESINE.		LEUTH!	A CH	ROID.	WOOM	LAFEL
tr	Rise Time (Note 2)	VGS(off)	12V	7V	5V		15	Labor.	25	2 Men 2 2	35	ns
td(off)	Turn-OFF Delay Time (Note 2)	RL	580Ω	743Ω	1800Ω		10	no re	15		20	
ty (enno) enno	Fall Time (Note 2)	VGS(on)	0	0	0		25		40		60	
(0030.) 9250		ID(on)	-15mA	-7mA	-3mA		1					

NOTES: 1. Pulse test pulsewidth =  $300\mu s$ , duty cycle  $\leq 3\%$ . 2. For design reference only, not 100% tested.

> BESO, 1960. BESO, 1960. BESO, 1960. BESO, 1960. BESO, 1960. BESO, 1960. BESO, 1960.





# ORDERING INFORMATION\*

When entering water/documents Section 10, page 10

## ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

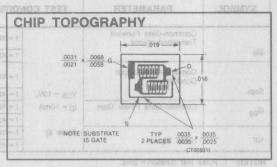
			7.0		90	CU.		
				641900	XAM	Milan	XAM	
riseo								
								Au
						-5		
		(90SP) A						
			2					



# FEATURES YT HIM XAM 9YT HIM XAM 9YT HIM

- High Power Gain
- Low Noise
- Dynamic Range Greater Than 100dB
- Easily Matched to 75Ω Input

# PIN CONFIGURATIONS TO-52 G,C



# ABSOLUTE MAXIMUM RATINGS

(T <sub>A</sub> = 25°C unless otherwise noted)	
Gate-Drain or Gate-Source Voltage	25V
Gate Current	
Storage Temperature65°C to +	-200°C
Operating Temperature Range55°C to +	-150°C
Lead Temperature (Soldering, 10sec)	-300°C
Power Dissipation	500mW
Derate above 25°C4	nW/°C

# **ORDERING INFORMATION\***

TO-52	WAFER	DICE
U308	U308/W	U308/D
U309	U309/W	U309/D
U310	U310/W	U310/D

<sup>\*</sup>When ordering wafer/dice refer to Section 10, page 10-1.

## **ELECTRICAL CHARACTERISTICS** (25°C unless otherwise noted)

OVILIDA:			IDITIONS		U308			U309			U310		
SYMBOL	PARAMETER	TEST CO	MIN	TYP	MAX	MIN	TYP	MAX	MIN	ТҮР	MAX	UNIT	
Igss	Gate Reverse Current	V <sub>GS</sub> = -15V				-150			-150			-150	рА
	T <sub>A</sub> = 125°C	V <sub>GS</sub> = 0				-150			-150			-150	nA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$		-25			-25			-25			
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub>	= 1nA	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0	V
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 10V, V <sub>O</sub>	GS = 0	12		60	12		30	24		60	mA
V <sub>GS(f)</sub>	Gate-Source Forward Voltage	I <sub>G</sub> = 10mA, V <sub>DS</sub> = 0				1.0			1.0			1.0	٧
9fg	Common-Gate Forward Transconductance (Note 1)	V <sub>DS</sub> = 10V,		10	17		10	17		10	17		μs
gogs	Common Gate Output Conductance	I <sub>D</sub> = 10mA	f = 1kHz			250			250			250	μs
C <sub>gd</sub>	Drain-Gate Capacitance	V <sub>GS</sub> = -10V,				2.5			2.5			2.5	
Cgs	Gate-Source Capacitance	V <sub>DS</sub> = 10V	f = 1MHz (Note 2)			5.0			5.0			5.0	pF
ēn	Equivalent Short Circuit Input Noise Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 10mA	f = 100Hz (Note 2)		10			10			10		nV √Hz

# U308-U310



# **ELECTRICAL CHARACTERISTICS (CONT.)**

				U308			U309				100		
SYMBOL	PARAMETER	TEST CONDITIONS			TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	Common-Gate Forward Transconductance		f = 100MHz		15			15		nis	15	re9 r	lgiH (
9fg	. 0900		f = 450MHz		14	SH	001	14	natan	c) 6	14	noti :	
4	Common-Gate Output Conductance		f = 100MHz		0.18			0.18	Oay	of t	0.18	lly Mi	μs
9ogs	/【建理》	V <sub>DS</sub> = 10V,	f = 450MHz		0.32			0.32	21.1 A	MU	0.32	100	MIG
Gpg	Common-Gate Power Gain	$I_D = 10mA$	f = 100MHz	14	16	B) / B	14	16		14	16		1915
~pg			f = 450MHz	10	11		10	- 11		10	11		
ann	LOND ANT STARTERING	(Note 2)	f = 100MHz		1.5	2.0		1.5	2.0		1.5	2.0	dB
NF	Noise Figure		f = 450MHz		2.7	3.5	-1-2	2.7	3.5	1	2.7	3.5	

NOTES: 1. Pulse test duration = 2ms.

2. For design reference only, not 100% tested.

ORDERING INFORMATION\*
TO-62 WAFER DICS
U308 U308/W U308/D
U309 U308/W U308/O

LECTRICAL CHARACTERISTICS (25°C unions officients noted)

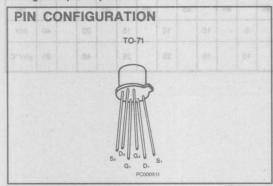
	YEST CON		KASS		XAM	SYT	
							V
Sabration Drain Opment (Note 1)			99				Am
					0.1		
	Amilit = cit						

# U401-U406 Dual N-Channel JFET Switch



# **FEATURES**

- Minimum System Error and Calibration
- Low Drift With Temperature
- Operates From Low Power Supply Voltages
- High Output Impedance



# **ORDERING INFORMATION\***

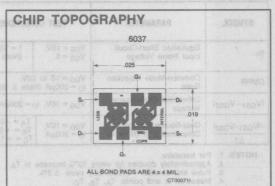
TO-71	WAFER	DICE
U40X	U40X/W	U40X/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted.

		F. Carlotte		U4	01	U4	102	U4	103	U4	104	U4	105	U4	406	
SYMBOL	PARAMETER	TEST CO	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
BVGSS	Gate-Source Breakdown Voltage	$V_{DS} = 0$ , $I_{G} = -1\mu A$		-50		-50		-50		-50		-50		-50		٧
IGSS	Gate Reverse Current (Note 2)	V <sub>DS</sub> = 0, V <sub>GS</sub>	= -30V		-25		-25		-25		-25		-25		-25	pA
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 15V, I <sub>C</sub>	) = 1nA	5	-2.5	5	-2.5	5	-2.5	5	-2.5	5	-2.5	5	-2.5	
V <sub>G</sub> S(on)	Gate-Source Voltage (on)	V <sub>DG</sub> = 15V, I <sub>E</sub>	$_{0} = 200 \mu A$	No. 1	-2.3		-2.3		-2.3		-2.3		-2.3		-2.3	٧
IDSS	Saturation Drain Current (Note 3)	V <sub>DS</sub> = 10V, V	GS = 0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA
IG	Operating Gate Current	V <sub>DG</sub> = 15V, I <sub>E</sub>	$_{0} = 200 \mu A$		-15		-15		-15		-15		-15		-15	pA
	(Note 2) T <sub>A</sub> = 125°C			1	-10	1	-10		-10		-10		-10		-10	nA
BV <sub>G1-G2</sub>	Gate-Gate Breakdown Voltage	$V_{DS} = 0$ , $V_{GS}$ $I_{G} = \pm 1 \mu A$	= 0,	±50		±50		±50		±50		±50		±50		٧
9fs	Common-Source Forward Transconductance (Note 3)	V <sub>DS</sub> = 10V,	f = 1kHz	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	
9os	Common-Source Output Conductance	V <sub>GS</sub> = 0	1802		20		20		20		20		20		20	
9fs	Common-Source Forward Transconductance			1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	μs
9os	Common-Source Output Conductance	V <sub>DG</sub> = 15V,	f = 1kHz		2.0		2.0		2.0		2.0		2.0		2.0	
Ciss	Common-Source Input Capacitance (Note 6)	$I_D = 200\mu A$	4 4101-		8.0		8.0		8.0		8.0		8.0		8.0	-
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance (Note 6)	f = 1MHz			3.0		3.0		3.0		3.0		3.0		3.0	pF



# ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	50V
Gate Current (Note 1)	10mA
Storage Temperature Range65°C to	+200°C
Operating Temperature Range55°C to	+150°C
Lead Temperature (Soldering, 10sec)	+300°C

500mW 5mW/°C 2

0101001	MURARE	0902.0	U	401	U402		U403		U404		U405		U406		-	
SYMBOL	PARAMETER	TEST CONDITIONS			MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
e <sub>n</sub>	Equivalent Short-Circuit Input Noise Voltage	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0	f = 10Hz (Note 6)		20		20	Talleri.	20	tavis	20	10T	20	218	20	nV √Hz
	input riolog voltago	105	(1.0.0 0)			Car Colores	100	of tride			COMP.	haber	MENDS	sandas	0 49	√Hz
CMRR	Common-Mode Rejection Ratio	$V_{DG} = 10 \text{ to}$ $I_{D} = 200 \mu \text{A}$ (1)	95		95	n wyse	95		95	FY	90	5)13	1140	10	dB	
IV <sub>GS1</sub> -V <sub>GS2</sub> I	Differential Gate-Source Voltage	V <sub>DG</sub> = 10V, 1		5		10		10		15		20		40	mV	
△IV <sub>GS1</sub> -V <sub>GS2</sub> I	Gate-Source Voltage Differential Drift (Note 4)	V <sub>DG</sub> = 10V, I <sub>D</sub> = 200μA	$T_A = -55$ °C, $T_B = +25$ °C, $T_C = +125$ °C	13.4	10		10		25		25		40		80	μV/°C

NOTES: 1. Per transistor.

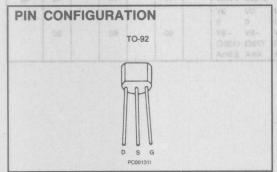
Per transistor.
 Approximately doubles for every 10°C increase in T<sub>A</sub>.
 Pulse test duration = 300 µs; duty cycle ≤ 3%.
 Measured at end points, T<sub>A</sub>, T<sub>B</sub>, T<sub>C</sub>.

6. For design reference only, not 100% tested. 

NAME OF THE OWNER, WHEN THE OW																					
3088745														MILL							
	Common-Source Forward Transconduciance (Note 3)		F# TRING																		

# FEATURES

- Low Insertion Loss
- No Error or Offset Voltage Generated By Closed Switch



#### **ORDERING INFORMATION\***

TO-92	TO-92-18	WAFER	DICE
U1897	U1897-18	U1897/W	U1897/D
U1898	U1898-18	U1898/W	U1898/D
U1899	U1899-18	U1899/W	U1899/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

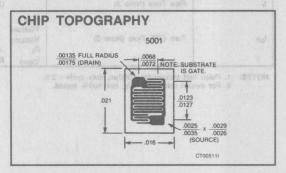
# **ELECTRICAL CHARACTERISTICS**

TEST CONDITIONS: 25°C unless otherwise noted

			U1	897	U1898		U1899			
SYMBOL	PARAMETER	TEST CONDIT	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$	-40		-40		-40		٧	
IGSS	Gate Reverse Current	VGS = -20V, VDS = 0		-400		-400		-400		
IDGO	Drain-Gate Leakage Current	V <sub>DG</sub> = 20V, I <sub>S</sub> = 0			200		200		200	pA
Isgo	Source-Gate Leakage Current	V <sub>SG</sub> = 20V, I <sub>D</sub> = 0		7181	200		200		200	PA
ID(off)	Drain Cutoff Current	V <sub>DS</sub> = 20V, V <sub>GS</sub> = -12V (U1897)			200					
	T <sub>A</sub> = 85°C	$V_{GS} = -8V \text{ (U1898)}$ $V_{GS} = -6V \text{ (U1899)}$			10		10		10	nA
VGS(off)	Gate-Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	-5.0	-10	-2.0	-7.0-	-1.0	-5.0	٧	
IDSS	Saturation Drain Current (Note 1)	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0	7 7	30		15		8.0		mA
V <sub>DS</sub> (on)	Drain-Source ON Voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 6.6mA (U1897) I <sub>D</sub> = 4.0mA (U1898) I <sub>D</sub> = 2.5mA (U1899)			0.2		0.2		0.2	٧
「DS(on)	Static Drain-Source ON Resistance	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0			30		50		80	Ω
C <sub>dg</sub>	Drain-Gate Capacitance	V <sub>DG</sub> = 20V, I <sub>S</sub> = 0			5		5		5	
C <sub>sg</sub>	Source-Gate Capacitance	V <sub>SG</sub> = 20V, I <sub>D</sub> = 0			5		5		5	
C <sub>iss</sub>	Common-Source Input Capacitance		f = 1MHz		16		16	MAN C	16	pF
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	$V_{DS} = 20V, V_{GS} = 0$	(Note 2)		3.5		3.5		3.5	

# APPLICATIONS

Analog Switches, Choppers



## **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)
Gate-Drain or Gate-Source Voltage40V
Forward Gate Current10mA
Storage Temperature Range55°C to +150°C
Operating Temperature Range55°C to +135°C
Lead Temperature (Soldering, 10sec)+300°C
Power Dissipation350mW
Derate above 25°C 3.2mW/°C

2

### U1897-U1899



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

	COMPANY	19 TEST COMPLETIONS	U1897		U1898		U1899		7.6.79
SYMBOL	PARAMETER ***	TEST CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>d(on)</sub>	Turn ON Delay Time (Note 2)	Switching Time Test Conditions	beden	15	mella	15	10 10	20	015
tr	Rise Time (Note 2)	U1897 U1898 U1899		10	No. 15	20		40	ns
	ТОРОСЯВРНУ	V <sub>DD</sub> 3V 3V 3V V <sub>GS(on)</sub> 0 0 0			MOL	TARK	Fici	400	1019
toff	Turn OFF Time (Note 2)	VGS(off) -12V -8V -6V R <sub>L</sub> 425Ω 770Ω 1120Ω ID(on) 6.6mA 4mA 2.5mA		40	\$9.01	60		80	

NOTES: 1. Pulse test pulsewidth = 300 µs; duty cycle < 3%.
2. For design reference only, not 100% tested.

		OFF			Hadro	
					50 /50	

N-Channel JFET Switch

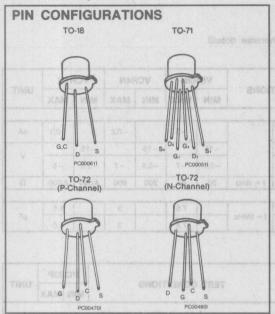
GV1981U		
	U1898/W	

						PARAMETER	
		XAM					
					V <sub>SQ</sub> = 20V <sub>1</sub> t <sub>D</sub> = 0		
An							
						Saturation Crain Current (Note 1)	
					Vgs + Q Amb.8 = q Amb.4 (1981U) Amb.4 = q Q Amb.4 = q Am		

## VCR2N/3P/4N/7N Voltage Controlled Resistors

## APPLICATIONS

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control



#### ORDERING INFORMATION\*

TO-18	TO-72	WAFER	DICE
VCR2N	- L	VCR2N/W	VCR2N/D
VCR4N	-	VCR4N/W	VCR4N/D
- a	VCR3P	VCR3P/W	VCR3P/D
_	VCR7N	VCR7N/W	VCR7N/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

CHIP TOPOGRAPHY 5001 .00135 FULL RADIUS GATE .0045 x .0036 (SOURCE) CT00680I VCR7N 5007 .015 .0060 .0062 (TYP) SUBSTRATE IS GATE FULL R VCR3P 5508 .021 016 NOTE: SUBSTRATE IS GATE VCR4N 5010 (4N) .0013 FULL R NOTE: SUBSTRATE lorent consbeam divertine nimel e control curr e160 The gate voltage is an TYP. 2 PLACES third quadrant Di .0035 x .0035 TYP. 2 PLACES

2-117

## VCR2N/3P/4N/7N

## 

#### **ABSOLUTE MAXIMUM RATINGS**

(T <sub>A</sub> = 25°C unless otherwise noted)	personal services
Gate-Drain or Gate-Source Voltage	15V
Gate Current	
Storage Temperature Range65°C t	o +200°C
Operating Temperature Range55°C t	o +175°C
Lead Temperature (Soldering, 10sec)	+ 300°C
Power Dissipation	300mW
Derate above 25°C	2mW/°C

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

#### N Channel VCR FETs

	CRUCKS (arrive 512 ments)		TIONS	VCR2N		VCR4N		VCR7N		UNIT	
SYMBOL	PARAMETER	TEST CONDI	IIONS	MIN	MAX	MIN	MAX	MIN	MAX		
STATIC		SHOULD BE SHOULD			( )(a)(a)			4			
Igss	Gate Reverse Current	V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0			-5		-0.2	K	-0.1	nA	
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$		-15	1 0 110	2-15		-15	0.0	V	
V <sub>GS</sub> (off)	Gate-Source Cutoff Voltage	$I_D = 1 \mu A, V_{DS} = 10 V$		-3.5	-7	-3.5	-7	-2.5	-5		
rds(on)	Drain source ON Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1kHz	20	60	200	600	4,000	8,000	Ω	
DYNAMIC (I	Note 1)										
C <sub>dgo</sub>	Drain-Gate Capacitance	$V_{GD} = -10V$ , $I_{S} = 0$	4 - 41411-		7.5		3	1	1.5		
C <sub>sgo</sub>	Source-Gate Capacitance	V <sub>GS</sub> = -10V, I <sub>D</sub> = 0		200	7.5		3	4	1.5	pF	

NOTE 1: For design reference only, not 100% tested.

#### P Channel VCR FETS

1000 6500			VC	R3P			
SYMBOL	PARAMETER	TEST CON	DITIONS		MIN	MAX	UNIT
STATIC		John	60A				
IGSS 3 TAT THE STATE	Gate Reverse Current	V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0		o an ing a		20	nA
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = 1\mu A, V_{DS} = 0$	MORTARIE		15	PARE	ELEST.
V <sub>G</sub> S(off)	Gate-Source Cutoff Voltage	$I_D = -1\mu A$ , $V_{DS} = -10V$	RESAM	534	3.5	7	V
rds(on)	Drain-Source ON Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1kHz	and the second	70	200	Ω
DYNAMIC (Note 1	)		The second second			7/10	
C <sub>dgo</sub>	Drain-Gate Capacitance	V <sub>GD</sub> = 10V, I <sub>S</sub> = 0	f = 1MHz			6	pF
C <sub>sgo</sub>	Source-Gate Capacitance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0	(Note 1)		OV	6	

NOTE 1: For design reference only, not 100% tested.

#### JFETS AS VOLTAGE REGULATORS

The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

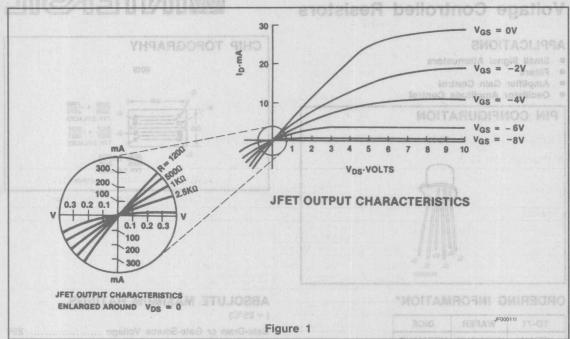
The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

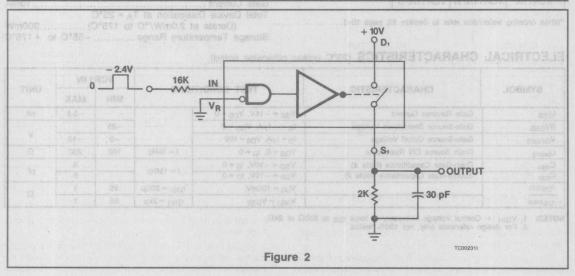
This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of VDS = 0 for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant

current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about  $100\Omega$ .

Best gate control voltage for best linearity is up to about 0.8VpK; ON resistance increases rapidly beyond this point.





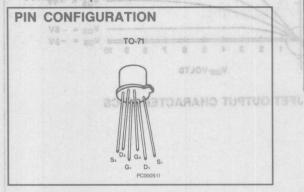
## VCR11N

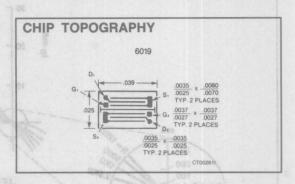
## **Voltage Controlled Resistors**

## 

#### **APPLICATIONS**

- Small Signal Attenuators
- Filters
- **Amplifier Gain Control**
- Oscillator Amplitude Control





#### **ORDERING INFORMATION\***

TO-71	WAFER	DICE
VCR11N	VCR11N/W	VCR11N/D

\*When ordering wafer/dice refer to Section 10, page 10-1.

#### ABSOLUTE MAXIMUM RATINGS

 $(=25^{\circ}C)$ 

Gate-Drain or Gate-Source Voltage 25	5V
Gate Current	nA
Total Device Dissipation at TA = 25°C	
(Derate at 2.0mW/°C to 175°C)300m	W
Ctorage Tomporature Denge	00

#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		1 100	VCF	UNUT			
SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN	MAX	UNIT	
Igss	Gate Reverse Current	V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0			-0.2	nA	
BVGSS	Gate-Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0$		-25			
VGS(off)	Gate-Source Cutoff Voltage	$I_D = 1\mu A, \ V_{DS} = 10V$		-8	-12	V	
rds(on)	Drain Source ON Resistance	V <sub>GS</sub> = 0, I <sub>D</sub> = 0	f = 1kHz	100	200	Ω	
C <sub>dgo</sub>	Drain-Gate Capacitance (Note 2)	$V_{GD} = -10V, I_S = 0$			. 8	_	
Csgo	Source-Gate Capacitance (Note 2)	$V_{GS} = -10V, I_{D} = 0$	f = 1MHz		8	pF	
r <sub>DS</sub> min	Sugar Sugar	V <sub>DS</sub> = 100mV	$r_{DS1} = 200\mu$	.95	1	Ω	
r <sub>DS</sub> max		V <sub>GS1</sub> = V <sub>GS2</sub>	$r_{DS1} = 2k\mu$	.95	1	22	

NOTES: 1. V<sub>GS1</sub> + Control Voltage necessary to force r<sub>DS</sub> to 200 $\Omega$  or 2k $\Omega$ . 2. For design reference only, not 100% tested.

# Section 3 — Analog Switches and Multiplexers

Section 3 — Analog Switches and Multiplexers

3

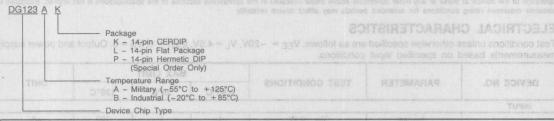
#### **GENERAL DESCRIPTION**

The D123 and D125 monolithic bipolar drivers convert low-level positive logic signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

#### **FEATURES**

- Provides DC Level Shifting Between Low-Level
   Logic and MOSFET or JFET Switches
- External Collector Pull-Ups Required
- Direct Interface With G116, G117, G119, G115, and G123 MOSFET Switches

#### ORDERING INFORMATION



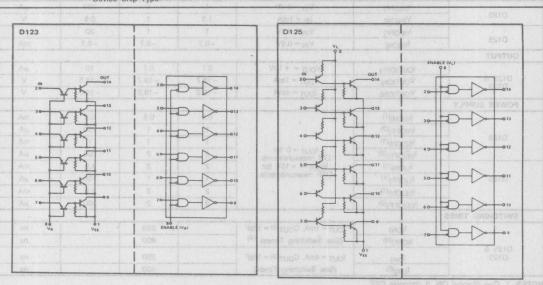


Figure 1: Functional Diagram (Outline Dwgs DD, FD-2, JD)

#### D123/D125



#### **ABSOLUTE MAXIMUM RATINGS**

Input-to-Emitter Voltage (VIN - VFF)	33V
Output-to-Emitter Voltage (VO - VEE)	33V
Logic Supply-to-Emitter Voltage (VL - VEE)	27V
Input-to-Reference Voltage (VIN - VR)	2V
Input-to-Logic Supply Voltage (VIN - VL)	+6V
Reference-to-Emitter Voltage (VR - VEE)	31V

Maximum Dissipation (Note)			750mW
Current (any pin)			
Storage Temperature	-65°C	to	+150°C
Operating Temperature	-55°C	to	+125°C
Lead Temperature (Soldering, 10sec)	BOAD I	9.	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/ °C for higher ambient temperature.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

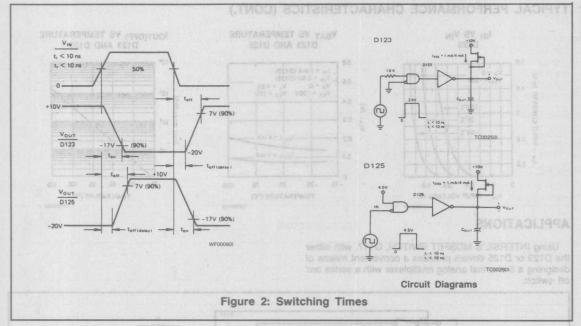
Test conditions unless otherwise specified are as follows: VEE = -20V, VL = 4.5V, IOUT = 0, VR = 0. Output and power supply measurements based on specified input conditions.

				MAX LIMIT		
DEVICE NO.	PARAMETER	TEST CONDITIONS	-55°C	25°C	125°C	UNIT
INPUT				and out	Various 1	
	IN(OFF)	V <sub>IN</sub> = 0.4V	1	1	100	μΑ
D123	VIN(ON)	I <sub>IN</sub> = 1mA	1.3	1	0.8	V
	IN(OFF)	V <sub>IN</sub> = 4.1V	1	1	20	μΑ
D125	IN(ON)	V <sub>IN</sub> = 0.5V	-0.7	-0.7	-0.7	mA
OUTPUT						
	lout(off)	V <sub>OUT</sub> = +10V	0.1	0.1	10	μΑ
D125 &	Vout(on)	I <sub>OUT</sub> = 1mA	-19.7	-19.7	-19.5	٧
D123	Vout(on)	I <sub>OUT</sub> = 4mA	-19.2	-19.2	-19.0	V
POWER SUPPLY	House	UK BALL BU BU BE	1 /1 /-	The state of the s	and a	
want -C	IR(ON)(1)		0.5	0.5	0.5	mA
	I <sub>R</sub> (OFF) <sup>(2)</sup>	HILLIE MAN	1	1	150	μΑ
D123	IEE(ON)(1)		1	1	1	mA
	IEE(OFF)(2)	I <sub>OUT</sub> = 0 for ON measurements.	2	2	200	μΑ
	I <sub>L</sub> (ON) <sup>(1)</sup>	V <sub>OUT</sub> = +10V for	2	2	1.9	mA
D125	IL(OFF)(1)	OFF measurements.	· (1)	1	100	μΑ
	IEE(ON)(1)	1000	2	2	1.9	mA
	JEE(OFF)(2)		2	2	200	μΑ
SWITCHING TIME						-
10-10-0	t(ON)	IOUT = 1mA, COUT(3) = 10pF	4	250	and the	ns
	t(OFF)(4)	(See Switching Times) (4)		800		ns
D125 & D123	t(on)	IOUT = 4mA, COUT(3) = 10pF		250		ns
	t <sub>(off)</sub> (5)	(See Switching Times)		600		ns

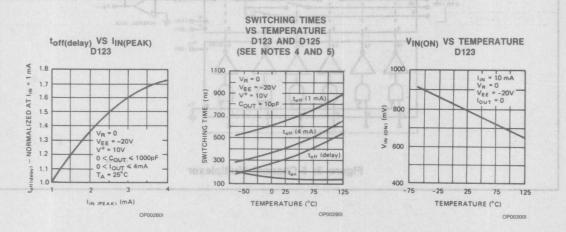
NOTES: 1. One channel ON, 5 channels OFF.

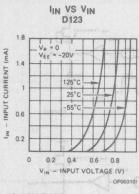
All channels OFF.
 Add 30ns per pF for 1mA and add 8ns per pF for 4mA for additional capacitive loading.
 For Dual-In-Line package add 120ns to t(off).
 For Dual-In-Line package add 30ns to t(off).

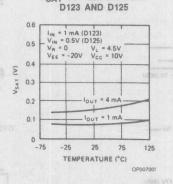




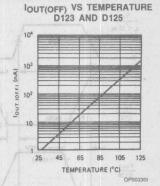
#### TYPICAL PERFORMANCE CHARACTERISTICS







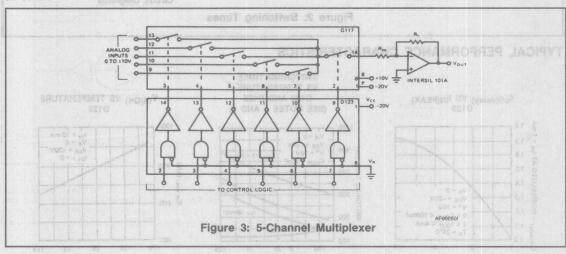
VSAT VS TEMPERATURE



#### **APPLICATIONS**

0

Using INTERSIL'S MOSFET SWITCH, G117, with either the D123 or D125 drivers provides a convenient means of designing a 5 channel analog multiplexer with a series on/off switch.

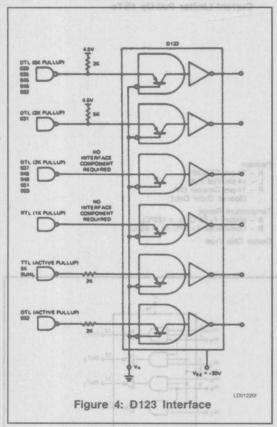


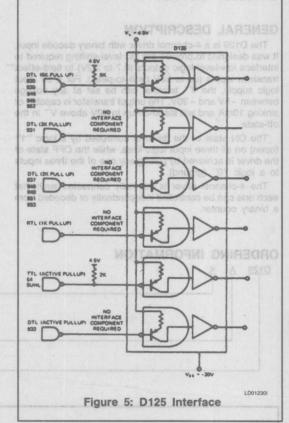
3

#### Interfacing the D123 and D125

In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping  $V_L - V_{IN} \leq 0.4V$  is a must to insure turn-off. To accomplish this, a shunt resistor must be added to supply the leakage current (ICES) for DTL devices. Since ICES =  $50\mu\text{A}$ , a  $0.4V/0.05\text{mA} = 8k\Omega$  or less resistor should be used. For TTL devices using a  $2k\Omega$  resistor will insure turn-off with up to  $200\mu\text{A}$  of leakage current.





#### Using the ENABLE Control

Device pins  $V_R$  or  $V_L$ , can be used to enable the D123 or D125 drivers. For the D123, the enabling driver must sink  $I_{R(ON)}$  X no. of channels used. For the D125,  $I_{L(ON)}$  X no. of channels used must be sourced with a voltage at least +4V greater than  $V_{IN}$ .

Equire 1: Functional Diagrams (Outline Dwgs DD, FD-2, JD

## D129

### 4-Channel Decoded JFET Switch Driver

#### GENERAL DESCRIPTION

The D129 is a 4-channel driver with binary decode input. It was designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V- terminal can be set at any voltage between -5V and -30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V in the

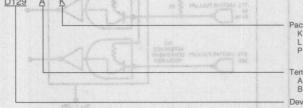
The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

#### FEATURES and term and feature at the mental party

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible With Low Power TTL and DTL. IF = 200 MA Max set ent viocus of bethe ed teurs
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required
- Compatible With G115 and G123 Series Multichannel MOSFET Switches Which Include Current-Limiter Pull-Up FETs

#### ORDERING INFORMATION



K - 14-pin CERDIP L - 14-pin Flat Pak P - 14-pin Ceramic DIP

(Special Order Only)

Temperature Range
A - Military (-55°C to +125°C)
B - Commercial (-20°C to +85°C)

Device Chip Type

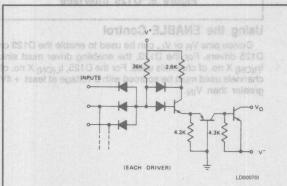


Figure 1: Functional Diagrams (Outline Dwgs DD, FD-2, JD)

#### ABSOLUTE MAXIMUM RATINGS

VO - V	. 50V
GND - V	. 33V
V <sup>+</sup> - GND	8V
V <sub>IN</sub> - GND	±6V
Current (any terminal)	30mA

Storage Temperature	-65°C	to	+150°C
Operating Temperature			
Power Dissipation (note)	301	AF	750mW
Lead Temperature (Soldering, 10sec)	uon:es	3173	300°C

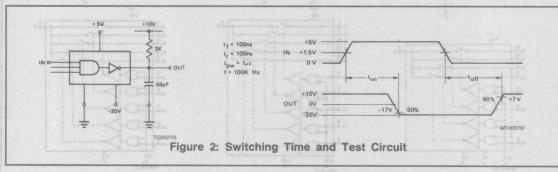
Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperatures.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified VT = -20V, VT = 5V

		3.18	ADMIXAM TABLE		M LIMI	RDERI				
SYM- BOL PARAMETER	5 87 8 75 75 V5 3 5 YU	TEST CONDITIONS			D129M			D129I		UNIT
	Switch Course Course	5/8/1		-55°C	25°C	125°C	-20°C	25°C	85°C	
OUT	and the same of th	-			okage	Plate Pa	9 41 - 1			
VOL	Output Voltage, Low	I <sub>O</sub> = 10mA		-19.3	-19.3	-19	-19.25	-19.25	-19	
VOL	Output Voltage, Low	10 = 1mA	$V_{IN} = 2.2V, V^{+} = 4.5V$	-19.8	-19.8	-19.75	- itmanim	4		V
ЮН	Output Current, High	V <sub>O</sub> = 10V, V <sub>II</sub>	V <sub>O</sub> = 10V, V <sub>IN</sub> = 0.7V		+0.1	20	0.2	0.2	10	μΑ
INPUT			and the second second	10,00	al or Var	1 7-1-17	mour e	D. T. S.		
INH*	Input Current Input Voltage High		V <sub>IN</sub> = 5V Input Under Test, V <sub>IN</sub> = 0 All Other Inputs		0.25	5	1	1	5	
I <sub>INL</sub> *	Input Current Input Voltage Low	V <sub>IN</sub> = 0, V +	V <sub>IN</sub> = 0, V <sup>+</sup> = 5.5V		-200	-160	-250	-225	-200	μΑ
TIME	ne Changel)	0)	(inverse	(One Ch		The Land		Hanna	Cons. Ca	
ton	Turn-ON Time				0.25	Dietis	70	0.3		
toff	Turn-OFF Time	See Switching	g Time Test Circuit		1.0			1.5		μs
SUPPL	LY									Y STA
IEE	Negative Supply Current		Other Committee of the		-2			-2.25	No.	
IL .	Logic Supply Current	$V^{-} = -20V$	One Channel "ON"		3	29-	-	3.3		mA
IEE	Negative Supply Current	V + = 5.5V	All V <sub>IN</sub> = 0,	NEED	-10			-25	francis	μΑ
IL.	Logic Supply Current		All Channels "OFF"		0.75	The said		13		mA





#### GENERAL DESCRIPTION

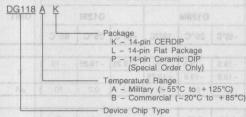
This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOSFET switch. Two driver versions are supplied for inverting and noninverting applications. A MOSFET, used as a current source provides an active pull-up for faster switching.

An external biasing connection is brought out for biasing, the current source, for optimization of speed and power.

#### **FEATURES**

- Available With and Without Programmable Constant Current Pull-up
- Zener Protection on All Gates
- P-Channel Enhancement-Type MOSFET Switches
- Each Switch Summed to One Common Point

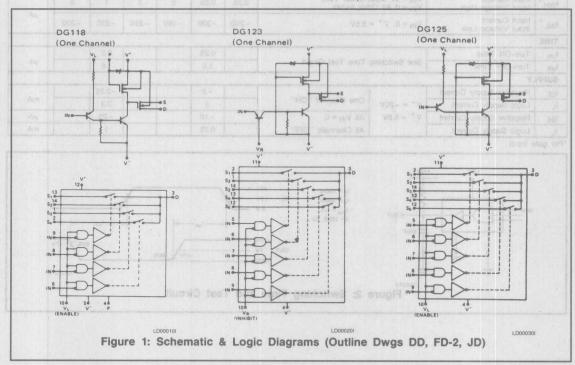
#### ORDERING INFORMATION



#### TRUTH TABLE

DG	123	DG118	Switch		
VIN	VR	VIN	V <sub>L</sub>	Cond.	
L	ALC:	L	Louis Louis	OFF	
S.S Hav	L	L	H H	ON	
L	H	Н	L	OFF	
H	Н —	H	H	OFF	

L = 0V, H = +V



#### **ABSOLUTE MAXIMUM RATINGS**

Collector to Emitter (V + -V -)	33V	
Collector to Pull-up (V + -Vp)	33V	
Drain to Emitter (VD-V-)	32V	
Source to Emitter (VS-VT)	32V	
Source to Emitter (V <sub>S</sub> -V <sup>-</sup> )	28V	
Source to Drain (VS-VD)		
Logic to Emitter (V <sub>L</sub> -V <sup>-</sup> )	33V	
Reference to Emitter (VR-V <sup>-</sup> )	31V	
Reference to Input (VR-VIN)	6V	

Logic to Input (VI -VIN)			±6V
Input to Emitter (VIN-V-)			33V
Current (any terminal)			30mA
Storage Temperature	-65°C	to	+150°C
Operating Temperature			
Dissipation (Note)			
Lead Temperature (Soldering, 10sec)			300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C.

Derate 10mW/°C for higher ambient temperature.

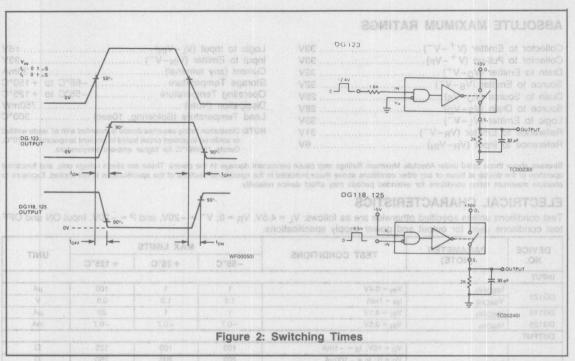
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

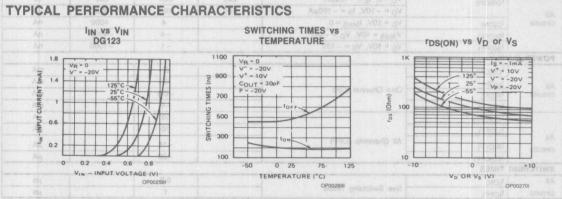
#### **ELECTRICAL CHARACTERISTICS**

Test conditions unless specified otherwise are as follows:  $V_L = 4.5V$ ,  $V_R = 0$ ,  $V^- = -20V$ , and P = -20V. Input ON and OFF test conditions used for output and power supply specifications.

DEVICE	PARAMETER TEST CONDITIONS		mg/ ===@	MAX LIMITS			
NO.	(NOTE)			+ 25°C	+ 125°C	UNIT	
INPUT							
DG123   I <sub>IN</sub> (OFF)   V <sub>IN</sub> = 0.4V   V <sub>IN</sub> (ON)   I <sub>IN</sub> = 1mA		V <sub>IN</sub> = 0.4V	1	1	100	μΑ	
		1.3	1.0	0.8	V		
DG118	IN(OFF)	V <sub>IN</sub> = 4.1V	1	1	20	μΑ	
DG125	I <sub>IN</sub> (ON)	V <sub>IN</sub> = 0.5V	-0.7	-0.7	-0.7	mA	
OUTPUT		esett pricipite	Figure 2: Sy				
		$V_D = 10V, I_S = -1mA$	100	100	125	Ω	
	$V_D = 0$ , $I_S = -100\mu A$ $V_D = -10V$ , $I_S = -100\mu A$		200	200	250	Ω	
All			450	450	600	Ω	
circuits	ID(ON)	V <sub>D</sub> = 10V, I <sub>S(all)</sub> = 0		4	4000	nA	
	ID(OFF)	$V_{S(all)} = 10V, V_{D} = -10V$	CANADA	-4	-4000	nA	
	IS(OFF)	$V_D = 10V, V_S = -10V$		-1	-1000	nA	
POWER SU	IPPLY		0 = pV   0041	PETER	With the second	-y. 5.1	
- V	ICC(ON)		V0- 4-7	3	V05-1-V	mA	
All	IL(ON)		300 TUDO 1 4	3	3389	mA	
circuits	I <sub>R</sub> (ON)	One Channel (ON)	100 V 100 E	-0.5	1225	mA	
	IEE(ON)	or o	- 5	-6		mA	
Jun-que-	ICC(OFF)		008	10	No and the latest	μΑ	
	IL(OFF)			10		μΑ	
All	IR(OFF)	All Channels (OFF)	1 300 70	-15		μΑ	
Circuits	IEE(OFF)		Jan 1001	-20	Deliver The Table	μΑ	
SWITCHING		924 92 92	0. 02-		100 A.D.		
All	t(ON)	LP / SREET AR	PART -	0.3	72	μs	
circuits	t(OFF)	See Switching Times		1		μs	

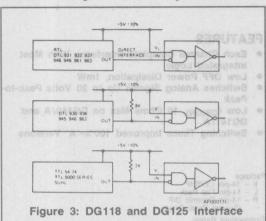
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOSFET switch for the given test condition.





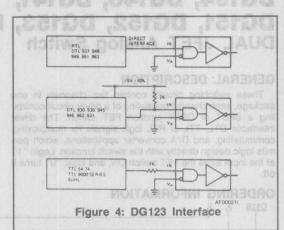
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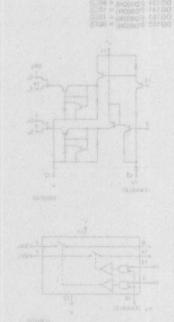
The recommended resistor values for interfacing RTL, DTL, and TTL Logic are shown in Figures 3 and 4.



#### **Enable Control**

The  $V_R$  and  $V_L$  terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at  $V_R$  or sourcing current at  $V_L$  are:  $L_{(ON)} \times No.$  of channels used, for DG118 and DG125, and  $L_{R(ON)} \times No.$  of channels used for the DG123 devices. The voltage at  $V_L$  must be greater than the voltage at  $V_{IN}$  by at least  $+4V_{\odot}$ 



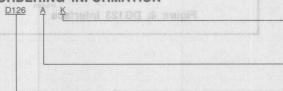


## DG151, DG152, DG153, DG154 DUAL JFET Analog Switch

#### GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it off.

#### ORDERING INFORMATION



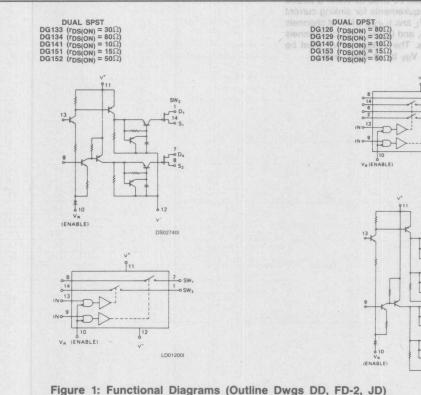
#### **FEATURES**

- Each Channel Complete-Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, 1mW
- Switches Analog Signals Up to 20 Volts Peak-to-Peak

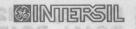
LD01210I

- Low r<sub>DS(ON)</sub>, 10 Ohms Max on DG140/A and DG141/A
- Switching Times Improved 100%-'A' Versions





## 



#### ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage (VA - V or V + - VA) 30V	Current (any terminal)
Total Supply Voltage (V + - V -)	Storage Temperature65°C to +150°C
Positive Supply Voltage to Ref. Voltage (V + - VR) 25V	Operating Temperature55°C to +125°C
Ref. Voltage to Neg. Supply Voltage (V <sub>R</sub> – V <sup>-</sup> ) 22V	Lead Temperature (Soldering, 10sec)300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS (Per Channel)**

Applied voltages for all test: DG126, DG129, DG133, DG134, DG140, DG141 (V+ = +12V, V− = -18V, VR = 0), and DG151, DG152, DG153, DG154 (V+ = + 15V, V- = -15V, V<sub>R</sub> = 0). Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

SYMBOL (NOTE)		SCIENT SS	3 85100	ABSOI			
	CHARACTERISTIC	TYPE	TEST CONDITIONS	-55°C	25°C	125°C	UNIT
INPUT	ag   rass	O ISTOO WA	SO DATED WHO SON		Chia Tarro	1997	
VIN(ON)	Input Voltage-On		V <sub>2</sub> = -12V	2.9 min	2.5 min	2.0 min	Volts
VIN(OFF)	Input Voltage-Off	Visc = 2.5V	$V_2 = -12V$	1.4	1.0	0.6	Volts
IN(ON)	Input Current	All Circuits	V <sub>IN</sub> = 2.5V	120	60	60	μΑ
IN(OFF)	Input Leakage Current		V <sub>IN</sub> = 0.8V	0.1	0.1	2	μΑ
SWITCH OUTP	UT TEST TOWNS OF	1 101 11011AW 175	T ord to letters more during a serie of t	reter numero	i ideoscaña	DAICH DUR (	(35.7) 330
rds(ON)		DG126 DG134	V <sub>IN</sub> = (See Note)	80	80	150	Ω
	Drain-Source On Resistance	DG129 DG133	$V_D = 10V$ , $I_S = 10mA$	30	30	50	Ω
		DG140 DG141		10	10	20	Ω
		DG151 DG153	V <sub>D</sub> = 7.5V, I <sub>S</sub> = 10mA	15	15	30	Ω
		DG152 DG154	V <sub>IN</sub> = (See Note)	50	50	100	Ω
ID(ON) + IS(ON)	Drive Leakage Current	DG126	$V_D = V_S = -10V$		±2	100	nA
IS(OFF)	Source Leakage Current	DG129 DG133	$V_S = 10V, V_D = -10V$		±1	100	nA
ID(OFF)	Drain Leakage Current	DG134	$V_D = 10V, V_S = -10V$		±1	100	nA
ID(ON) + IS(ON)	Drive Leakage Current		$V_D = V_S = -10V$		±2	100	nA
IS(OFF)	Source Leakage Current	DG140 DG141	$V_S = 10V, V_D = -10V$		±10 -	1000	nA
ID(OFF)	Drain Leakage Current	Daisi	$V_D = 10V, V_S = -10V$		±10	1000	nA
ID(ON) + IS(ON)	Drive Leakage Current		$V_D = V_S = -7.5V$		±2	500	nA
IS(OFF)	Source Leakage Current	DG151 DG153	$V_S = 7.5V, V_D = -7.5V$		±10	1000	nA
ID(OFF)	Drain Leakage Current	DG153	$V_D = 7.5V, V_S = -7.5V$		±10	1000	nA
D(ON) + IS(ON)	Drive Leakage Current		$V_D = V_S = -7.5V$		±2	500	nA
Is(OFF)	Source Leakage Current	DG152 DG154	$V_S = 7.5V, V_D = -7.5V$		±2	200	nA
ID(OFF)	Drain Leakage Current		$V_D = 7.5V, V_S = -7.5V$		±2	200	nA

NOTE:  $V_{IN}$  must be a step function with a minimum slew-rate of  $1V/\mu s$ .

## DG126, DG129, DG133, DG134, DG140, DG141, DG151, DG152, DG153, DG154



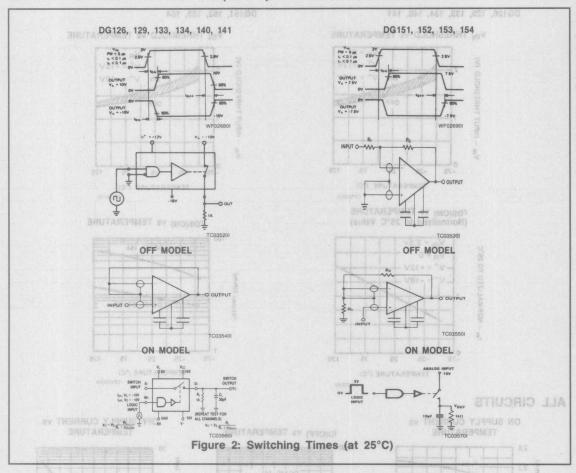
#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL				ABSO				
(NOTE)	CHARACTERISTIC	ed viTYPEems	TEST CONDITIONS	-55°C	25°C	125°C	UNIT	
POWER SUPPL	Y) sturister	gerating Temp	O VER THY - TY) BE	stieV Jel	age to P	NoV yleigus	evineo	
I <sub>1(ON)</sub>	Positive Power Supply Drain Current	IsregmoT bea	7. (All All All All All All All All All Al	epsilov.	3	ige to Ner skipstice i	mA	
1 <sub>2</sub> (ON)	Negative Power Supply Drain Current	tionio balning et be	One Driver ON, V <sub>IN</sub> = 2.5V	rom al goly	-1.8	i gnitisi notied	mA e	
IR(ON)	Reference Power Supply Drain Current	All Circuits	ve. Johnom Rabriga may dadab parmane	niki elufoet	-1.4	sil eggitt evo	mA	
I <sub>1(OFF)</sub>	Positive Power Supply Leakage Current	he operational section in a contract section	inditions above tages indicated in the periods rosy affect device rosy	o teath (m helve to)	25	s salveb and padar muroks	μА	
I <sub>2(OFF)</sub>	Negative Power Supply Leakage Current		Both Drivers OFF, V <sub>IN</sub> = 0.8V	CTERN	- 25	BICAL	μΑ	
IR(OFF)	Reference Power Supply Leakage Current	"V) TATOO .0	9129, DG193, DG194, DG14	0 8510	-25	rol constic	μА	
SWITCHING	sieh quarantees FET switch	w molifibrigo tue	V = -15V. Vq = 0). Input v	Var + =	* V) 16	96 Para	G.Saro	
ton	Turn-On Time	See Below	DG126, DG129, DG133, DG134, DG152, DG154	voq nns	600	of teau a	ns	
toff	Turn-Off Time	See Below	DG126, DG129, DG133, DG134, DG152, DG154	DITSING!	0 A 1.6	10	μs	
ton	Turn-On Time	See Below	DG140, DG141, DG151, DG153	-	1.0	in house in	μs	
toff	Turn-On Time	See Below	DG140, DG141, DG151, DG153	and the second	2.5	The second	μs	
POWER	U.S.   Hint E.S.   Hall et S.		AS1 = SV		U-eganov I	ugai	(100)417	
Pon	ON Driver Power		Both Inputs V <sub>IN</sub> = 2.5V		175	light	mW	
POFF	OFF Driver Power	All Circuits	Both Inputs V <sub>IN</sub> = 1∀		- JUST A PROPERTY OF	ACT LAND	mW	

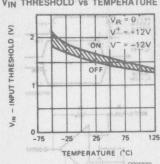
NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

	DQ163			
		Vor pV .Vot = oV		
		. V8.7 0V V8.7 - 84	01±	
	DG (52 DG (52			
				PR

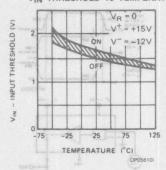
26 -60 -26 0 26 50 75 100 126



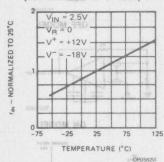
VIN THRESHOLD VS TEMPERATURE



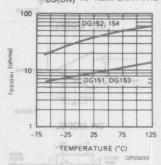
#### VIN THRESHOLD VS TEMPERATURE



#### TDS(ON) VS TEMPERATURE (Normalized to 25°C Value)

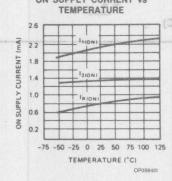


TDS(ON) VS TEMPERATURE

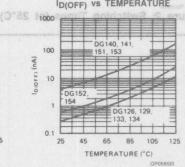


#### **ALL CIRCUITS**

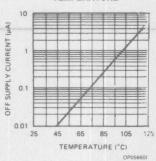
ON SUPPLY CURRENT VS



ID(OFF) VS TEMPERATURE



OFF SUPPLY CURRENT vs **TEMPERATURE** 



## DG139, DG142-DG146, DG161-DG164 DUAL JFET Analog Switch

## **BINTERSIL**

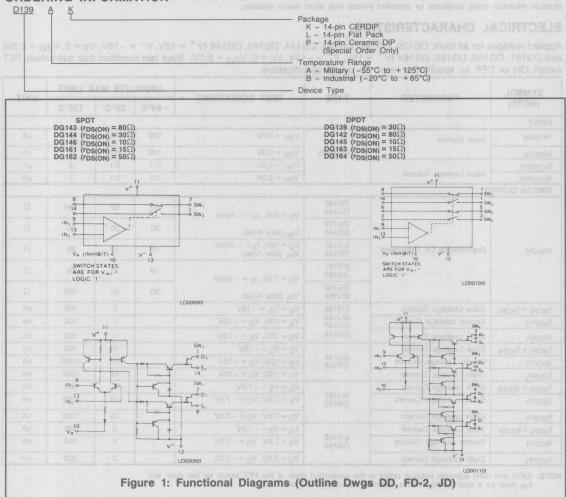
#### GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V<sub>R</sub> terminal.

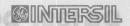
#### **FEATURES**

- Each Channel Complete Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, 1mW
- Switches Analog Signals Up to 20 Volts Peak-to-Peak
- Low r<sub>DS(ON)</sub>, 10 Ohms Max on DG145 and DG146

#### ORDERING INFORMATION



## DG139, DG142-DG146, DG161-DG164



#### ABSOLUTE MAXIMUM RATINGS

V <sup>+</sup> - V <sup>-</sup>	V <sub>IN1</sub> – V <sub>R</sub> ±6V
V <sub>S</sub> - V <sup>-</sup> 30V	V <sub>IN2</sub> - V <sub>R</sub> ±6V
V <sup>+</sup> - V <sub>S</sub>	Power Dissipation (Note)750mW
Vs - Vp±22V	Current (any terminal)
V <sub>B</sub> - V <sup>-</sup> 21V	Storage Temperature65°C to +150°C
V <sup>+</sup> - V <sub>B</sub> Wint added and reward T10 wall 17V	Operating Temperature55°C to +125°C
V <sup>+</sup> - V <sub>IN1</sub> or V <sub>IN2</sub>	Lead Temperature (Soldering, 10sec)300°C
VINI1 - VINI2 ±6V	

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG139, DG142, DG143, DG144, DG145, DG146 (V $^+$  = 12V, V $^-$  = -18V, V<sub>R</sub> = 0, V<sub>IN2</sub> = 2.5V) and DG161, DG162, DG163, DG164 (V $^+$  = 15V, V $^-$  = -15V, V<sub>R</sub> = 0, V<sub>IN2</sub> = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

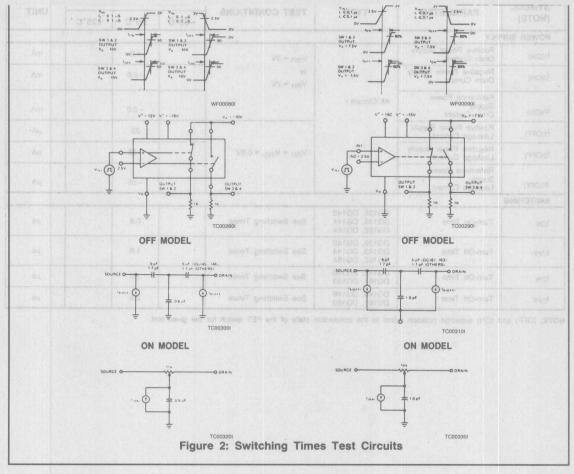
SYMBOL	DARAMETER TYPE TEST CONDITIONS		0	ABSOL	ABSOLUTE MAX LIM		
(NOTE)			-55°C	25°C	125°C	UNIT	
INPUT	70.00	TORIS			(T) (T) (T) (T) (T)	1098	
IN1(ON)	Input Current	NEOT SALOG	V <sub>IN1</sub> = 3.0V	120	60	60 00	μΑ
IN2(ON)	Mar = M	All Circuits	V <sub>IN2</sub> = 2.0V	120	60	60	μΑ
IN1(OFF)			V <sub>IN1</sub> = 2.0V	0.1	0.1	2	μΑ
IN2(OFF)	Input Leakage Current		V <sub>IN2</sub> = 3.0V	0.1	0.1	2	μΑ
SWITCH OUTPU	JT.				70.		
		DG142 DG143	V <sub>D</sub> = 10V, I <sub>S</sub> = -10mA	80	80	150	Ω
		DG139 DG144	V <sub>IN</sub> (See Note)	30	30	60	Ω
rDS(ON) Drain-Source On Resistance	DG145 DG146	V <sub>D</sub> = 10V, I <sub>S</sub> = -10mA V <sub>IN</sub> (See Note)	10	10	20	Ω	
		DG161 DG163	V <sub>D</sub> = 7.5V, I <sub>S</sub> = -10mA	15	15	30	Ω
		DG162 DG164	V <sub>IN</sub> (See Note)	50	50	100	Ω
ID(ON) + IS(ON)	Drive Leakage Current	DG139	$V_D = V_S, = -10V$		2	100	nA
IS(OFF)	Source Leakage Current	DG142 DG143	$V_S = 10V, V_D = -10V$		1	100	nA
ID(OFF)	Drain Leakage Current	DG144	$V_D = 10V, V_S = -10V$		1 1	100	nA
ID(ON) + IS(ON)	Drive Leakage Current		$V_D = V_S = -10V$		2	100	nA
IS(OFF)	Source Leakage Current	DG145 DG146	$V_S = 10V, V_D = -10V$	Service of the servic	10	1000	nA
ID(OFF)	Drain Leakage Current		$V_D = 10V, V_S = -10V$		10	1000	nA
ID(ON) + IS(ON)	Drive Leakage Current		$V_D = V_S = -7.5V$	172-	2	500	nA
IS(OFF)	Source Leakage Current	DG161 DG163	$V_S = 7.5V$ , $V_D = -7.5V$		10	1000	nA
ID(OFF)	Drain Leakage Current		$V_D = 7.5V, V_S = -7.5V$		10	1000	nA
ID(ON) + IS(ON)	Drive Leakage Current		$V_D = V_S = -7.5V$		2	500	nA
Is(OFF)	Source Leakage Current	DG162 DG164	$V_S = 7.5V$ , $V_D = -7.5V$		2	200	nA
I <sub>D</sub> (OFF)	Drain Leakage Current		$V_D = 7.5V, V_S = -7.5V$		2	200	nA

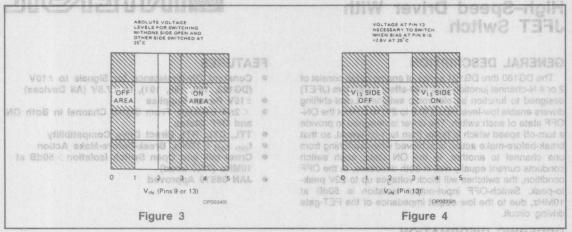
**NOTE:** (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.  $V_{IN}$  must be a step function with a minimum slew-rate of  $1V/\mu s$ .

### **ELECTRICAL CHARACTERISTICS (CONT.)**

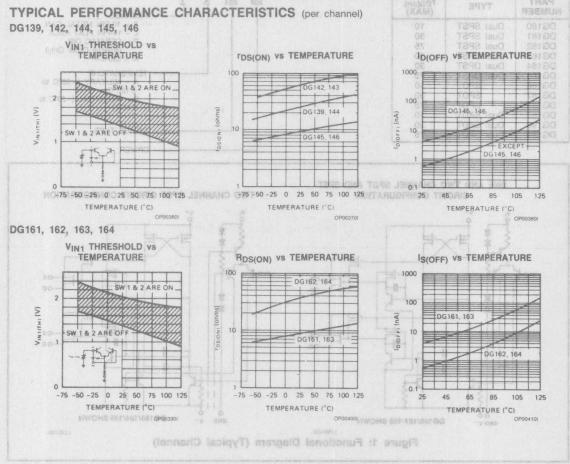
SYMBOL	PER 100 100 100 100			ABSOL	LUTE MAX	LIMIT	
(NOTE)	PARAMETER TYPE TEST CONDITIONS		-55°C	25°C	125°C	UNIT	
POWER SUI	PPLY	14.00		P-10/	B.F.		
1(ON)	Positive Power Supply Drain Current	Seal and the seal of the seal	V <sub>IN1</sub> = 3V	100 mm	4.0		mA
12(ON)	Negative Power Supply Drain Current	T. Marie	or V <sub>IN1</sub> = 2V	1 (1 (1 (1 (1 (1 (1 (1 (1 (1 (1 (1 (1 (1	-2.0	phino phino	mA
I <sub>R(ON)</sub>	Reference Power Supply Drain Current	All Circuits	150,000W		-2.0		mA
I <sub>1</sub> (OFF)	Positive Power Supply Leakage Current				25		μΑ
I <sub>2(OFF)</sub>	Negative Power Supply Leakage Current	(HB)	V <sub>IN1</sub> = V <sub>IN2</sub> , = 0.8V	0	-25		μΑ
I <sub>R(OFF)</sub>	Reference Power Supply Leakage Current			1 250	-25	9-	μΑ
SWITCHING				1		REE NOT	
ton	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164	See Switching Times	4	0.8		μs
<sup>t</sup> OFF	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164	See Switching Times	MODEL	1.6		μs
ton	Turn-On Time	DG145, DG146 DG161, DG163	See Switching Times		1.0		μs
toff	Turn-Off Time	DG145, DG146 DG161, DG163	See Switching Times	Der a	2.5		μs

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.





NOTE 1: An example of Absolute Minimum Differential Voltage,  $V_9 - V_{13}$ , is when  $V_9 = 3V$  and  $V_{13} = 2.5V$ , the  $V_9$  side of the switch is OFF at 25°C. Conversely, when  $V_9 = 2V$  and  $V_{13} = 2.5V$ , the  $V_9$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and the  $V_{13}$  side of the switch is OFF and  $V_{13}$ 



## DG180-191

## High-Speed Driver With JFET Switch

## 

#### **GENERAL DESCRIPTION**

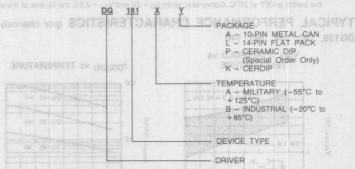
The DG180 thru DG191 series of analog gates consist of 2 or 4 N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output isolation is 50dB at 10MHz, due to the low output impedance of the FET-gate driving circuit.

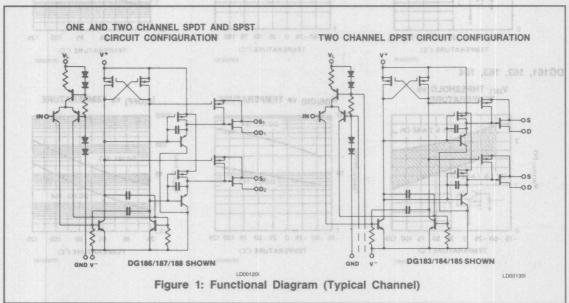
#### **FEATURES**

- Constant ON-Resistance for Signals to ±10V (DG182, 185, 188, 191), to ±7.5V (All Devices)
- ±15V Power Supplies
- < 2nA Leakage From Signal Channel in Both ON and OFF States
- TTL, DTL, RTL Direct Drive Compatibility
- ton, toff < 150ns, Break-Before-Make Action
- Cross-talk and Open Switch Isolation > 50dB at 10MHz (75Ω Load)
- JAN 38510 Approved

#### ORDERING INFORMATION

PART NUMBER	TYPE	rDS(on) (MAX)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75



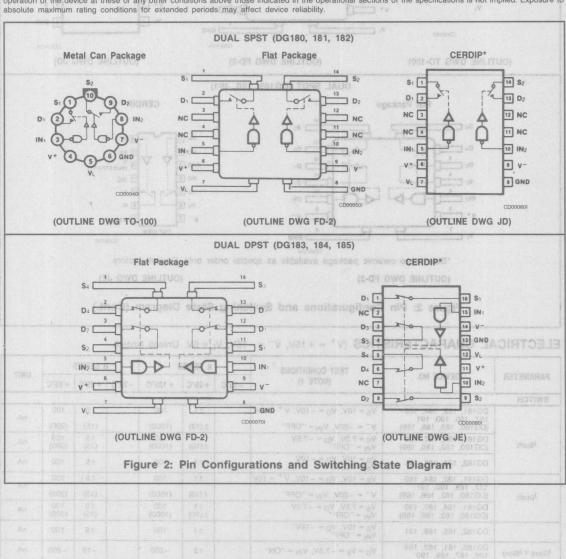


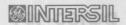
3

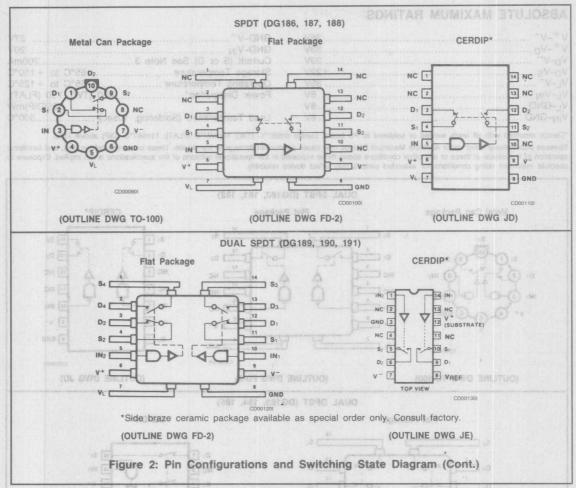
V <sup>+</sup> -V <sup>-</sup>	36V	GND-V <sup>-</sup>
V <sup>+</sup> -V <sub>D</sub>	33V	GND-V <sub>IN</sub> 20V
V <sub>D</sub> -V*-		Current (S or D) See Note 3200mA
V <sub>D</sub> -V <sub>S</sub>		Storage Temperature65°C to +150°C
V <sub>L</sub> -V	36V	Operating Temperature55°C to +125°C
V <sub>L</sub> -V <sub>IN</sub>	8V	Power Dissipation*
V <sub>L</sub> -GND	8V	825(DIP)mW
VIN-GND	8V	Lead Temperature (Soldering, 10sec)300°C

ABSULUIE MAXIMUM HATINGS

\*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.







#### ELECTRICAL CHARACTERISTICS (V + = +15V, V = -15V, VL = 5V, Unless Noted)

	The first of the second	TEST CONDITIONS	A SERIES	40-0	В	SERIES		
PARAMETER	DEVICE NO.	(NOTE 1) -55°C	+ 25°C	+ 125°C	-20°C	+ 25°C	+ 85°C	UNIT
SWITCH	18 (4)	2 0 -	- manager ma	and green	annual .	THE R		Sille
	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V$ , $V_D = -10V$ , $V^+ = 10V$ $V^- = -20V$ , $V_{IN} = "OFF"$	±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
Is(off)	DG181, 184, 187, 190 (DG180, 183, 186, 189)	V <sub>S</sub> = 7.5V, V <sub>D</sub> = -7.5V V <sub>IN</sub> = "OFF"	±1. ±(10)	100 (1000)	(TUO)	±5 (15)	100 (300)	nA
	DG182, 185, 188, 191	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V V <sub>IN</sub> = "OFF"	o 0# 1519	100	Fig	±5	100	nA
I <sub>D(off)</sub>	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V$ , $V_D = -10V$ , $V^+ = 10V$ $V^- = -20V$ , $V_{IN} = "OFF"$	±1 ±(10)	100 (1000)	77	±5 (15)	100 (300)	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	V <sub>S</sub> = 7.5V, V <sub>D</sub> = -7.5V V <sub>IN</sub> = "OFF"	±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG182, 185, 188, 191	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V V <sub>IN</sub> = "OFF"	±1	100		±5	- 100	nA
I <sub>D(on)</sub> + I <sub>S(on)</sub>	DG180, 181, 183, 184 186, 187, 189, 190	$V_D = V_S = -7.5V$ , $V_{IN} = "ON"$	±2	-200		-10	-200	nA
	DG182, 185, 188, 191	$V_D = V_S = -10V, V_{IN} = "ON"$	±2	-200		-10	-200	nA

### ELECTRICAL CHARACTERISTICS (CONT.)

	JAIRTRUGIR	TEST CONDITIONS		A SERIE	S		B SERIES	3	
PARAMETER	DEVICE NO.	(NOTE 1)	-55°C	+ 25°C	+ 125°C	-20°C	+ 25°C	+85°C	UNIT
INPUT	4 3 684 3 08- 3	021 + U 03 + U 05-							
INL	ALL BY BY	V <sub>IN</sub> = 0V	-250	-250	-250	-250	-250	-250	μΑ
INH	ALL DE CE	V <sub>IN</sub> = 5V		10	20	V	10	20	μΑ
DYNAMIC	001 001	75 75 100				V	01- = 01	/	SBTDC
52 31	10Ω Switches	10 40 1 20		300		V	350		28180
ton e	30Ω Switches	30 08 08		150		V	180		18100
Ω 00	75Ω Switches	See switching time test circuit		250		V	300		ns ns
toff	10Ω Switches	10 10 20		250		. V	300	19 113	88120
Ω at	$30\Omega$ and $75\Omega$ Switches	08 00 08	The Marie of	130	y I	V	150		VALDO
C <sub>S(off)</sub>	DG181, 182, 184, 185,	$V_S = -5V$ , $I_D = 0$ , $f = 1MHz$			typical (21	typical)	07- = -10	7	BETER
C <sub>D(off)</sub>	187, 188, 190, 191 (DG180, 183, 186 189)	$V_D = +5V$ , $I_S = 0$ , $f = 1MHz$			typical (17		15-00	/ 1	pF
CD(on) + CS(on)	(Da 160, 163, 160 163)	V <sub>D</sub> = V <sub>S</sub> = 0, f = 1MHz		1	4 typical (1	7 typical)	7 7	7	08180
OFF Isolation						MHz (Se	e Note 2	2)	10050
SUPPLY				Partition of the last					
tollowing witches and	DG180, 181, 182, 189 190, 191	122 gates to seed 15 tests above. F S.Vanaloo(beak) - Ve where Ve =	E bas O	1.5	ir-to-pook h	ee votos	1.5	spens Cal	the 7
vit va	DG183, 184, 185	(2 - qV) nomine 1207 a bina lange	olene (al	0.1	micuro VOI	D. D. O.	0.1	(or 755)	= 5.0V
	DG186, 187, 188			0.8		- Services	0.8		-
	DG180, 181, 182, 189 190, 191	181/182 Snown)	(DETEC)	-5.0	10N" (30)	-01 'F	-5.0	t hugai	olgo
1-	DG183, 184, 185	V <sub>IN</sub> = 5V	- (%)	-4.0	m <sub>k</sub>		-4.0	VE	Hoerd
	DG186, 187, 188	3.0		-3.0	4		-3.0	8.8	rugia)/iii
ROTHWS OUTPUT	DG180, 181, 182, 183 184, 185, 189, 190, 191	BWITCH 6. I		4.5	Assistance	- on a series of	4.5		mot>
040-	DG186, 187, 188	TURNS		3.2			3.2	- 1	
IGND	ALL	lon, Vo + 100 pm		-2.0			-2.0	-sv	mA
	DG180, 181, 182, 189 190, 191	TUBEL TUBEL	- CY	1.5		T	1.5		G-681
14603 783	DG183, 184, 185			3.0	BIRME	3	3.0	0	CHALL
A N	DG186, 187, 188	vo I A		0.8	1	not ye	0.8	4 11	1
moraris 134	DG180, 181, 182, 189 190, 191	T MODERN TO A CALL OF	1981	-5.0			-5.0		
1-	DG183, 184, 185	VIN = 0V set om f pains	3: Swi	-5.5	9		-5.5	TALE OF	
	DG186, 187, 188			-3.0			-3.0	1111111	
liposis eser emit miotevav lutili	DG180, 181, 182, 183 184, 185, 189, 190, 191	waveloute as shown. Note that Visin to capacitance may result in epistre a	hugai aiga	4.5	lanco # gV i	of nwork	4.5	to higheo	
ΙL	DG186, 187, 188	North Total Yan Schuldstags V		3.2			3.2		I al Old
IGND	ALL			-2.0			-2.0		-

NOTES 1. See Switching State Diagrams for V<sub>IN</sub> "ON" and V<sub>IN</sub> "OFF" Test Conditions.
2. Off Isolation typically > 55dB at 1MHz for DG180, 183, 186, 189.
3. Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2ms Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

Channels 1 & 2	V0.5 = "MO" MIV
	V8.0 = "VO" MV

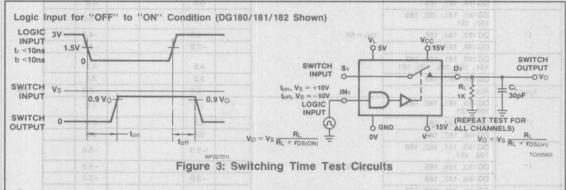
DUAL SPSY-DG180/181/182



#### ELECTRICAL CHARACTERISTICS (CONT.) MAXIMUM RESISTANCES (rDS(ON) MAX)

DEVICE NUMBER	CONDITIONS (Note 1) V+ = 15V, V- = -15V, V <sub>L</sub> = 5V		MILITAR	Y TEMPE	RATURE		IDUSTRIA MPERATU		UNIT
NUMBER	V = 15V, V =	= -15V, VL = 5V	-55°C	+ 25°C	+ 125°C	-20°C	+ 25°C	+85°C	TUSH
DG180	$V_D = -7.5V$	085- 085-	10	10	20	15	15	25	Ω
DG181 09	$V_D = -7.5V$	07 1	30	30	60	50	50	JA 75	Ω
DG182	$V_D = -10V$		75	75	100	100	100	150	Ω
DG183	$V_D = -7.5V$	000	10	10	20	15	158 5	25	Ω
DG184	$V_D = -7.5V$	oer	30	30	60	50	50	08 75	ne Ω
DG185	$V_D = -10V$	Is = -10mA	3 000 75 1 G	75	2 9/150	100	100	150	Ω
DG186	$V_D = -7.5V$	250	10	10	20	15	150 S	25	nol Ω
DG187	$V_D = -7.5V$	V <sub>IN</sub> = "ON"	30	30	60	50	50	75	Ω
DG188	VD = -10V (OR) (18) (18)	VI B	75	75	150	100	100	150	Ω
DG189	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG190	$V_D = -7.5V$	111	30	30	60	50	50	50	Ω
DG191	$V_D = -10V$	Typically > 50d	75	75	150	100	100	150	Ω

**APPLICATION HINT** (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω (refer  $l_D$  and  $l_S$  tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that  $V^- \le V_{ANALOG}(peak) - V_{p}$  where  $V_p = 7.5V$  for the 10Ω and 30Ω switches and  $V_p = 5.0V$  for 75Ω switches e.g., -10V minimum (-peak) analog signal and  $-75\Omega$  switch ( $V_p = 5V$ ), requires that  $V^- \le -10V - 5V = -15V$ .



Switch output waveform shown for  $V_S$  = constant with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

### DUAL SPST-DG180/181/182

TEST CONDITIONS

DG180/181/182						
V <sub>IN</sub> ''ON'' = 0.8V	All Channels					
V <sub>IN</sub> ''OFF'' = 2.0V	All Channels					

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

#### SPDT-DG186/187/188

**TEST CONDITIONS** 

DG186/1	187/188	
V <sub>IN</sub> ''ON'' = 2.0V	Channel 1	
V <sub>IN</sub> "ON" = 0.8V	Channel 2	
V <sub>IN</sub> "OFF" = 2.0V	Channel 2	
V <sub>IN</sub> "OFF" = 0.8V	Channel 1	

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

#### **DUAL DPST-DG183/184/185**

TEST CONDITIONS

DG183/184/185						
V <sub>IN</sub> ''ON'' = 2.0V	All Channels					
V <sub>IN</sub> ''OFF'' = 0.8V	All Channels					

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

### DUAL SPDT-DG189/190/191

TEST CONDITIONS

	DG189/1	90/191				
Γ	V <sub>IN</sub> ''ON'' = 2.0V	Channels	1	&	2	
1	V <sub>IN</sub> "ON" = 0.8V	Channels	3	&	4	
1	V <sub>IN</sub> "OFF" = 2.0V	Channels	3	&	4	
L	V <sub>IN</sub> "OFF" = 0.8V	Channels	1	&	2	

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

## **DG200/IH5200**

## **CMOS Dual SPST Analog Switches**

## GENERAL DESCRIPTION

The DG200/IH5200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

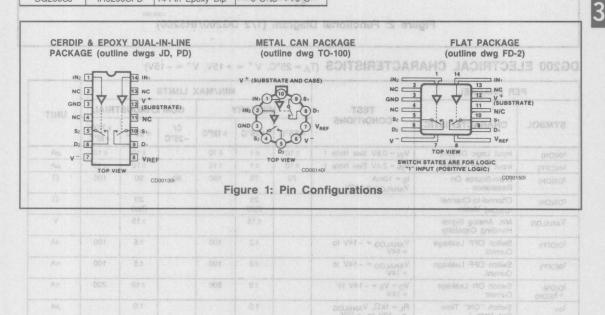
The DG200 is completely spec and pin-out compatible with the industry standard device, while the IH5200 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

#### **FEATURES**

- Switches Greater Than 28Vpp Signals With ±15V Supplies
- Break-Before-Make Switching toff 250ns, ton 700ns Typical
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200)
- Improved Performance Version (IH5200)

#### ORDERING INFORMATION

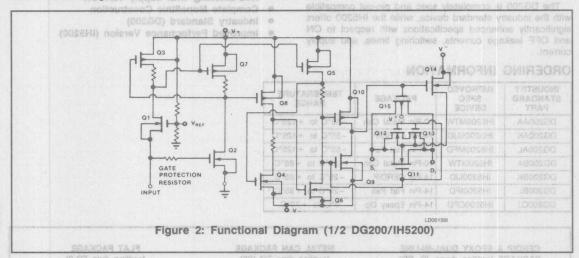
INDUSTRY STANDARD PART	SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG200AA	IH5200MTW	10-Pin Metal Can	-55°C to +125°C
DG200AK	IH5200MJD	14-Pin CERDIP	-55°C to +125°C
DG200AL	IH5200MFD	14-Pin Flat Pak	-55°C to +125°C
DG200BA	IH5200ITW	10-Pin Metal Can	-25°C to +85°C
DG200BK	IH5200IJD	14-Pin CERDIP	-25°C to +85°C
DG200BL	IH5200IFD	14-Pin Flat Pak	-25°C to +85°C
DG200CJ	IH5200CPD	14-Pin Epoxy Dip	0°C to +70°C



V <sup>+</sup> -V <sup>-</sup>	Storage
V <sup>+</sup> -V <sub>D</sub>	Operati
V <sub>D</sub> -V <sup>-</sup> <30V	Lead T
Vp-Vs < ±22V	Power
V <sub>IN</sub> -GND< 20V	(All Lead
Current (Any Terminal)>30mA	(All Lead

Storage Temperature	65°C	to +150°C
Operating Temperature	-55°C	to +125°C
Lead Temperature (Soldering, 10sec)	034 4	300°C
Power Dissipation	35/1/00	450mW
(All Leads Soldered to a P.C. Board.) Derate	6mW/°C	Above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



#### DG200 ELECTRICAL CHARACTERISTICS (TA = 25°C, V+ = +15V, V- = -15V)

PER CHANNEL		COM COM		977.	MIN/MAX	K LIMITS	3 m E		Dec.
SYMBOL	CHARACTERISTIC	TEST (6	MILITARY C				COM'L/INDUSTRIAL		
		CONDITIONS	-55°C	+25°C	+ 125°C	0/ -25°C	+25°C	+70°C/ +85°C	UNIT
IN(ON)	Input Logic Current	V <sub>IN</sub> = 0.8V See Note 1	±10	±1	±10		±10	±10	μΑ
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 2.4V See Note 1	±10	±1	±10		±10	±10	μΑ
rDS(ON)	Drain-Source On Resistance	Is = 10mA Vanalog = ±10V	70	70	100	80	80	100	Ω
rDS(ON)	Channel-to-Channel rDS(ON) Match			25 (typ)			30 (typ)		Ω
VANALOG	Min. Analog Signal Handling Capability			±15			±15		٧
I <sub>D(OFF)</sub>	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -14V to +14V		±2	100		±5	100 -	nA
IS(OFF)	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -14V to +14V		±2	100		±5	100	nA
ID(ON) + IS(ON)	Switch ON Leakage Current	$V_D = V_S = -14V$ to +14V		±2	200		±10	200	nA
ton	Switch ''ON'' Time See Note 1	$R_L = 1k\Omega$ , $V_{ANALOG}$ = -10V to +10V See Fig. 3		1.0			1.0		μs
toff	Switch "OFF" Time	$R_L = 1k\Omega$ , VANALOG = -10V to +10V See Fig. 3		0.5			0.5		μs
Q(INJ.)	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV

SYMBOL	or all save	TEST	MILITARY			COM'	UNIT		
	CHARACTERISTIC		-55°C	+ 25°C	+ 125°C	0/ -25°C	+ 25°C	+70°C/ +85°C	
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$ , $R_L = 100\Omega$ , $C_L \le 5pF$ See Fig. 5 (Note 1)	-0-	54 (typ)	-10	1	50 (typ)	1 -	dB
lv1	+ Power Supply Quiescent Current	V <sub>IN</sub> = 0V or V <sub>IN</sub> = 5V	1000	1000	2000	1000	1000	2000	μΑ
I <sub>V2</sub>	- Power Supply Quiescent Current		1000	1000	2000	1000	1000	2000	μΑ
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off	Figure	54 (typ)	elivarii sepo	"t" flous	50 (typ)	ugiil ut eta etani	dB

NOTE 1: Pull Down Resistor must be  $\leq 2k\Omega$ NOTE 2: Typical values are for design aid only, not guaranteed and not subject to production testing.

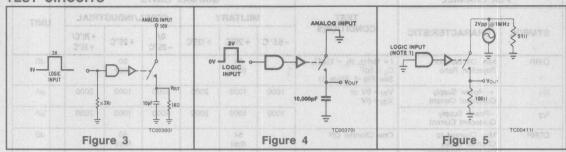
#### IH5200 ELECTRICAL CHARACTERISTICS (@ 25°C, V+ = +15V, V- = -15VREF open)

P	ER CHANNEL		MIN/MAX LIMITS						
SYMBOL CHARACTERISTIC		TEST	1	<b>ILITAR</b>	Y	COM'L/INDUSTRIAL			UNIT
	CONDITIONS	-55°C	+25°C	+ 125°C	0/ -25°C	+25°C	+70°C/ +85°C	ONIT	
IN(ON)	Input Logic Current	V <sub>IN</sub> = 0.8V	±10	±1	±10		±10	±10	μΑ
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 2.4V	±10	±1	10		±10	±10	μΑ
rDS(ON)	Drain-Source On Resistance	Is = 10mA VanaLog = ±10V	70	70	100	80	80	100	Ω.,
rDS(ON)	Channel-to-Channel rDS(ON) Match			25 (typ)			30 (typ)	10 to	Ω
VANALOG	Min. Analog Signal Handling Capability	01 - 27 -		± 15 (typ)	or e	0 8- 0	±15 (typ)		٧
I <sub>D(OFF)</sub>	Switch OFF Leakage Current	VanaLog = -14V to +14V		±1	50	1	±2	50	nA
IS(OFF)	Switch OFF Leakage Current	VANALOG = -14V to +14V		±1	50	(no)dl	±2	50	nA
ID(ON) + IS(ON)	Switch ON Leakage Current	$V_D = V_S = -14V$ to + 14V		±1	100	1	±2	100	nA
ton	Switch "ON" Time See Note 3	$R_L = 1k\Omega$ , $V_{ANALOG}$ = -10V to +10V See Fig. 3		0.7			0.8	60-60	μs
t <sub>off</sub>	Switch "OFF" Time	$R_L = 1k\Omega$ , $V_{ANALOG}$ = -10V to +10V See Fig. 3		0.25			0.4	THERETA VIETNET	μs
Q(INJ.)	Charge Injection	See Fig. 4		5 (typ)			10 (typ)	50	mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$ , $R_L = 100\Omega$ , $C_L \le 5pF$ See Fig. 5		54 (typ)			50 (typ)	o FESSIC godow	dB
l <sub>V1</sub>	+ Power Supply Quiescent Current	V <sub>IN</sub> = 0V or V <sub>IN</sub> = 5V	250	200	150	300	250	200	μΑ
lv2	-Power Supply Quiescent Current		10	10	100	10	10	100	μΑ
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

# DG200/IH5200

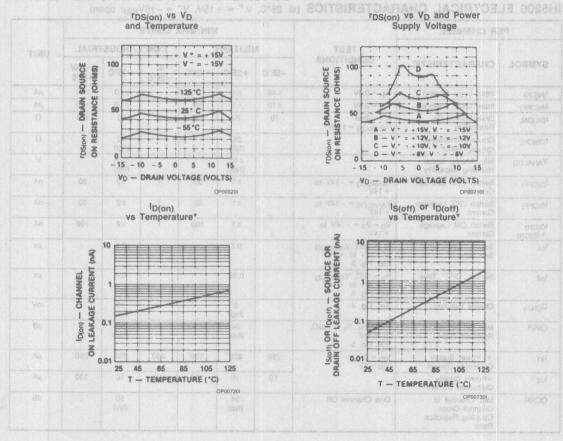


# TEST CIRCUITS



NOTE 3: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically -120µA.

#### TYPICAL PERFORMANCE CHARACTERISTICS



#### **APPLICATIONS**

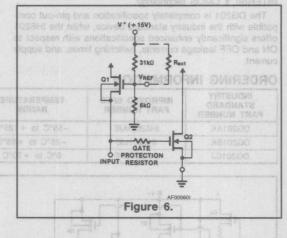
# Using the VREF Terminal

The DG200 has an internal voltage divider setting the TTL threshold on the input control lines for V $^+$  equal to +15V. The schematic shown here with nominal resistor values, gives approximately 2.4V on the V<sub>REF</sub> pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than  $\pm$  15V, then a resistor must be added between V  $\pm$  and the V<sub>REF</sub> pin, to restore  $\pm$  2.4V at V<sub>REF</sub>. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a  $\pm$  5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of  $\pm$  5V to  $\pm$  5V, no resistor is needed.

In general, the "low" logic level should be < 0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds > 1.5V, allowing the user to define the "low" as < 1.5V (consult factory). The VREF point should be set at least 2.6V above this "low" state, or to > 4.1V. An external resistor of  $27 k\Omega$  between V  $^+$  and VREF is required, for a +15 V supply.

V <sup>+</sup> Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+ 15	SCRIPTION	ENERAL DE
+12	100 les 10	The DOSOT/INS
	stlov-ric51 bevore	
	(34)	
	(27)	
	ed setap18 dans of	



3



Figure 2: Pin Configuration (Outline dwgs JE, PE)
DUAL-IN-LINE PACKAGE

Figure 1: Functional Diagram (1/4 DG201/H6201)

#### GENERAL DESCRIPTION

The DG201/IH5201 solid-state analog switches are designed using an improved, high-voltage CMOS monolithic technology. They provide performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG201 is completely specification and pin-out compatible with the industry standard device, while the IH5201 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current

# FEATURES to sgatlov lametri as and ooxed ant

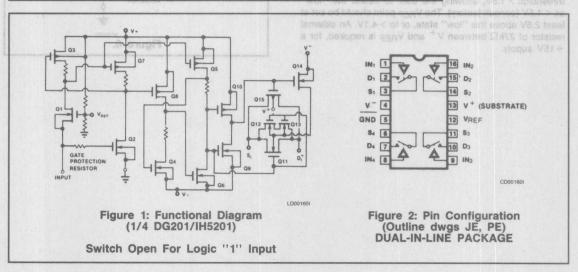
 Switches Greater Than 28V<sub>p-p</sub> Signals With ±15V Supplies

column of suitable values is given in the table. For logic

- Break-Before-Make Switching toff = 250ns, ton = Typically 500ns
- TTL. DTL. CMOS. PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG201)
- Improved Performance Version IH5201

#### ORDERING INFORMATION

INDUSTRY STANDARD PART NUMBER	IMPROVED SPEC PART NUMBER	TEMPERATURE RANGE	V8.0 > PACKAGE level ofgo
DG201AK	IH5201MJE	-55°C to +125°C	10 101016-Pin CERDIP W (1100)
DG201BK	IH5201IJE	-25°C to +85°C	16-Pin CERDIP
DG201CJ	IH5201CPE	0°C to +70°C	16-Pin Plastic DIP



V+       to VD       < 30V         VD to VT       < 30V         VD to VS       < ±22V         VREF to VIN       < 30V         VBCF to GND       < 20V	Current (Any Terminal) <a href="mailto:30ma">30ma</a> Storage Temperature -65°C to +150°C Operating Temperature -55°C to +125°C Lead Temperature (Soldering, 10sec)
V <sub>REF</sub> to GND< 20V	Derate 6mW/°C Above 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DG201 ELECTRICAL CHARACTERISTICS (TA = 25°C, V+ = +15V, V- = -15V)

PER CHANNEL		ed on by low "0" inpute: he			MIN/	MAX LIMI	TS		HA S STO	
		TEST (OS) - YOU	MILITARY DESIRED			COMMERCIAL				
SYMBOL	CHARACTERISTIC	CONDITIONS	-55°C	+ 25°C	+ 125°C	0°C	+ 25°C	+70°C/ +85°C	15201	
IN(ON)	Input Logic Current	V <sub>IN</sub> = 0.8V See Note 1	10	±1	10	±1	±1	10	μΑ	
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 2.4V See Note 1	10	±1	10	±1	±1	10	μΑ	
RDS(ON)	Drain-Source On Resistance	Is = 10mA VANALOG = ±10V	08	80	125	100	010013	DARAH25	08120	
RDS(ON)	Channel to Channel RDS(ON) Match	1 01 1	1	25 (typ)	. V8.0	= VIV	30 (typ)	Input Logic	(AO)MI	
VANALOG	Analog Signal	1 01 5	1	±15	V4.5	View or	±15	laput Legic	(HAWH)	
0	Handling Capability	75 190 100	76	(typ)	Ami	l'az gl	(typ)	Distri-Source	DSCON	
ID(OFF)	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -14V to +14V		±1	100	YAMAY	±5 tennerio	Channel to	nA (MCNRGF	
IS(OFF)	Switch OFF Leakage	VANALOG = -14V to		±1	100		±5	SM (M100 A	nA	
3(0)17	Current	+14V ers					1	Analog Sign	COD JAMAS	
ID(ON)	Switch ON Leakage	$V_D = V_S = \pm 14V$ (90)		±2	200		±5	200	nA	
+ IS(ON)	Current	08   8.01	1.2.1	61 V	N - # 80	IAMAY	Leakage	Switch OFF	\magoo	
ton	Switch "ON" Time	$R_L = 1k\Omega$ , $V_{ANALOG}$		1.0		(B) + 1	1.0	Current	μs	
An.	See Note 2	= -10V to +10V See Figure 3			Apti = 5	= CV	eakage	Switch ON 1 Current	(MO)O	
toff	Switch "OFF" Time See Note 2	$R_L = 1k\Omega$ , $V_{ANALOG}$ = -10V to +10V See Figure 3		0.5	hΩ, Varus 3V to + tV Igure 3	1-2	0.5	Switch ''ON' See Note 2	μs	
Q(INJ.)	Charge Injection	See Figure 4		15 (typ)	KΩ, V <sub>ANS</sub> N to + id	n jA	20 (typ)	Switch "OFF See Note 2	mV	
OIRR	Min. Off Isolation	$f = 1MHz$ , $R_L = 100\Omega$ ,		54	gure 3	See F	50		dB	
Vm	Rejection Ratio	C <sub>L</sub> ≤ 5pF See Figure 5		(typ)	\$ .g	H see	(typ)	Charge Inject	CLMI)S	
Idas	+ Power Supply Quiescent Current	V <sub>IN</sub> = 0V to 5V AB (qui)	2000	1000	2000	2000	1000	nal ta 2000	μА	
Iā	-Power Supply		2000	1000	2000	2000	1000	2000	μΑ	
Ast	Quiescent Current	poer   909   087	1000		Và oi Việ	= priV	pply	* Power St	6	
CCRR	Min. Channel to	One Channel Off		54	FILIP		50	Outescent O	dB	
Au	Channel Cross Coupling Rejection Ratio	05 001 01	10	(typ)			(typ)	-Power Sup Outrepent C	ő	

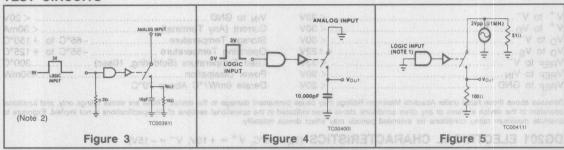
NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

NOTE: Pull Doron resistor must be  $\stackrel{\vee}{\times} 2 h \Omega$  NOTE: Typical values are for design aid only, not guaranteed and not subject to production fasting

# DG201/IH5201

# **BINTIERSIL**

#### **TEST CIRCUITS**



NOTE 2: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically -120µA.

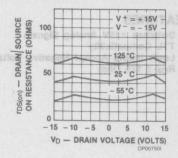
# IH5201 ELECTRICAL CHARACTERISTICS (TA = 25°C, V+ = +15V, V- = -15V)

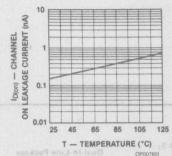
	PER CHANNEL	11 01 11	- Indiana		MIN/	MAX LIMI	rs		
Au	01 12	TEST FE	01	MILITARY	es8 VAS	S = veV	COMME	RCIAL	UNIT
SYMBOL	CHARACTERISTIC	CONDITIONS	-55°C	+ 25°C	+ 125°C	0°C	+ 25°C	+70°C/ +85°C	POSICIN
IN(ON)	Input Logic Current	V <sub>IN</sub> = 0.8V	1	1	10	1	1	10	μΑ
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 2.4V	1	1	10	1	1	10	μΑ
RDS(ON)	Drain-Source On Resistance	I <sub>S</sub> = 10mA VANALOG = ±10V	75	75	100	100	100	125	Ω
RDS(ON)	Channel to Channel RDS(ON) Match	007 15		25 (typ)	h1 - = 510	AMAY -	30 (typ)	Current Switch OFF	Ω
VANALOG	Analog Signal Handling Capability	90S Sw		± 15 (typ)	VACT = pl	(#1 + 1   = 8V	± 15 (typ)	Switch ON	V
I <sub>D(OFF)</sub> / I <sub>S(OFF)</sub>	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -14V to +14V		±0.5	50	# 0 FF	±2	50	onA .
ID(ON) + IS(ON)	Switch ON Leakage Current	$V_D = V_S = \pm 14V$		±0.5	100	*-1 See F	±2	\$ 86 100	nA
ton	Switch "ON" Time See Note 2	$R_L = 1k\Omega$ , $V_{ANALOG}$ = -10V to +10V See Figure 3		0.700	RD VARA N to + N Sure G	Comment of the second	0.8	Sea Note 2	μs
toff	Switch "OFF" Time See Note 2	$R_L = 1k\Omega$ , $V_{ANALOG}$ = -10V to +10V		0.35	a sugi	A said	0.4101	Charge Inset	μs
80	69	See Figure 3		1 ,7300	HA BE	-		eet tho et M.	RAIO
Q(INJ.)	Charge Injection	See Fig. 4		5 (typ)	S earls	Bee F	10 (typ)	ist persales	mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$ , $R_L = 100\Omega$ , $C_L \le 5pF$ See Figure 5, (Note 1)	2000	54 (typ)	VB of V6	= MM =	and the boundary of the Contract of	A Power St Quiescent C -Power Sta	dBO
iđ	+ Power Supply Quiescent Current	V <sub>IN</sub> = 0V to 5V	1000	750	600	1500	7000	1000	μΑ
Iā	-Power Supply Quiescent Current	(98)	10	10	100	20		10 191200 19 protono	μΑ
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off (Note 1)	heldus icr	54 (typ)	rishing for	ylari bie	50 (typ)	ens sáulav leak	dB T : stor

**NOTE:** Pull Down resistor must be  $\leq 2k\Omega$ 

NOTE: Typical values are for design aid only, not guaranteed and not subject to production testing.

# TYPICAL PERFORMANCE CHARACTERISTICS



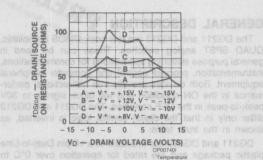


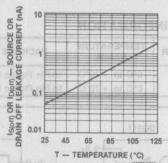
# **APPLICATIONS** Using the VREF Terminal

The DG201 has an internal voltage divider that sets the TTL threshold on the input control lines for V + = 15V. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V<sub>REF</sub> pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

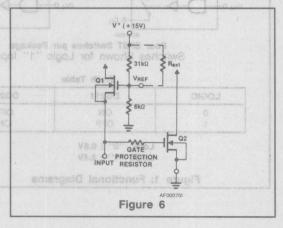
If the power supply voltage is less than +15V, then a resistor needs to be added between V+ and VREF pin, to restore +2.4V at VRFF. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to +5V, no resistor is needed.

In general, the "low" logic level should be < 0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic 'low' level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds > 1.5V(consult factory). The V<sub>REF</sub> point should be set at least 2.6V above this "low" state, or to > 4.1V. An external resistor of  $27k\Omega$  and  $V_{RFF}$  is required, for a + 15V supply.





V <sup>+</sup> Supply (V)	TTL Resistor (kΩ)	CMOS Resisto (kΩ)
+ 15	(C p)	1
+ 12	100	
+ 10	51	print -
+9	(34)	34
+8	(27)	27
+7	18,	18



# DG211/DG212 SPST 4-Channel Analog Switch



#### **GENERAL DESCRIPTION**

The DG211 and DG212 are low cost, CMOS monolithic, QUAD SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

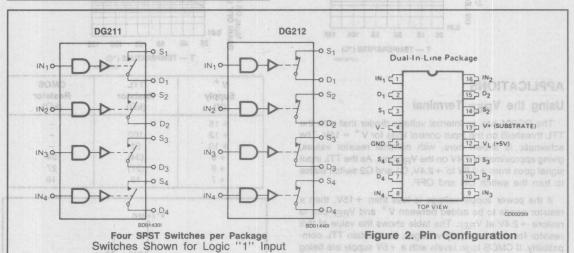
DG211 and DG212 are available in a 16-pin Dual-In-Line plastic package and are rated for operation over 0°C to 70°C.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG211CJ	0°C to +70°C	16-Pin Plastic DIP
DG212CJ	0°C to +70°C	16-Pin Plastic DIP

# **FEATURES**

- Switches ±15V Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- RoN ≤ 175 Ohm



Truth Table

LOGIC	DG211	DG212
0	ON	OFF O
1	OFF	ON

Logic ''0'' ≤ 0.8V Logic ''1'' ≥ 2.4V

Figure 1: Functional Diagrams

#### ABSOLUTE MAXIMUM RATINGS

V+ to V	V81 ×	V2+	36V
VIN to Ground	- 4 9		V-, V+
V <sub>L</sub> to Ground			0.3V, 25V
Vs or Vp to V+			0, -36V
Vs or VD to V			0, 36V
V <sup>+</sup> to Ground			
V <sup>-</sup> to Ground	0)		25V
Current, Any Terminal Exc	cept S or D		30mA
Continuous Current, S or	D		20mA

Peak Current, S or Dilovi awards as anotevow tugal algol
(Pulsed at 1msec, 10% duty cycle max) 70mA
Storage Temperature65°C to +125°C
Operating Temperature 0°C to +70°C
Lead Temperature (Soldering, 10sec)300°C
Power Dissipation (Package)*
16 Pin Plastic DIP**470mW

<sup>\*</sup>Device mounted with all leads soldered or welded to PC board.

# ELECTRICAL CHARACTERISTICS (TA = 25°C)

			T CONDITIONS	Shell les-			
SYMBOL	PARAMETER	V <sub>1</sub> = +15V, V <sub>2</sub> = -15V, V <sub>L</sub> = +5V, GND		MIN <sup>1</sup>	TYP <sup>2</sup>	MAX	UNIT
SWITCH							
VANALOG	Analog Signal Range	$V^{-} = -15V, V_{L}$	= +5V	-15	and the same of th	15	V
RDS(ON)	Drain-Source On Resistance		V <sub>D</sub> = ±10V, V <sub>IN</sub> = 2.4V — DG212 I <sub>S</sub> = 1mA, V <sub>IN</sub> = 0.8V — DG211		115	175	Ω
lov m	Source OFF Leakage Current	V <sub>IN</sub> = 2.4V	$V_S = 14V, V_D = -14V$		0.01	5.0	1
IS(off)	Source OFF Leakage Current	DG211 $V_S = -14V, V_D = 14V$		-5.0	-0.02		
	Drain OFF Leakage Current	V <sub>IN</sub> = 0.8V DG212	$V_D = 14V, V_S = -14V$		0.01	5.0	
D(off)	Drain OFF Leakage Current	UGZIZ	$V_D = -14V, V_S = 14V$	-5.0	-0.02		
	Drain ON Leakage Current <sup>3</sup>	V <sub>S</sub> = V <sub>D</sub> = -14V, V <sub>IN</sub> = 0.8V, DG211 V <sub>IN</sub> = 2.4V, DG212			0.1	5.0	- ^
D(ON)	Drain ON Leakage Current			-5.0	-0.15		nA
INPUT						4	
	Input Current With Input	V <sub>IN</sub> = 2.4V V <sub>IN</sub> = 15V V <sub>IN</sub> = 0V		-10	-0.0004		μΑ
INH	Voltage High			Many-Rates In	0.003	1.0	
INL	Input Current With Input Voltage Low			-1.0	-0.0004		
DYNAMIC	V011					1	
ton	Turn-ON Time				460	1000	
t <sub>off1</sub>	Turn-OFF Time		Time Test Circuit <sup>5</sup> $1k\Omega$ , $C_L = 35pF$		360	500	ns
toff2		VS - 10V, HL -	1K22, OL - 30pr	URA IS TO	450		
C <sub>S(off)</sub>	Source OFF Capacitance	VS = OV, VIN =	5V, f = 1MHz <sup>2</sup>		5		pF
C <sub>D(off)</sub>	Drain OFF Capacitance	VD = OV, VIN =	5V, f = 1MHz <sup>2</sup>		5		
CD + S(on)	Channel ON Capacitance	$V_D = V_S = 0V$	$V_{IN} = 0V$ , $f = 1MHz^2$		16		
OIRR	OFF Isolation <sup>4</sup>	V - 5V 5	41.0		70	-41-4	
CCRR	Crosstalk (Channel to Channel)	$V_{IN} = 5V$ , $R_L = 1k\Omega$ , $C_L = 15pF$ , $V_S = 1VRMS$ , $f = 100kHz^2$			90	F	dB
SUPPLY	A' I					V8+	
1+	Positive Supply Current				.1	10	
- var-	Negative Supply Current	VIN = 0 and 2.4	4V		.1	. 10	μΑ
IL	Logic Supply Current				.1	10	

NOTES: 1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data

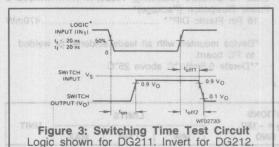
sheet.
2. For design reference only, not 100% tested.
3. ID(on) is leakage from driver into "ON" switch.

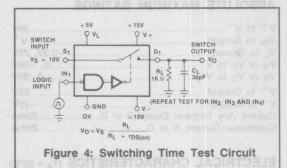
4. OFF Isolation =  $20\log \frac{V_S}{V_D}$ ,  $V_S$  = input to OFF switch,  $V_D$  = output.

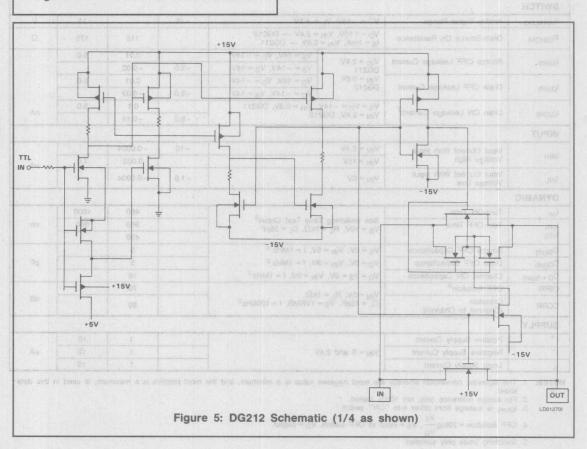
5. Switching times only sampled.

<sup>\*\*</sup>Derate 6.5mW/°C above 25°C

Switch output waveform shown for  $V_S$  = constant with logic input waveform as shown. Note the  $V_S$  may be + or + as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.







# **DGM181-191**

# High-Speed CMOS Analog Switch



#### GENERAL DESCRIPTION

The DGM181 family of CMOS monolithic switches utilizes intersil's latch-free junction isolated processing to combine the speed of the hybrid DG181 family with the reliability and low power consumption of a monolithic CMOS construction. These devices, therefore, are a cost effective replacement for the DG181 family.

The DGM181 family has a high state threshold of 2.4V; and a low state of +0.8V.

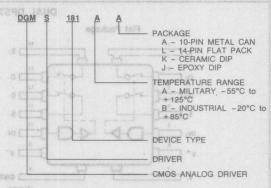
Very low quiescent power is dissipated in either the ON or OFF state of the switch. Maximum power supply current is  $10\mu A$  from any supply, and typical quiescent currents are in the 10nA range. OFF leakages are typically less than 200pA at  $25^{\circ} C$ .

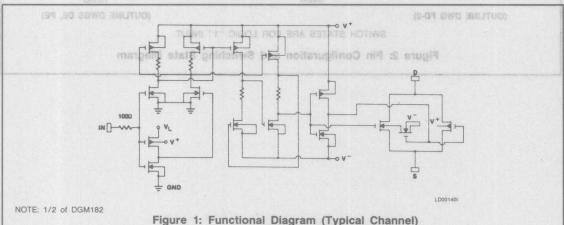
#### **FEATURES**

- Pin and Function Replacement for DG181 Family
- Meets or Exceeds All DG181 Family Specifications With Monolithic Reliability
- Low Power Consumption
- 1nA Leakage From Signal Channel in Both ON and OFF States
- TTL, DTL, RTL Direct Drive Capability
- ton, toff < 150ns, Break-Before-Make Action
- Crosstalk and Open Load Switch Isolation > 50dB at 10MHz (75Ω Load)

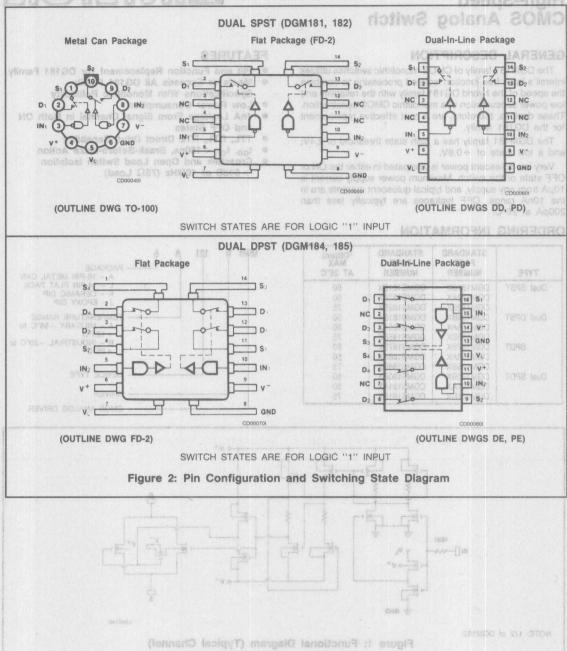
#### ORDERING INFORMATION

TYPE	STANDARD PART NUMBER	STANDARD PART NUMBER	rDS(on) MAX AT 25°C
Dual SPST	DGM181BX	DGMS181BX	50
	DGM182AX	DGMS182AX	50
	DGM182BX	DGMS182BX	75
Dual DPST	DGM184BX	DGMS181BX	50
	DGM185AX	DGMS185AX	50
	DGM185BX	DGMS185BX	75
SPDT	DGM187BX	DGMS187BX	50
	DGM188AX	DGMS188AX	50
	DGM188BX	DGMS188BX	75
Dual SPDT	DGM190BX	DGMS190BX	50
	DGM191AX	DGMS191AX	50
	DGM191BX	DGMS191BX	75



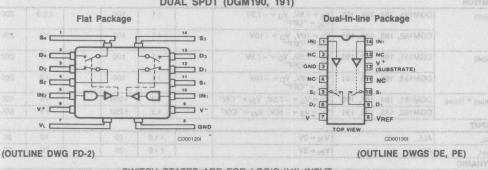


3-39



SWITCH STATES ARE FOR LOGIC "1" INPUT

**DUAL SPDT (DGM190, 191)** 



SWITCH STATES ARE FOR LOGIC "1" INPUT

Figure 2: Pin Configuration and Switching State Diagram (Cont.)

3-41

# DGM181-191



#### **ABSOLUTE MAXIMUM RATINGS**

V <sup>+</sup> -V <sup>-</sup> specifical solutions	36V	GND-V <sub>IN</sub>
VVD		Current (Any Terminal)
V <sub>D</sub> -V <sup>-</sup>		Storage Temperature65°C to +150°C
V <sub>D</sub> -V <sub>S</sub>	±22V	Operating Temperature55°C to +125°C
V <sub>I</sub> -V <sup>-</sup>	36V	Lead Temperature (Soldering, 10sec)300°C
VV <sub>IN</sub>	30V	Power Dissipation*
VL-VGND		825(DIP)mV
V <sub>IN</sub> -V <sub>GND</sub>	20V	*Device mounted with all leads welded or soldered to PC board. Derate
GND-V-		6mW/°C (TW): 10mW/°C (FLAT): 11mW/°C (DIP) above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **ELECTRICAL CHARACTERISTICS** (V<sup>+</sup> = +15V, V<sup>-</sup> = -15V, V<sub>L</sub> = 5V, unless noted)

(04 ,0)		TEST CONDITIONS	A SERIES			B SERIES			
PARAMETER	DEVICE NO.	(Note 1)	-55°C	+ 25°C	+ 125°C	-20°C	+ 25°C	+ 85°C	UNIT
SWITCH		rer ,oermag) T	AL SPD	U0					
IS(off)	DGM181, 184, 187, 190	V <sub>S</sub> = 7.5V, V <sub>D</sub> = -7.5V V <sub>IN</sub> = "OFF"		,±1	100	Flat 9	±2.0	200	nA
	DGM182, 185, 188, 191	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V V <sub>IN</sub> = "OFF"	on mile	±1	100		±2	200	nA
I <sub>D(off)</sub>	DGM181, 184, 187, 190	V <sub>S</sub> = 7.5V, V <sub>D</sub> = -7.5V V <sub>IN</sub> = "OFF"	10 C	±10-	100		±2	200	nA
The second secon	DGM182, 185, 188, 191	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V V <sub>IN</sub> = "OFF"	(8 ( )	±1	100		±2	200	nA
ID(on) + IS(on)	DGM181, 184, 187, 190	$V_D = V_S = -7.5V$ , $V_{IN} = "ON"$	-1996	±2	±200		±5	500	nA
	DGM182, 185, 188, 191	$V_D = V_S = -10V$ , $V_{IN} = "ON"$	-v 6/11	±2	±200	(.1	±5	500	nA
INPUT	Appropriation of Approp		use City				100		
I <sub>INL</sub>	ALL IOSZOGIA	V <sub>IN</sub> = 0V	103/0002	±1.0	20		10	20	μΑ
INH (39 .30	ALLWG BULTUGE	V <sub>IN</sub> = 5V		±1.0	20	00-078 8	10	20	μΑ
DYNAMIC		<b>经验证证的</b> 的对象。可以是是							
ton	DGM181, 184, 187, 190 DGM182, 185, 188, 191	See switching time test circuit		450	W.S.		500		ns
toff	ALL (MOD) MSIGE	nd Switching State D	a nous	250	D TEN	ix aim	275		
Cs(off)	DGM181, 182, 184, 185,	$V_S = -5V$ , $I_D = 0$ , $f = 1MHz$		-	5pF	typical	dependency land		
C <sub>D(off)</sub>	187, 188, 190, 191	$V_D = +5V$ , $I_S = 0$ , $f = 1MHz$			6pF	typical		pF	
CD(on) + CS(on)		$V_D = V_S = 0$ , $f = 1MHz$	11pF typical						
OFF Isolation		$R_L = 75\Omega$ , $C_L = 3pF$	Typically > 50dB at 10MHz						
SUPPLY									
1+	ALL		10	10	100		100		
IT.	ALL	V <sub>IN</sub> = 5V	10	10	100		100		
IL.	ALL		10	10	100		100	A GARAGE	
IGND	ALL		10	10	100		100		μΑ
1+	ALL		10	10	100		100		
1-	ALL	V <sub>IN</sub> = 0V	10	10	100		100	Market S	
ار	ALL		10	10	100		100		
IGND	ALL		10	10	100		100		

Note 1: See Switching State Diagrams for VIN and VIN "OFF" Test Conditions.

# 3

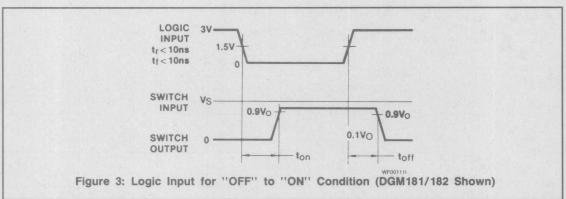
#### ELECTRICAL CHARACTERISTICS MAXIMUM RESISTANCES (DS(ON)

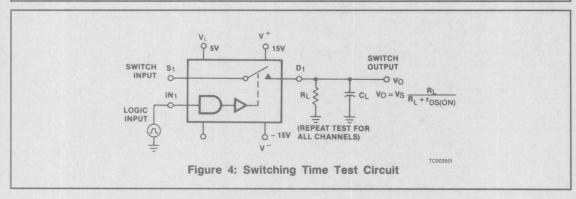
DEVICE NUMBER	CONDITIONS (Note 1)	MILITAF	RY TEMPE	RATURE	і зионт <b>Т</b> Е	TINU		
	$V^{+} = 15V, V^{-} = -15V, V_{L} = 5V$	-55°C	+25°C	+ 125°C	-20°C	+ 25°C	+85°C	
DGM181 DGM182 DGM184	V <sub>D</sub> = -7.5V V <sub>D</sub> = -10V V <sub>D</sub> = -7.5V	50 30	50 30	75 60	50 75 50	50 75 50	75 100 75	Ω
DGM185 DGM187	$V_D = -10V$ $V_D = -10mA$ $V_{IN} = -10mA$	50	50	75 60	75 50	75 50	100	Ω
DGM188 DGM190	V <sub>D</sub> = -10V V <sub>D</sub> = -7.5V	50	50 30	75 60	75 50	75 50	75 100 75	Ω
DGM191	$V_D = -10V$	50	50	75	75	75	100	Ω

APPLICATION COMMENT: The charge injection in these switches is of opposite polarity to that of the standard DG180 family, but considerably smaller.

#### SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S = constant$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





#### DCM101/102

0°88 + 0 DGM18	31/182
V <sub>IN</sub> "ON" = 0.8V V <sub>IN</sub> "OFF" = 2.4V	All Channels All Channels

 DGM184/185

 V<sub>IN</sub> "ON" = 2.4V
 All Channels

 V<sub>IN</sub> "OFF" = 0.8V
 All Channels

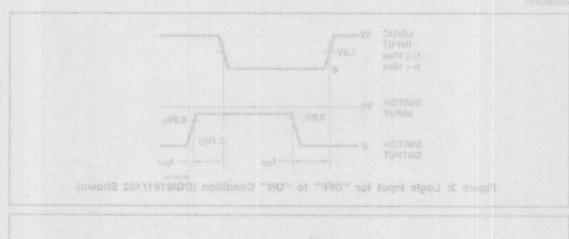
#### SPDT DGM187/188

#### TEST CONDITIONS

DGM18	7/188
V <sub>IN</sub> "ON" = 2.4V	Channel 1
V <sub>IN</sub> ''ON'' = 0.8V	Channel 2
V <sub>IN</sub> "OFF" = 2.4V	Channel 2
V <sub>IN</sub> "OFF" = 0.8V	Channel 1

#### DUAL SPDT DGM190/191 TEST CONDITIONS

DGM190	/191			18	riyli
V <sub>IN</sub> "ON" = 2.4V	Channels	1	&	2	M
VIN "ON" = 0.8V	Channels	3	&	4	
V <sub>IN</sub> "OFF" = 2.4V	Channels	3	&	4	
V <sub>IN</sub> ''OFF'' = 0.8V	Channels	1	&	2	107



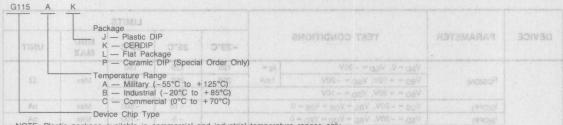
# GENERAL DESCRIPTION W - BV) 6180 of 1008

These switches may be connected directly to the INTER-SIL switch-driver D123 series without the need of any interfacing components, and are internally protected by a Zener diode integrated on the silicon chip. A MOSFET used as a current source provides an active pull-up for faster switching capability. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

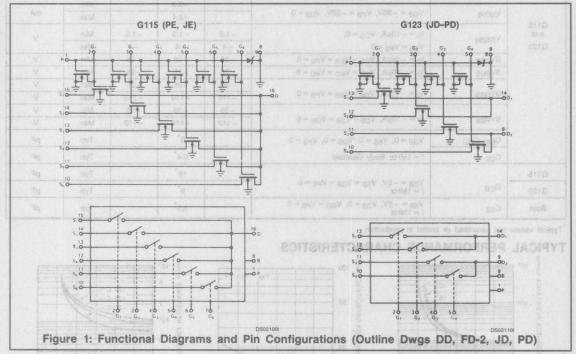
# FEATURES (20) INTERIOR CONTROL OF THE PARTY OF THE PARTY

- Integrated MOSFET Constant-Current Sources for Open Collector Driver Pull-up
- Integrated Zener Diode Protection for Both
   Positive and Negative Spike Protection
- P-Channel Enhancement-Type Switches

#### ORDERING INFORMATION



NOTE: Plastic package available in commercial and industrial temperature ranges only.



NOTE: G115 Built-in 16-Pin DIP Only.

# G115/G123

# **WINTERSIL**

# ABSOLUTE MAXIMUM RATINGS (25°C)

Body to Gate (V <sub>B</sub> – V <sub>G</sub> )+35V
Body to Pull-up (V <sub>B</sub> – V <sub>P</sub> )+35V
Power Dissipation
(derate 10mW/°C above 70°C)
Lead Temperature (Soldering, 10sec)300°C
Zener close integrated on the succending. A McCarter tised

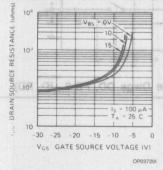
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

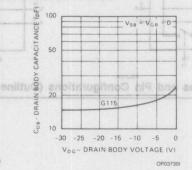
# **ELECTRICAL CHARACTERISTICS** (per channel unless noted)

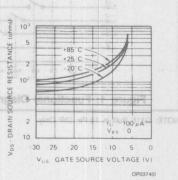
DEVICE	PARAMETER	TEST CONDITIONS		-20°C	25°C	85°C	MIN/ MAX	UNIT	
		$V_{BD} = 0, V_{GD} = -30V$	Is=	125	125	150			
	RDS(ON)	$V_{BD} = +10V, V_{GD} = -20V$	1mA	250	250	300	Max	Ω	
	Though the same of	$V_{BD} = +20V, V_{GD} = -10V$		500	500	600	8		
	I <sub>D</sub> (OFF)	$V_{DS} = -20V$ , $V_{BS} = V_{GS} = V_{PS} = 0$			-10	-500	Max	nA	
	IS(OFF)	$V_{SD} = -20V$ , $V_{BD} = V_{GD} = V_{PD} = 0$			-5	-100	Max	nA	
	IGBS	$V_{GB} = -20V$ , $V_{DB} = V_{SB} = V_{PB} = 0$	SE INTELLEGIS	TODAY GAZAGE TO	-5	-100	Max	nA	
	A SEASON DISCONNESS CONTRACTOR				-0.8	Marketing Income	Min		
	IG(ON)	$V_{GB} = -30V$ , $V_{PB} = -30V$ , $V_{DB} = 0$	$-30V$ , $V_{DB} = 0$		-2.4		Max	mA	
G115 and	Vocate	$V_{GS(th)}$ $I_S = -10\mu A, V_{DG} = 0,$		-1.5	-1.5	-1.5	Min	V	
G123	$V_{BS} = V_{PS} = 0$			-4	-4	-4	Max		
	BVDSS	$I_D = -10\mu A$ , $V_{GB} = V_{BS} = V_{PS} = 0$	-	-25	-25	-25	Min	V	
	BVSDS	$I_S = -10\mu A$ , $V_{GD} = V_{BD} = V_{PD} = 0$		-25	-25	-25	Min	٧	
	the did list and	1111111		-35	-35	-35	Min	٧	
	BV <sub>GBS</sub> $I_G = -10\mu A$ , $V_{DB} = V_{SB} = V_{PB} = 0$			-110	-110	-110	Max	V	
		THE RESERVE OF THE PARTY OF THE		-35	-35	-35	Min	V	
	BVPBS	$I_{P} = -10\mu A$ , $V_{DB} = V_{SB} = V_{GB} = 0$		-110	-110	-110	Max	٧	
	CGS, CGD	$V_{GB} = 0$ , $V_{SB} = 0$ , $V_{DB} = 0$ , $V_{PB} = 0$			3*		Тур	pF	
	C <sub>DS</sub>	f = 1MHz, Body Guarded		and the second	0.4*		Тур	pF	
G115				二·-	18*		Тур	pF	
G123	G <sub>DB</sub>	$V_{DB} = -5V$ , $V_{SB} = V_{GB} = V_{PB} = 0$ f = 1MHz		4	9*		Тур	pF	
Both	C <sub>SB</sub>	$V_{SB} = -5V$ , $V_{DB} = 0$ , $V_{GB} = V_{PB} = 0$ f = 1MHz		-	3.5*		Тур	pF	

<sup>\*</sup>Typical values not garanteed or tested in production

#### TYPICAL PERFORMANCE CHARACTERISTICS







3

G-Terminal — This is the control terminal of the switch. The voltage at this terminal determines the conduction state of  $Q_2$ . To insure conduction of  $Q_2$  when voltages between  $\pm 10 \text{V}$  are switched, the gate voltage (V<sub>G</sub>) should be at least 10 V more negative than the most negative

voltage to be switched (-10V). Therefore,  $V_G$  should go to -20V. To insure turn-off  $V_G$  should not be less than the most positive voltage to be switched, +10V. For convenience the same potential as the body could be used.

B-Terminal — This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to ensure that the drain-to-body or the source-to-body junctions do not become forward biased.

P-Terminal — The potential, with respect to the body, at this terminal determines the gate-to-source voltage of  $Q_1$  which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents  $Q_1$  and  $Q_3$  from conducting, but still allows the body-to-drain junction of  $Q_1$  to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BVDSS (-30 to -90V) for protecting the gate of  $Q_2$ .

D-Terminal — The common point of the MOSFET switches (summing point).

S-Terminal — This is the normally-open terminal of the MOSFET switch and is normally used as the input.

# APPLICATIONS Dual Current-to-Voltage Converter With Range Programming Channel Multiplexer AP031001 AP031001

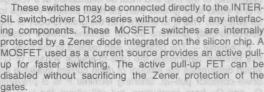
# G116, G118, G119



# GENERAL DESCRIPTION

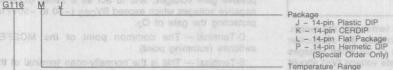
SIL switch-driver D123 series without need of any interfacing components. These MOSFET switches are internally protected by a Zener diode integrated on the silicon chip. A MOSFET used as a current source provides an active pullup for faster switching. The active pull-up FET can be disabled without sacrificing the Zener protection of the

# ORDERING INFORMATION





- P-Channel Enhancement-Type MOSFET Switches
- Zener Protection on All Gates
- With and Without Constant Current Source Pull-Up

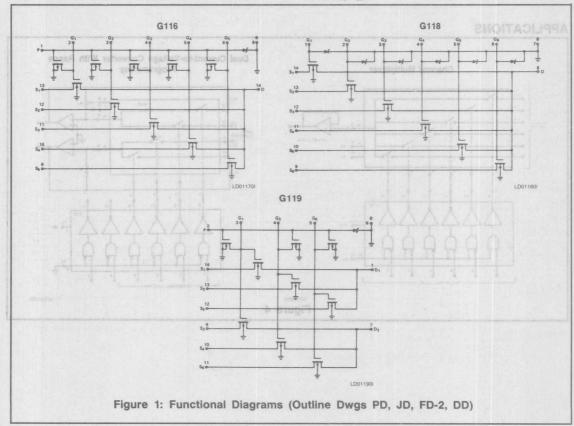


Temperature Range

A = Military (-55°C to +125°C)

B = Industrial (-20°C to +85°C)

Device Chip Type



# G116, G118, G119

# **WINTERSIL**

#### **ABSOLUTE MAXIMUM RATINGS (25°C)**

Source Current (Is)	nA
Drain Current (ID)100r	nA
Control Gate Current Ig5r	
Pull-Up Gate Current Ip	μΑ
Body Voltage (VB) to Any Terminal2 to +3	OV

Power Dissipation (Note)			.750mW
Storage Temperature			
Operating Temperature	-50°C	to	+125°C
Lead Temperature (Soldering, 10sec)			300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS** (Per Channel Unless Noted)

References to pull-up gate P do not apply to G118.

			LIMITS						
PARAMETER	TEST CONDITIONS		G116M Series		G116C Series				
			25°C	125°C	25°C	125°C	MIN/MAX	UNIT	
[DO/ON)	$V_{BD} = 0$ , $V_{GD} = -30V$ , $V_{PB} = 0$	Is =	100	125	125	1 10° 200			
rDS(ON) (Note 1)	$V_{BD} = +10V$ , $V_{GD} = -20V$ , $V_{PB} = 0$	-1mA	200	250	250	El son.	Max	Ω	
(11010-1)	$V_{BD} = +20V$ , $V_{GD} = -10V$ , $V_{PB} = 0$		450	600	600				
IS(OFF)	$V_{SD} = -20V$ , $V_{BD} = V_{GD} = V_{PD} = 0$	By Ships	-0.5	-500	-1		Max	nA	
	V <sub>DS</sub> = -20V	G116	-2.5	-2500	-5			14.7	
	$V_{BD} = V_{GD} = V_{PD} = 0$	G118	-3.0	-3000	-6		Max	nA	
ID(OFF)		G119	-1.5	-1500	-3				
	$V_{G1B}$ to $V_{G5B} = 0$ , $V_{G6B} = -30V$ , $V_{DB} = -20V$ , $V_{SB} = V_{PB} = 0$	G117	-0.5	-500	-1	Sett	Max	nA	
BVDSS	$I_D = -10 \mu A$ , $V_{GS} = V_{BS} = V_{PS} = 0$	-30		-30		Min			
BVSDS	$I_S = -10 \mu A$ , $V_{GD} = V_{BD} = V_{PD} = 0$	REI BUTCH	-30		-30	THE PERSON	Min		
e to be switched. This is	$I_{G} = -10\mu A$ , $V_{PB} = V_{SB} = V_{DB} = 0$		-30		-30		Min		
BVGBS Vood-of-morb			-110	8	-110	- 15	Max	٧	
Tot amooso ton op anot	luni Apde di edinos		-30		-30	1	Min		
BVPBS	$I_P = -10 \mu A$ , $V_{GB} = V_{SB} = V_{DB} = 0$		-110		-110	131	Max		
respect to the body, a	-Terminal The potential, with	9 1	-1.5	1	-1.5		Min		
VGD(th) of else off sens	$I_S = -10\mu A$ , $V_{DS} = -10V$ , $V_{SB} = 0$		-4	STATISTICS	-4	1	Max		
IGS(ON)	form (O to agation		-0.5	institute.	-0.3		Min		
(Note 2)	$V_{GB} = -30V$ , $V_{PB} = -30V$ , $V_{SB} = V_{DB}$	= 0	-2	lenns	-2.5	2: 91	Max	mA	
IGSS wells lide fuel conito	V <sub>GB</sub> = -20V, V <sub>DS</sub> = V <sub>BS</sub> = V <sub>PS</sub> = 0		-0.5	-500	-1		Max	nA	
C <sub>GD</sub> or C <sub>GS</sub>	V <sub>PB</sub> = 0, V <sub>BS</sub> = 0, or V <sub>BD</sub> = 0	96	3.00	arti to fee	3	thao arti	Тур	pF	
Csp (Note 3)	Body Guarded, f = 1MHz		0.4	determin	0.4	atrit ts	Тур	pF	
C <sub>SB</sub> (Note 3)	$V_{PB} = V_{GB} = V_{DB} = 0$ , $V_{SB} = -5V$ , $f =$	1MHz	-3.5	un enuali	-3.5	o stara	Тур	pF	
E-) gagV8 begaxe flaid	wedgelov evuspen	G116	18	TISBN239	18	FOY THE	W SD		
	Vac - 6V f - 1MU2	G118	18	(E) 4) OE	18	y and Ju	Тур	pF	
C <sub>DG</sub> (Note 3)		G119	10	A Comme	10	antino	18891		
	V <sub>G6B</sub> = -30V, V <sub>PB</sub> = V <sub>SB</sub> = 0, V <sub>G1B</sub> to V <sub>G5B</sub> = 0, V <sub>DB</sub> = -5V, f=1MHz	G117	20	102- of c	20	ore, V <sub>G</sub>	Тур	pF	

NOTES: 1. For the G117 this is the resistance from each of the source terminals (5 terminals) and the one drain terminal to the internal junction of the output MOSFETs.

2: Not applicable to G118.

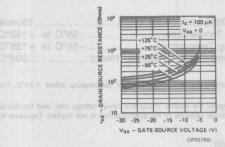
3: Typical values not guaranteed or tested in production.

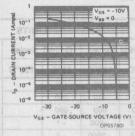
3

# G116, G118, G119

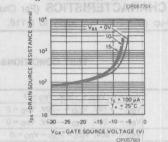
# **WINTERSIL**

# TYPICAL PERFORMANCE CHARACTERISTICS



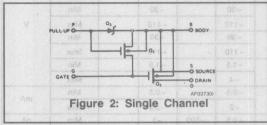


# 



# **APPLICATION TIPS**

Description of Analog Switch



G-Terminal — This is the control terminal of the switch; the voltage at this terminal determines the conduction state of  $Q_2$ . To insure conduction of  $Q_2$  when voltages between  $\pm 10V$  are switched, the gate voltage (V<sub>G</sub>) should be at least 10V more negative than the most negative voltage to be switched (-10V). Therefore, V<sub>G</sub> should go to -20V. To insure turn-off V<sub>G</sub> should not be less than the most positive voltage to be switched,  $\pm 10V$ . For convenience the same potential as the body could be used.

B-Terminal — This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to insure that the drain-to-body or the source-to-body junctions do not become forward biased.

P-Terminal — The potential, with respect to the body, at this terminal determines the gate-to-source voltage of Q<sub>1</sub> which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents Q<sub>1</sub> and Q<sub>3</sub> from conducting, but still allows the body-to-drain junction of Q<sub>1</sub> to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BVDSS (-30 to -110V) for protecting the gate of Q<sub>2</sub>.

D-Terminal — The common point of the MOSFET switches (summing point).

S-Terminal — This is the normally-open terminal of the MOSFET switch and is normally used as the input

# **APPLICATIONS**

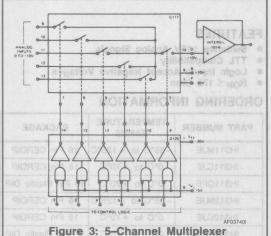


Figure 3: 5-Channel Multiplexer With Series Switch

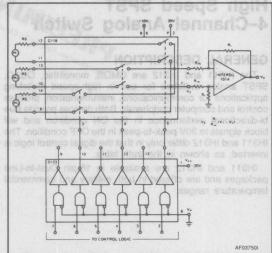


Figure 4: 3-Channel Differential Multiplexer

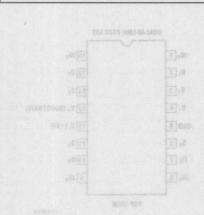
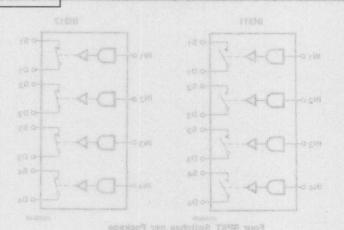


Figure 2: Pin Configuration (Outline dwgs OE, PE)



\$18HI	
770	

Logic "9" ≤ 0.8V Logic "1" ≥ 2.4V

Figure 1: Functional Diagram

#### GENERAL DESCRIPTION

The IH311 and IH312 are CMOS, monolithic, QUAD, SPST analog switches for use in high-speed switching applications for communications, instrumentation, process control and computer peripherals. Both devices provide true bi-directional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The IH311 and IH312 differ only in that the digital control logic is inverted, as shown in the truth table.

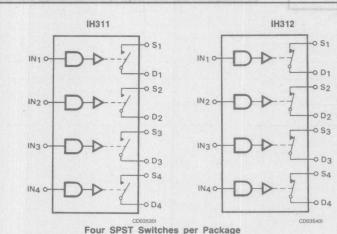
IH311 and IH312 are available in 16-pin Dual-In-Line packages and are offered in both military and commercial temperature ranges.

#### **FEATURES**

- Switches ±15V Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- RoN ≤ 175 Ohm

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE					
IH311MJE	-55°C to +125°C	16 Pin CERDIP					
IH311CJE	0°C to +70°C	16 Pin CERDIP					
IH311CPE	0°C to +70°C	16 Pin Plastic DIP					
IH312MJE	-55°C to +125°C	16 Pin CERDIP					
IH312CJE	0°C to +70°C	16 Pin CERDIP					
IH312CPE	0°C to +70°C	16 Pin Plastic DIP					



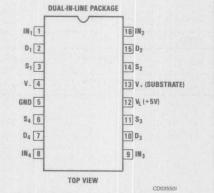


Figure 2: Pin Configuration (Outline dwgs DE, PE)

Switches Shown for Logic "1" Input

Truth Table

LOGIC	IH311	IH312		
0	ON	OFF		
1	OFF	ON		

Logic ''0'' ≤ 0.8V Logic ''1'' ≥ 2.4V

Figure 1: Functional Diagram

# IH311/IH312

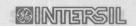
# **ABSOLUTE MAXIMUM RATINGS**

IH311/IH312			5
ABSOLUTE MAXIMUM RATINGS	3		
V <sup>+</sup> to V <sup>-</sup>	36V	Peak Current, S or D	
VIN to Ground	V+, V+	(Pulsed at 1msec, 10% duty cycle max) 70m	Α
V <sub>L</sub> to Ground		Storage Temperature65°C to +125°	C
Vs or Vp to V+	0, -36V	Operating Temperature55°C to +125°	
Vs or VD to V		Power Dissipation (Package)*  16 Pin Plastic DIP**	
V <sup>+</sup> to Ground		16 Pin Plastic DIP**470m\	N
V <sup>-</sup> to Ground		*Device mounted with all leads soldered or welded	
Current, Any Terminal Except S or D	30mA	to PC board.	
Continuous Current, S or D	20mA	**Derate 6.5mW/°C above 25°C	

# ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE

SYMBOL	PARAMETER	TEST CONDITIONS  V <sub>1</sub> = +15V, V <sub>2</sub> = -15V  V <sub>L</sub> = 5V, GND			LIMITS	Negalius	UNIT								
STMBOL	PARAMETER			-55°C	+ 25°C	+ 125°C	UNI								
SWITCH						Jeorla									
VANALOG	Analog Signal Range	$V^- = -15V, V_L$	= +5V	60°L stai novi	±15	of all mounts	٧								
RDS(ON)	Drain-Source On Resistance	$V_D = \pm 10V$ , $V_{IN} = 1$	$V_D = \pm 10V$ , $V_{IN} = 2.4V$ — IH312 $I_S = 1$ mA, $V_{IN} = 0.8V$ — IH311		125	150	Ω								
	Source OFF Leakage Current	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14V		±1	100									
Source OFF Leakage Current	IH311	V <sub>S</sub> = -14V, V <sub>D</sub> = 14V		±1	100										
I=	Drain OFF Leakage Current	V <sub>IN</sub> = 0.8V							V <sub>IN</sub> = 0.8V IH312		V <sub>D</sub> = 14V, V <sub>S</sub> = -14V		±1	100	
ID(off)	Drain OFF Leakage Current	111312	V <sub>D</sub> = -14V, V <sub>S</sub> = 14V		±1	100									
la caso	Drain ON Leakage Current <sup>3</sup>		V, V <sub>IN</sub> = 0.8V, IH311		±2	200	- 1								
ID(ON)	Drain ON Leakage Current	$V_{IN} = 2.4V, IH3$	112		±2	200	nA								
INPUT															
lana.	Input Current With Input	V <sub>IN</sub> = 2.4V		10	±1.	10									
INH	Voltage High	V <sub>IN</sub> = 15V		10	±1	10	μА								
INL	Input Current With Input Voltage Low	V <sub>IN</sub> = 0V		10	10	10	μη								

# IH311/IH312



ABSOLUTE MAXIMUM RATINGS

#### DYNAMIC

DITTAMIO	10.	id Inamic black Mile				
ton (X	Turn-ON Time	ts beautiful ty *v		200		in to G
toff1	Turn-OFF Time	See Switching Time Test Circuit $V_S = 10V$ , $R_L = 1k\Omega$ , $C_L = 35pF$	ACART TELEPE	80	briu	ns ns
toff2	rature55°	Committee of Value Temp	interpression		* V et	g or Vp
C <sub>S(off)</sub>	Source OFF Capacitance	V <sub>S</sub> = 0V, V <sub>IN</sub> = 5V, f = 1MHz	construction.	5	V 0	g or Vo
C <sub>D(off)</sub>	Drain OFF Capacitance	$V_D = 0V$ , $V_{IN} = 5V$ , $f = 1MHz^2$		5	baud	D PF
CD+S(on)	Channel ON Capacitance	$V_D = V_S = 0V$ , $V_{IN} = 0V$ , $f = 1MHz$		16		ne of
OIRR	OFF Isolation <sup>4</sup>	$V_{IN} = 5V$ , $R_{I} = 1k\Omega$ ,	O 10 E	70	my Termin	urrent, f
CCRR	Crosstalk (Channel to Channel)	$VIN = 5V$ , $H_L = 1K35$ , $C_L = 15pF$ , $V_S = 1VRMS$ , $f = 100kHz^2$		90	s Current,	dB
SUPPLY	JAE RANGE	:S MILITARY TEMPERATI	HERISTIC	HARACT	O JAOH	LECTI
1+	Positive Supply Current		10	1	10	- Commence
1-	Negative Supply Current	VIN = 0 and 2.4V TIGHOO TRAT	10	1	10	μА
Real -	Logic Supply Current	V <sub>1</sub> = + 15V, V <sub>2</sub> = -15V	10	PARAMETE	10	syws.

NOTES:	1. The algebraic	convention	whereby	the r	most	negative	value	is a	minimum,	and	the	most	positive	is a	maximum,	is	used	in t	his	data
	sheet.																			

For design reference only, not 100% tested.
 ID(on) is leakage from driver into "ON" switch.

<sup>4.</sup> OFF Isolation =  $20\log \frac{V_S}{V_D}$ ,  $V_S$  = input to OFF switch,  $V_D$  = output.

# IH311/IH312

# **BINTERSIL**

# **ABSOLUTE MAXIMUM RATINGS**

V <sup>+</sup> to V <sup>-</sup>	36V
V <sub>IN</sub> to Ground	V+
V <sub>L</sub> to Ground0.3V,	
Vs or Vp to V+, 0, -	36V
Vs or VD to V,0,	40V
V <sup>+</sup> to Ground	25V
V <sup>-</sup> to Ground	25V
Current, Any Terminal Except S or D30	)mA
Continuous Current, S or D	)mA

Peak Current, S or D	logic input waveform as
(Pulsed at 1msec, 10% duty	cycle max) 70mA
Storage Temperature	65°C to +125°C
Operating Temperature	0°C to +70°C
Power Dissipation (Package)*	
16 Pin Plastic DIP**	470mW

<sup>\*</sup>Device mounted with all leads soldered or welded to PC board.

# ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE

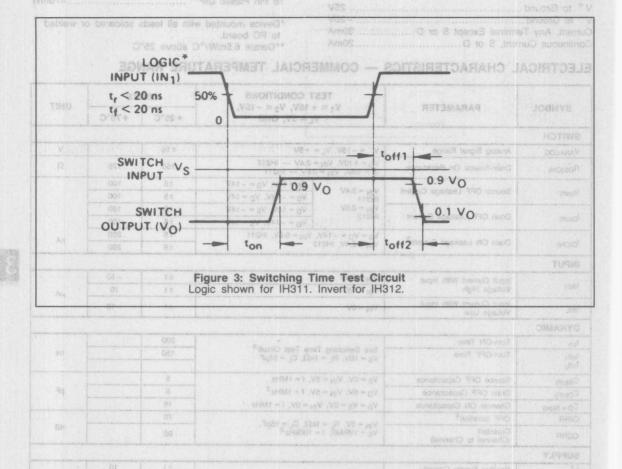
		1		1	(4 (2)) 1	DAM				
			T CONDITIONS	- 9609	ELIM	ITS ,				
SYMBOL PARAMETER		$V_1 = +15V, V_2 = -15V, V_L = 5V, GND$			+ 25°C	+70°C	UNIT			
SWITCH										
VANALOG	Analog Signal Range	$V^- = -15V, V_L =$	+ 5V		±15		V			
R <sub>DS</sub> (ON)	Drain-Source On Resistance	$V_D = \pm 10V, V_{IN} = 0$ $I_S = 1 \text{mA}, V_{IN} = 0$	0.8V — IH211		150	175	Ω			
loc-m	Source OFF Leakage Current	Van = 24V 0V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14\	1	±5	100				
IS(off)	Source Of Leanage Current	IH311	$V_S = -14V, V_D = 14V$	1	±5	100				
lav in	Drain OFF Leakage Current	V <sub>IN</sub> = 0.8V IH312	$V_D = 14V, V_S = -14V$	1	H±5T IW	100				
ID(off)	Drain Of F Leanage Current	IIIOTZ	$V_D = -14V, V_S = 14V$	/us/ricingston	1222 1 2	100				
ID(ON)	Drain ON Leakage Current <sup>3</sup>	$V_S = V_D = -14V$ ,	V <sub>IN</sub> = 0.8V, IH211		±5	200	nA			
ID(ON)	(ON) Drain ON Leakage Current		V <sub>IN</sub> = 2.4V, IH212		±5	200	IIA			
INPUT										
Laura Carlo	Input Current With Input	VIN = 2.4V Smit on Holling :E		Un = 2.4V amil oninofiwe is anu	oung!	±1	-10			
INH	Voltage High	V <sub>IN</sub> = 15V	hown for iH311.	la pipo	±1	10	μΑ			
I <sub>INL</sub>	Input Current With Input Voltage Low	V <sub>IN</sub> = 0V			- ±1	-10	1			
DYNAMIC										
ton	Turn-ON Time		, ,		300					
toff1 toff2	Turn-OFF Time	See Switching Tile $V_S = 10V$ , $R_L = 1$			150		ns			
Cs(off)	Source OFF Capacitance	V <sub>S</sub> = 0V, V <sub>IN</sub> = 5V	/, f = 1MHz		5					
C <sub>D(off)</sub>	Drain OFF Capacitance	$V_D = 0V, V_{IN} = 5$	$V, f = 1MHz^2$		5		pF			
CD + S(on)	Channel ON Capacitance	V <sub>D</sub> = V <sub>S</sub> = 0V, V <sub>IN</sub> = 0V, f = 1MHz								
OIRR	OFF Isolation <sup>4</sup>	V 5V D 41	0.0 45.5	URIUS S	70		ME THE			
CCRR	Crosstalk (Channel to Channel)	$V_{IN} = 5V$ , $R_L = 1k\Omega$ , $C_L = 15pF$ , $V_S = 1VRMS$ , $f = 100kHz^2$			$V_{IN} = 5V$ , $H_L = 1k32$ , $C_L = 15pF$ , $V_S = 1VRMS$ , $f = 100kHz^2$			90		dB
SUPPLY							Ser la			
1+	Positive Supply Current				±1	10				
1-	Negative Supply Current	V <sub>IN</sub> = 0 and 2.4V			±1	-10	μΑ			
IL.	Logic Supply Current				±1	10				

NOTES: 1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data

- 2. For design reference only, not 100% tested.
  3. ID(on) is leakage from driver into "ON" switch.
- 4. OFF Isolation =  $20\log \frac{V_S}{V_D}$ ,  $V_S$  = input to OFF switch,  $V_D$  = output,
- 5. Switching times only sampled.

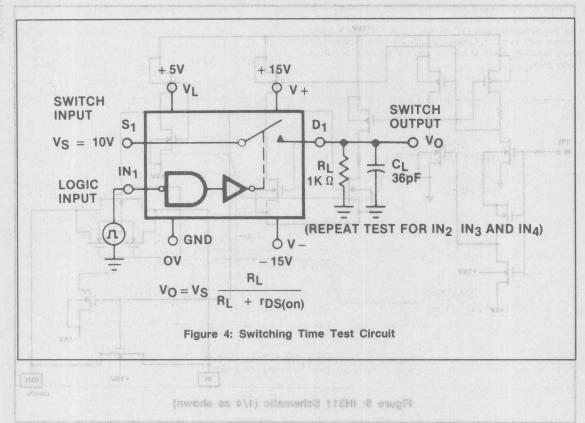
<sup>\*\*</sup>Derate 6.5mW/°C above 25°C

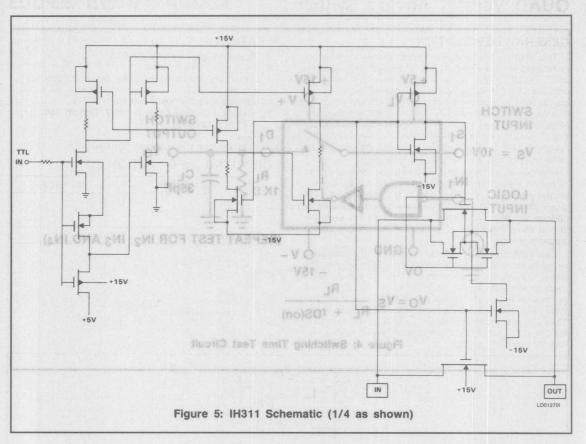
logic input waveform as shown. Note the  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



NOTES: 1. The absolute convention whereby the most negative value is a minimum, and the most positive is a maximum is used in this data.

4. OFF inclusion = 20leg  $\frac{V_S}{V_D}$ ,  $V_S$  = input to OFF switch,  $V_\Omega$  = output





#### GENERAL DESCRIPTION

The IH401 is made up of 4 monolithically constructed combinations of a varactor type diode and an N-channel JFET. The JFET itself is very similar to the popular 2N4391, and the driver diode is specially designed, such that its capacitance is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel FET and simulates a back-to-back diode structure. This structure is needed to prevent forward biasing the source-to-gate or drain-to-gate junctions of the JFET when used in switching applications.

Previous applications of JFETs required the addition of diodes, in series with the gate, and then perhaps a gate-to-source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401 does this same job in one component (with a great deal better performance characteristics).

Like a standard JFET, to practically perform a solid state switch function a translator should be added to drive the diode. This translator takes the TTL levels and converts them to voltages required to drive the diode/FET system (typically a 0V to -15V translation and a 3V to +15V shift). With  $\pm 15V$  power supplies, the IH401 will typically switch  $18V_{p-p}$  at any frequency from DC to 20MHz, with less than  $30\Omega$  RDS(on). The IH401A will typically switch  $22V_{p-p}$  with less than  $50\Omega$  RDS(on).

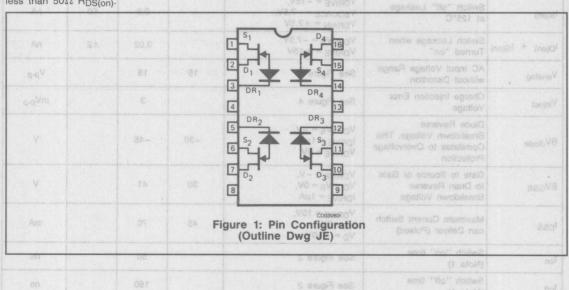
# **FEATURES**

- R<sub>DS(on)</sub> = 25Ω Typical (IH401)
- ID(off) of 10pA Typical
- Switching Times of 25ns for t<sub>on</sub> and 75ns for t<sub>off</sub> (R<sub>L</sub> = 1kΩ)
- Built-In Overvoltage Protection (±25V)
- Charge Injection Error of 3mV Typical Into 0.01μF Capacitor
- Ciss < 1pF Typical
- Can Be Used for Hybrid Construction

#### ORDERING INFORMATION

PART NUMBER	doriwa PACKAGE
IH401	CERDIP
IH401A	CERDIP
IH401/D	DICE

MOTE 1: Oriving waveform must be > 100ns use and fall time





# IH401/IH401A

# ABSOLUTE MAXIMUM RATINGS

QUAD Varafet Analog Switch

V <sub>S</sub> to V <sub>D</sub>	Storage Temperature65°C to +150°C
Vg to Vs, Vp	Lead Temperature (Soldering, 10sec)300°C
Operating Temperature	The IH401 is made up of 4 monolithically constructed

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to operation of the device at these or any other conditions above these managements about the device reliability.

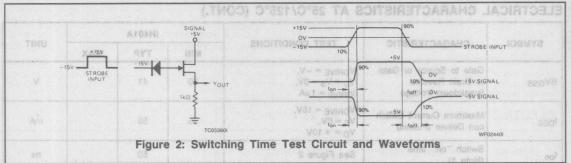
absolute maximum rating conditions for extended periods may affect device reliability.

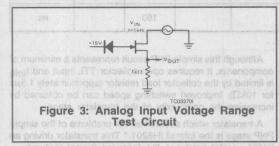
# ELECTRICAL CHARACTERISTICS AT 25°C/125°C to stap ent riliw sense ni vilschiosie al abolib revib ent

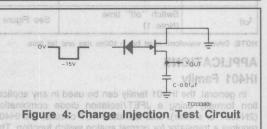
SYMBOL	CHARACTERISTIC	TEST CONDITIONS	Librayiot mave to of beloven status			ure. This situal
			MIN	TYP	MAX	offwe mines
R <sub>DS(on)</sub>	Switch "on" Resistance	15.0 11.0011007	ien perhaps or in paralle	br 20	eut 304 se	ioder Qri Berr Quebe referr
Vp	Pinch-Off Voltage	I <sub>D</sub> = 1nA, V <sub>DS</sub> = 10V	T OTEVS SITE	60 8	2697.5	lode, Vinereld
I <sub>D(off)</sub>	Switch ''off'' Current or ''off'' Leakage	VSOURCE = -7.5V,	al better pe	10	±500	primos eno ir lotan PAssan
I <sub>D</sub> (off)	Switch ''off'' Leakage at 125°C	VSOURCE = -7.5V, anavago	L fevels and	0.25	st 150 lens	witch function libde Anths transition to volta
IS(off)	Switch ''off'' Current	VDRIVE = -15V, dotiwe vilk	20MHz, with	10 .a	±500	VO a vileolovi VO a v
IS(off)	Switch ''off'' Leakage at 125°C	V <sub>DRIVE</sub> = -15V, V <sub>SOURCE</sub> = -7.5V, V <sub>DRAIN</sub> = +7.5V		0.3		An Sol
I <sub>D(on)</sub> + I <sub>S(on)</sub>	Switch Leakage when Turned "on"	$V_D = V_S = -7.5V,$ $V_{DRIVE} = +15V$		0.02	±2	nA
V <sub>analog</sub>	AC Input Voltage Range without Distortion	See Figure 3	15	18		V <sub>p-p</sub>
V <sub>inject</sub>	Charge Injection Error Voltage	See Figure 4		3		mV <sub>p-p</sub>
BV <sub>diode</sub>	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S = -V$ , $I_{DRIVE} = 1\mu A$ , $V_{DRIVE} = 0V$	-30	-45		٧
BVGSS	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V,$ $V_{D} = V_{S} = 0V,$ $I_{DRIVE} = 1\mu A$	30	41		٧
IDSS	Maximum Current Switch can Deliver (Pulsed)	V <sub>DRIVE</sub> = 15V, V <sub>S</sub> = 0V, V <sub>D</sub> = +10V	45	70		mA
ton	Switch ''on'' time (Note 1)	See Figure 2		50	***	ns
t <sub>off</sub>	Switch ''off'' time (Note 1)	See Figure 2		150		ns

NOTE 1: Driving waveform must be > 100ns rise and fall time.









#### ELECTRICAL CHARACTERISTICS AT 25°C/125°C single potents VOL efforts of ALON-II to) elempte potents

SYMBOL	CHARACTERISTIC of the	TEST CONDITIONS	IH401A			
			MIN	TYP	MAX	UNIT
RDS(on)	Switch "on" Resistance	V <sub>DRIVE</sub> = 15V, V <sub>DRAIN</sub> = -10V, I <sub>D</sub> = 10mA	10000 3	35	50	Ω
VP	Pinch-Off Voltage	I <sub>D</sub> = 1nA, V <sub>DS</sub> = 10V	2	4	5	V
D(off)	Switch ''off'' Current or ''off'' Leakage	V <sub>DRIVE</sub> = -15V, V <sub>SOURCE</sub> = -10V, V <sub>DRAIN</sub> = +10V	\$ 18 \$ 18	10	±500	PA J
ID(off)	Switch ''off' Leakage at 125°C	V <sub>DRIVE</sub> = -15V, V <sub>SOURCE</sub> = -10V, V <sub>DRAIN</sub> = +10V		0.25	50	nA
IS(off)	Switch ''off'' Current	V <sub>DRIVE</sub> = -15V, V <sub>DRAIN</sub> = -10V, V <sub>SOURCE</sub> = +10V		10	±500	pA
IS(off)	Switch ''off'' Leakage at 125°C	V <sub>DRIVE</sub> = -15V, V <sub>SOURCE</sub> = -10V, V <sub>DRAIN</sub> = +10V		0.3	50	nA
I <sub>D(on)</sub> + I <sub>S(on)</sub>	Switch Leakage when Turned "on"	$V_D = V_S = -10V$ , $V_{DRIVE} = +15V$		0.02	±2	nA
Vanalog	AC Input Voltage Range without Distortion	See Figure 3	20	22		V <sub>p-p</sub>
Vinject	Charge Injection Amplitude	See Figure 4		3		mV <sub>p-p</sub>
BV <sub>diode</sub>	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S = -V,$ $I_{DRIVE} = 1 \mu A,$ $V_{DRIVE} = 0 V$	-30	-45		V

# IH401/IH401A



# ELECTRICAL CHARACTERISTICS AT 25°C/125°C (CONT.)

SYMBOL	CHARACTERISTIC TEST CONDIT	V61	IH401A			
		TEST CONDITIONS	MIN	TYP	MAX	UNIT
- 000	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V,$ $V_{D} = V_{S} = 0V,$ $I_{DRIVE} = 1\mu A$	30	41	aros is tugui	٧
IDSS	Maximum Current Switch can Deliver (Pulsed)	V <sub>DRIVE</sub> = 15V, V <sub>S</sub> = 0V, V <sub>D</sub> = +10V	35	55		m̈́Α
t <sub>on</sub>	Switch "on" time (Note 1)	See Figure 2	2: Switch	50		ns
toff	Switch "off" time (Note 1)	See Figure 2		150		ns

NOTE: Driving waveform must be > 100ns rise and fall time.

# **APPLICATIONS** IH401 Family

In general, the IH401 family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401 requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401 to handle ±7.5V analog signals (or IH401A to handle ±10V analog signals). A typical simple PNP translator is shown in Figure 5.

XAM 10kΩ ≥ 1/4 OF IH401 +15V - ANALOG FROM TTL OPEN COLLECTOR TC03390I Figure 5

Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and toff is limited by the collector load resistor (approximately 1.5 µs for  $10k\Omega$ ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

A translator which overcomes the problems of the simple PNP stage is the Intersil IH6201.\* This translator driving an IH401 varafet produces the following typical features:

- top time of approx. 200ns ) break before
- toff time of approx. 80ns
- make switch
- TTL compatible strobing levels of
  - ID(on) + IS(on) typically 20pA up to ±10V analog signals
- ID(off) or IS(off) typically 20pA
  - Quiescent current drain of approx. 100nA in either "on" or "off" case

\*The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 6.

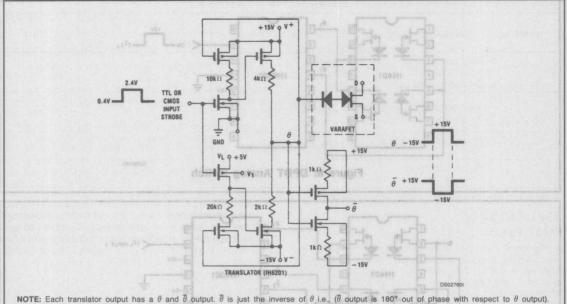


Figure 6: IH6201 Driving An IH401 1

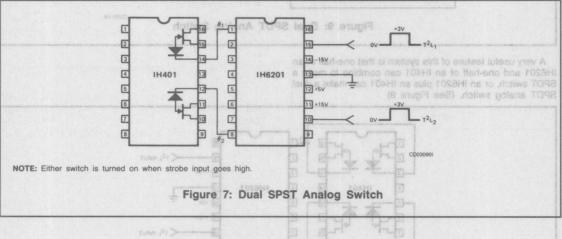
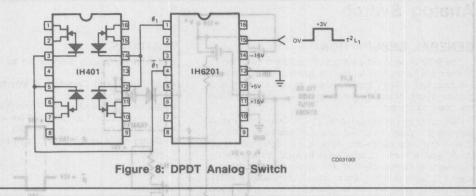
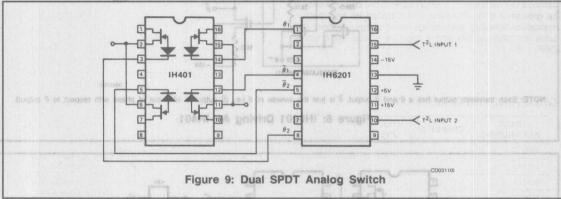
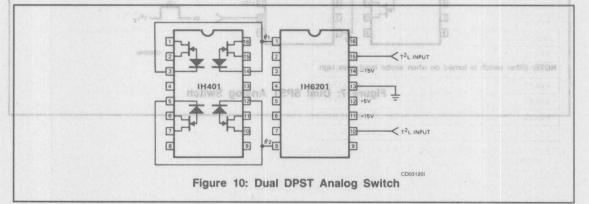


Figure 10: Dual DPST Analog Switch





A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See Figure 9)



# **Analog Switch**

# GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from TTI open collector logic (15 volts) while the even numbered devices are driven directly from low level TTL logic (5 volts). Each channel simulates a SPDT switch. SPDT switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (OV). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF

# FEATURES ...... manua shoid

- Switches Analog Signals Up to 20 Volts Peak-to-Peak
- Each Channel Complete Interfaces With Most Integrated Logic
- Switching Speeds Less Than 0.5 us of words assented
- ID(OFF) Less Than 500pA Typical at 70°C
- Effective  $r_{ds(ON)} 5\Omega$  to  $50\Omega$

- Par - - - 2

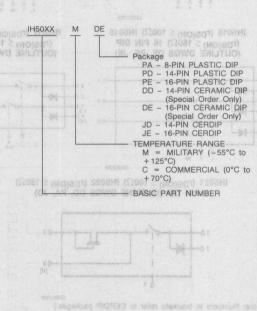
 Commercial and Military Temperature Range Operation

(DSCOM) S (SOO) 14 PIN DIP

#### ORDERING INFORMATION

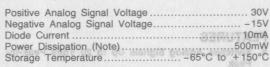
PART NUMBER	CHANNELS	LOGIC	PACKAGES	
IH5009	SOWCI AMILITU	+ 15	JD,DD,PD	
IH5010	4	+5	JD,DD,PD	
IH5011	4	+ 15	JE,DE,PE	
IH5012	4	+5	JE,DE,PE	
IH5013	3	+ 15	JD,DD,PD	
IH5014	3	+5	JD,DD,PD	
IH5015	3	+15	JE,DE,PE	
IH5016	3	+5	JE,DE,PE	
IH5017 1 = (IIO)	801) A238H (8	00 + 15 10	JD,DD,PA	
IH5018	2	+5	JD,DD,PA	
IH5019	2	+15	JE,DE,PA	
IH5020	2	+5	JE,DE,PA	
IH5021	1	+15	JD,DD,PA	
IH5022	1	+5	JD,DD,PA	
IH5023	1	+ 15	JE,DE,PA	
IH5024	1	+5	JE,DE,PA	

NOTE: Mil-Temperature range (-55°C to +125°C) available in ceramic packages only. Figure 1: Pin Connections



#### IH5009-IH5024

#### **ABSOLUTE MAXIMUM RATINGS**



	b	nuo	Gr	Isu	triv	
		offia	100	mento	anA	
perature Tempera	(Soldering,	10sec)		G	.300°C	

 Operating Temperature
 5009C Series
 0°C to +70°C

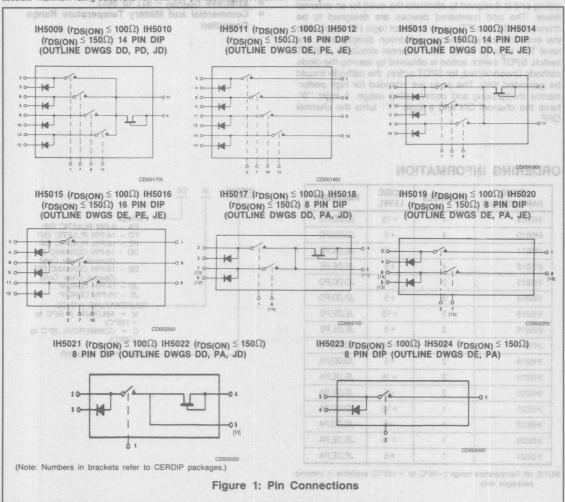
 5009M Series
 -55°C to +125°C

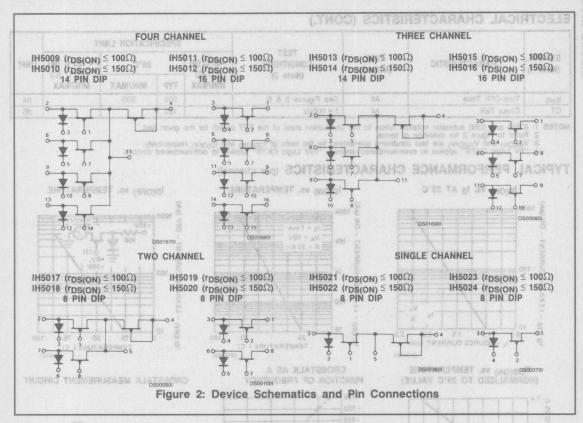
 Lead Temperature (Soldering, 10sec)
 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

Lead Tem

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





#### ELECTRICAL CHARACTERISTICS (per channel)

100 V De-1	A 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	*	TECT OF	1 6	SPECI	FICATION LIM	п	NAME OF
SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	CONDITIONS (Note 2)	-55°C (M) 0°C (C) MIN/MAX	TYP	25°C MIN/MAX	+ 125°C (M) + 70°C (C) MIN/MAX	UNIT
IN(ON)	Input Current-ON	ALL ,	$V_{IN} = 0V$ , $I_D = 2mA$		0.01	±0.5	100	μА
IN(OFF)	Input Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V$ , $V_A = \pm 10V$		0.04	(0 ) ±0.5TAR3	20	nA
IN(OFF)	Input Current-OFF	15V Logic Ckts	$V_{IN} = +11V$ , $V_A = \pm 10V$		0.04	±0.5	20	nA
VIN(ON)	Channel Control Voltage-ON	5V Logic Ckts	See Figure 7, Note 3	0.5	0.654	0.5	0.5	V
VIN(ON)	Channel Control Voltage-ON	15V Logic Ckts	See Figure 8, Note 3	1.5	2.00	1.5	1.5	V
VIN(OFF)	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 6, Note 3	moitonui s	tex esi	4.5	4.5	V
VIN(OFF)	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 8, Note 3	n out mini l	underland.	11.0	11.0	V
D(OFF)	Leakage Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V, V_A = \pm 10V$	seart has	0.02	±0.5	20	nA
D(OFF)	Leakage Current-OFF	15V Logic Ckts	V <sub>IN</sub> = + 11V, V <sub>A</sub> = ± 10V	ni venneto:	0.02	±0.5	000 + 20	nA
ID(ON)	Leakage Current-ON	5V Logic Ckts	V <sub>IN</sub> = 0V, I <sub>S</sub> = 1mA hv and		0.30	gnk±1.0vs e	1000 (M) 200 (C)	9 nAd
ID(ON)	Leakage Current-ON	15V Logic Ckts	V <sub>IN</sub> = 0V, I <sub>S</sub> = 1mA	many town		±0.5	500 (M) 100 (C)	nA
ID(ON)	Leakage Current-ON	5V Logic Ckts	V <sub>IN</sub> = 0V, I <sub>S</sub> = 2mA	distribution of	Hr. You	1.0	10	μΑ
ID(ON)	Leakage Current-ON	15V Logic Ckts	V <sub>IN</sub> = 0V, I <sub>S</sub> = 2mA	arli have in		2.0	100	μА
rDS(ON)	Drain-Source ON-Resistance	5V Logic Ckts	I <sub>D</sub> = 2mA, V <sub>IN</sub> = 0.5V	150 .bs	1000	le si 150 loqu	385 (M) 240 (C)	odΩos
rDS(ON)	Drain-Source ON-Resistance	15V Logic Ckts	I <sub>D</sub> = 2mA, V <sub>IN</sub> = 1.5V	100	80	od dago da	250 (M) 160 (C)	Ω
t(on)	Turn-ON Time	All	See Figures 5 & 6		150	500	THE STATE OF THE S	ns

#### IH5009-IH5024

## 

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

	Jamana 22	Mari I		2010	SPECI	FICATION LIM	IT	
SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST	-55°C (M) 0°C (C)	APPEARAGE SELECTION OF THE PERSON OF THE PER		+ 125°C (M) + 70°C (C)	UNIT
	16 PIN DIP	1 PIN DIP	(Note 2)	MIN/MAX	TYP	MIN/MAX	MIN/MAX	
t(off)	Turn-OFF Time	All	See Figures 5 & 6		300	500		ns
CT	Cross Talk	All	f = 100Hz	700	120			dB

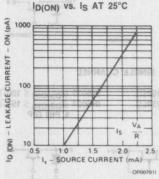
NOTES 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

2: Refer to Figure 2 for definition of terms.

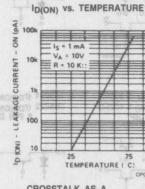
3: VIN(ON) and VIN(OFF) are test conditions guaranteed by the tests of rDS(ON) and ID(OFF) respectively.

4: "5V Logic CKTS" applies to even-numbered devices. "15V Logic CKTS" applies to odd-numbered devices

#### TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

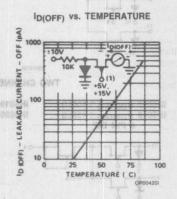


RDS(ON) VS. TEMPERATURE (NORMALIZED TO 25°C VALUE)

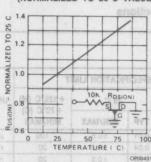


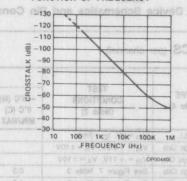
CROSSTALK AS A **FUNCTION OF FREQUENCY** 

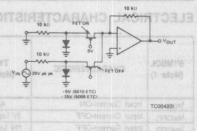
100



CROSSTALK MEASUREMENT CIRCUIT







#### **DETAILED DESCRIPTION**

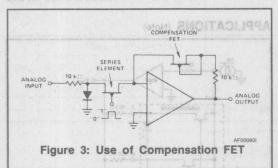
The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual - When placed in series with the feedback resistor (Figure 3) ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

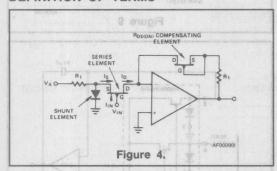
Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that VGS = 0, is intended to compensate for the on-resistance of the switch. the gain is given by:

GAIN = 
$$\frac{10k\Omega + r_{DS(ON)}(compensator)}{10k\Omega + r_{DS(switch)}}$$



Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within  $50\Omega$ . Selections down to  $5\Omega$  are available however. Contact factory for details. Since the absolute value of  $r_{DS(ON)}$  is guaranteed only to be less than  $100\Omega$  or  $150\Omega$ , a substantial improvement in gain accuracy can be obtained by using the compensating FET.

#### **DEFINITION OF TERMS**

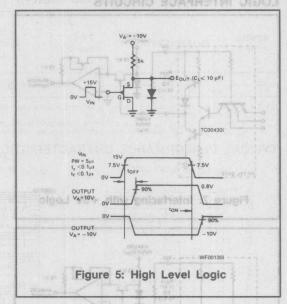


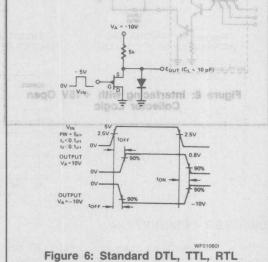
#### NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a  $\pm 10 \text{V}$  analog input is being switched by TTL open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

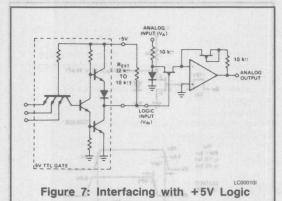
When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

#### SWITCHING CHARACTERISTICS





#### LOGIC INTERFACE CIRCUITS



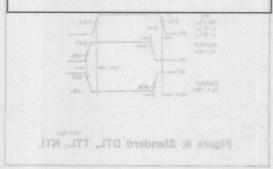
ANALOG INPUT (Vig)

10 kt:

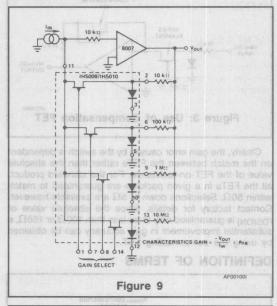
ANALOG
OUTPUT

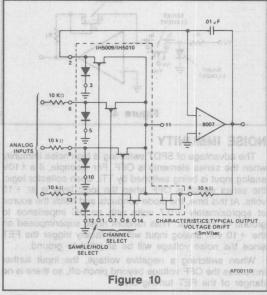
ANALOG
OUTPUT

Collector Logic



#### **APPLICATIONS** (Note)





NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches".

## IH5025-IH5038

# Positive Signal Analog Switch

# **WINTERSIL**

H5026 (τρε(ομ) ≤ 160Ω) 14 PH DIP

#### **GENERAL DESCRIPTION**

The IH5025 series of analog switches was designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 14) or by capacitor isolation (Figure 13). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

#### ORDERING INFORMATION

BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5025	4	+15	JD,DD,PD
IH5026	4	+5	JD,DD,PD
IH5027	4	+15	JE,DE,PE
IH5028	4	+5	JE,DE,PE
IH5029	3	+15	JD,DD,PD
IH5030	3	+5	JD,DD,PD
IH5031	3	+ 15	JE,DE,PE
IH5032	3	+5	JE,DE,PE
IH5033	2	+15	JD,DD,PA
IH5034	2	+5	JD,DD,PA
IH5035	2	+15	JE,DE,PA
IH5036	2	+5	JE,DE,PA
IH5037	1	+15	JD,DD,PA
IH5038	1	+5	JD,DD,PA

NOTE: Mil-Temperature range (-55°C to +125°C) available in WHARD AUDITOR ceramic packages only.

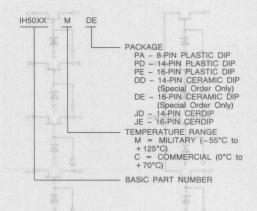
#### **FEATURES**

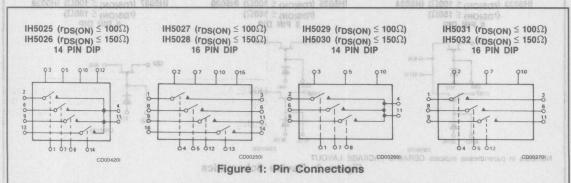
MISDES (FUSION) SECRET

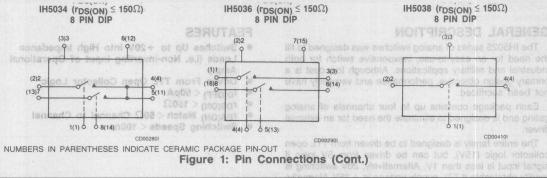
- Switches Up to +20V Into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)
- Driven From TTL Open Collector Logic
- ID(OFF) < 50pA
- rDS(ON) < 150Ω

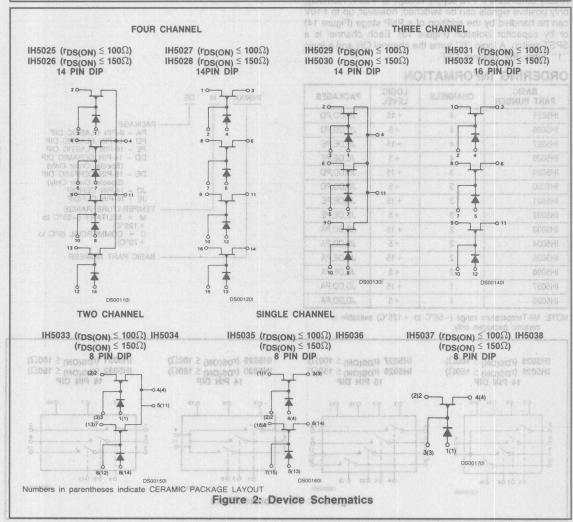
(Costo) ≤ (Moyaqs) scool)

- rDS(ON) Match < 50Ω Channel to Channel</li>
- Switching Speeds < 100ns









#### IH5025-IH5038

#### **ABSOLUTE MAXIMUM RATINGS**

Positive Analog Signal Voltage	9		25V
Negative Analog Signal Voltage			-0.5VDC
Drain Current	Siliper		25mA
Power Dissipation (Note)			.500mW
Storage Temperature	-65°C	to	+150°C

Operating Temperature	
5025M Series	55°C to +125°C
Lead Temperature (Soldering,	10sec)300°C

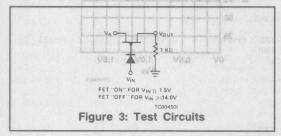
NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

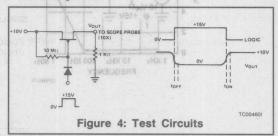
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

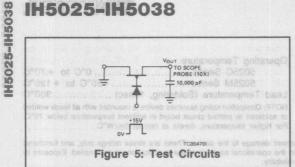
#### **ELECTRICAL CHARACTERISTICS** (per channel)

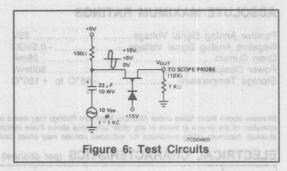
		(ienner)	TERISTICS (per o	DARAC	PERPU	TYPICAL		
SYMBOL (Note 1)	CHARACTERISTIC V (MO)	TYPE	DE TEST CONDITIONS (M)		19W T 25	°C (390)	+ 125°C (M)	UNIT MIN/MAX
	CTTTTT		I man	0°C (C)	TYP	MIN/MAX	+70°C (C)	
lin(on)	Input Current-ON	All	V <sub>IN</sub> = 0V	T-(2)±	0.30	1.0	100 (M) 25 (C)	nA (max)
IN(OFF)	Input Current-OFF	All	V <sub>IN</sub> = 15V		0.20	1:0	50 (M) 50 (C)	nA (max)
VIN(ON)	Channel Control Voltage-ON	AAII	See Figure 3	1.5	16	1.5	0 1.5	V (max)
VIN(OFF)	Channel Control Voltage-OFF	All	See Figure 3	14.0	Ver+	14.0	14.0	V (min)
ID(OFF)	Leakage Current-OFF	All	See Figure 5		0.06	0.5	100 (M) 50 (C)	nA (max)
ID(ON)	Leakage Current-ON	Odd Nos.	See Figure 6		1.00	10.0	5000 (M) 250 (C)	nA (max)
ID(ON)	Leakage Current-ON	Even Nos.	See Figure 6		0.10	1.0	500 (M) 25 (C)	nA (max)
rDS(ON)	Drain-Source ON-Resistance	Odd Nos.	V <sub>IN</sub> = 0.5V, I <sub>D</sub> = 1mA	100	60.00	100,0	250 (M) 150 (C)	Ω (max)
rDS(ON)	Drain-Source ON-Resistance	Even Nos.	V <sub>IN</sub> = 0.5V, I <sub>D</sub> = 1mA	150	90.00	150.0	385 (M) 240 (C)	Ω (max)
rDS(ON)	Drain-Source ON-Resistance	Odd Nos.	V <sub>IN</sub> = 1.0V, I <sub>D</sub> = 1mA	160	85.00	160.0	420 (M) 250 (C)	Ω (max)
rDS(ON)	Drain-Source ON-Resistance	Even Nos.	V <sub>IN</sub> = 1.0V, I <sub>D</sub> = 1mA	TIT	110.00	200.0	400 (M) 250 (C)	Ω (max)
t(on)	Turn-ON Time	All	See Figure 4		0.10	0.2	-0.4	μs (max)
t(off)	Turn-OFF Time	All	See Figure 4	SHE SE	0.10	0.2	0.4	μs (max)
Q <sub>(INJ)</sub>	Charge Injection	All	See Figure 5	THE ST	7.0	20.0		mV <sub>p-p</sub> (max)
V <sub>A</sub> (OFF)	Cross Coupling Rejection	All	See Figure 6		0.10	1.0	-8 %	mV <sub>p-p</sub> (max)
Δr <sub>DS</sub> (ON)	Channel to Channel rDS(ON) Match	All	V <sub>IN</sub> = 0.5V, I <sub>D</sub> = 1mA	13 13	25.00	the Contract		Ω (max)

Note 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

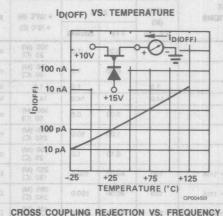


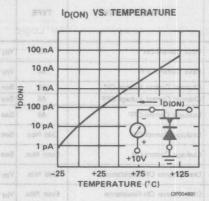












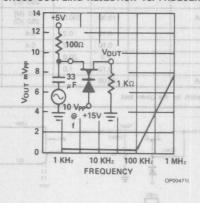
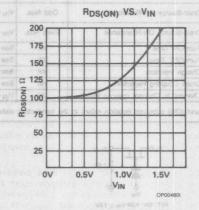


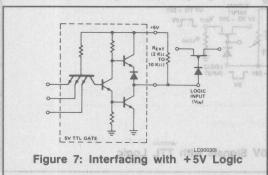
Figure 4: Test Circuits

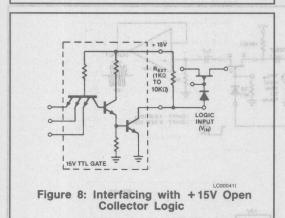


3

#### LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pullup resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.





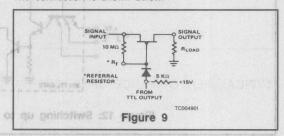
#### THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that they may be driven by floating outputs. This family is generally used when operating into the non-inverting input of an operational amplifier, while the IH5009 series is used in operations where the output feeds into the inverting (virtual ground) input.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacitance vs. voltage relationship for the diode junctions. This C vs. V, when integrated, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-

Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched. The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:



For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

#### **APPLICATIONS**

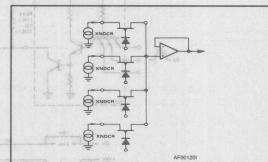


Figure 10: Multiplexer from Positive Output Transducers

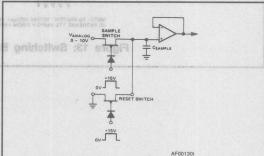
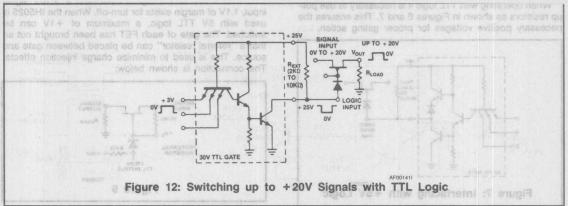
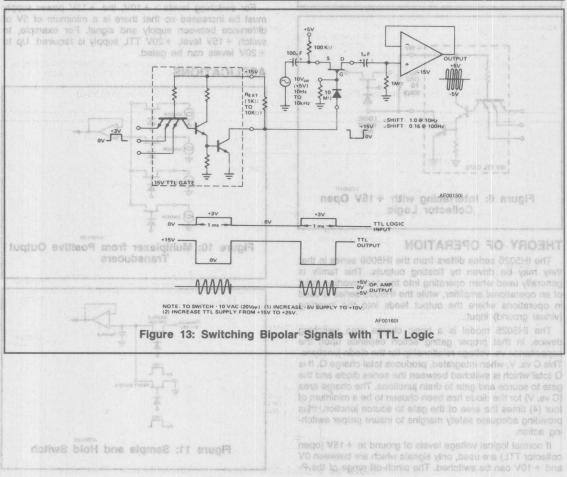


Figure 11: Sample and Hold Switch

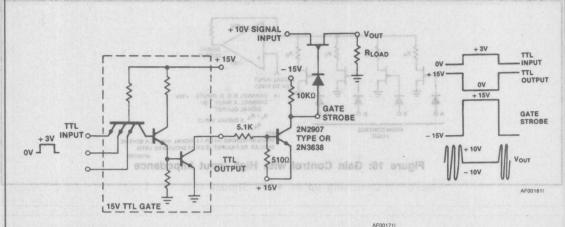
2 75





APPLICATIONS (CONT.)

**APPLICATIONS (CONT.)** 



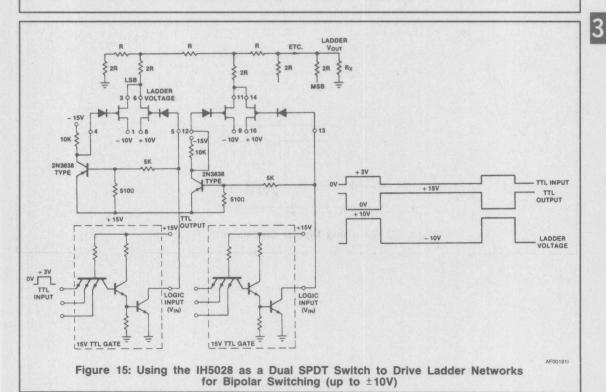
ADVANTAGES OVER FIGURE NO. 10 METHOD

- A. DC LEVELS OF UP TO ±10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100kHz; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10MHz TO 10kHz.
- B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES

- A. PNP CKT DRAWS 3mA, WHEN ON; THUS ADDS 3mA x 30V = 90mW POWER DISS.
- B.  $t_{\rm ON}$  TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100ns (BEFORE IN FIGURE NO. 13 TO)  $1-2\mu s$  NOW.

Figure 14: Switching Bipolar Signals with TTL Logic (Alternate Method)



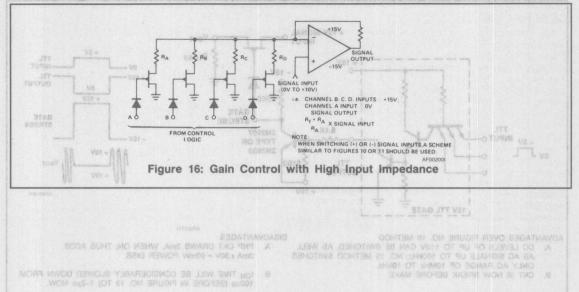
3-77

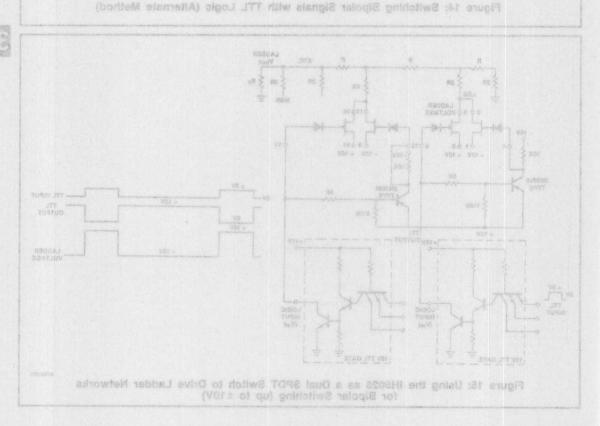
## IH5025-IH5038

APPLICATIONS (CONT.)



APPLICATIONS (CONT.)





## IH5040-IH5047 High-Level CMOS Analog Switch



#### GENERAL DESCRIPTION (IsrameT virA) Inemail

The IH5040 family of solid state analog switches use an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious problem.

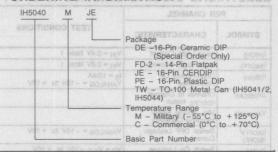
Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1 $\mu$ A. Also, the 5040 guarantees Break-Before-Make switching, accomplished by extending the  $t_{on}$  time (300ns TYP.) so that it exceeds  $t_{off}$  time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

#### **FEATURES**

- Switches Greater Than 20Vpp Signals With ±15V
   Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching toff 200ns, ton
   Substituting toff 200ns, ton
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- New DPDT & 4PST Configurations
- Complete Monolithic Construction

#### ORDERING INFORMATION O JACISTOS JA



#### FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	T	PE SOS	rDS(on)	PIN FOR PIN COMPATIBLE
IH5040	- JA 7	SPST	75Ω	HI5040/DG5040
IH5041	Dual	SPST	75Ω	HI5041/DG5041
IH5042		SPDT	75Ω	HI5042/DG5042
IH5043	Dual	SPDT	75Ω	HI5043/DG5043
IH5044	A Abt	DPST	75Ω	HI5044/DG5044
IH5045	Dual	DPST	75Ω	HI5045/DG5045
IH5046		DPDT	75Ω	HI5046
IH5047		4PST	75Ω	ylogus HI5047

NOTE 1. See Switching State diagrams for applicable package equivalency.

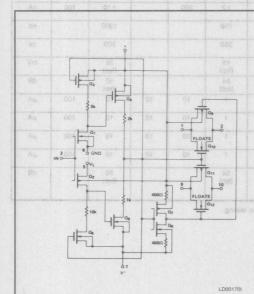


Figure 1: Functional Driver, Typical Driver, Gate — IH5042

V <sup>+</sup> -V <sup>-</sup> < 33V	Current (Any Terminal) < 30mA
V <sup>+</sup> -V <sub>D</sub> <30V	Storage Temperature65°C to +150°C
V <sub>D</sub> -V <sup>-</sup> <30V	Operating Temperature55°C to +125°C
V <sub>D</sub> -V <sub>S</sub>	Lead Temperature (Soldering, 10sec)300°C
V <sub>L</sub> -V <sup>−</sup> (33V	Power Dissipation450mW
V <sub>L</sub> -V <sub>IN</sub>	(All Leads Soldered to a P.C. Board)
V <sub>L</sub> -GND < 20V	Derate 6mW/°C Above 70°C
V <sub>IN</sub> -GND< 20V	and destructive latch-up has been eliminated. Early CMOS

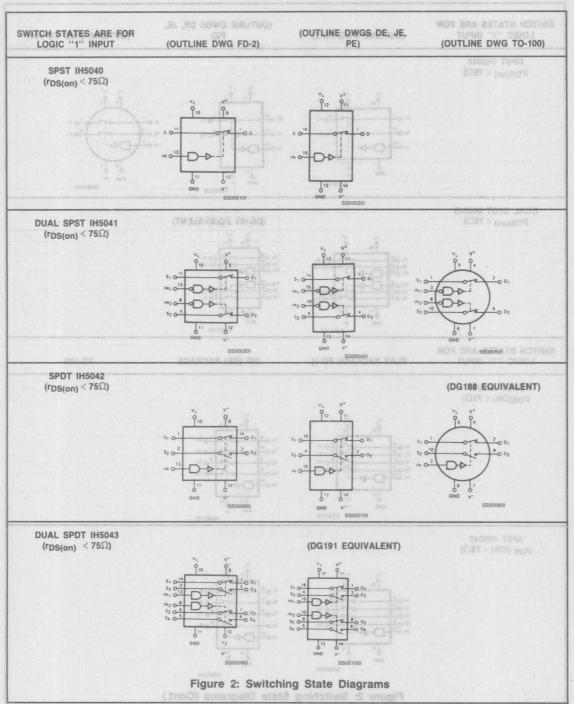
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (@ 25°C, V+ = +15V, V- = -15V, VL = +5V)

PI	ER CHANNEL	BI M DESHE	5040	6402 edi .oziA MIN/MAX LIMITSel ai Inemeriupe						
B	BANKS MACHINE	TEST CONDITIONS MILITARY		s ,pairleti	dake sw	ALEIE SE	UNIT			
SYMBOL	CHARACTERISTIC		-55°C	+ 25°C	+ 125°C	0	+ 25°C	+70°C	dendir	
IIN(ON)	Input Logic Current	V <sub>IN</sub> = 2.4V Note 1	±1	±1	10	±1	±1	10	μА	
IIN(OFF)	Input Logic Current	V <sub>IN</sub> = 0.8V Note 1	±1	±1	10	±1	±1	10	μΑ	
rDS(on)	Drain-Source On Resistance	Is = 10mA VANALOG = -10V to +10V	75	75	150	80	80	130	Ω	
Δr <sub>DS</sub> (ON)	Channel to Channel rDS(ON) Match		niq-rot	25 (typ)	ns hogu	evorigini o	30 (typ)	of the 50	Ω	
VANALOG	Min. Analog Signal Handling Capability			± 11 (typ)		0 101 0	± 10 (typ)	DI IBORD	V	
ID(OFF)/ IS(OFF)	Switch OFF Leakage Current	VANALOG = -10V to +10V		±1	100		±5	100	nA	
ID(ON) + IS(ON)	Switch On Leakage Current	$V_D = V_S = -10V \text{ to } +10V$		±2	200		±10	100	nA	
ton	Switch "ON" Time	$R_L = 1k\Omega$ , $V_{ANALOG} = -10V$ to +10V See Fig. 3		750			1000		ns	
toff	Switch "OFF" Time	$R_L = 1k\Omega$ , $V_{ANALOG} = -10V$ to +10V See Fig. 3		350			500		ns	
Q(INJ.)	Charge Injection	See Fig. 3		15 (typ)			20 (typ)		mV	
OIRRUM EE	Min. Off Isolation Rejection Ratio	$f = 1MHz$ , $R_L = 100\Omega$ , $C_L \le 5pF$ See Fig. 5	A	54 (typ)			50 (typ)	Br.	dB	
1 054030	V + Power Supply Quiescent Current	H6042 BPDT	1	1	10	10	10	100	μΑ	
GEORG O	V Power Supply Quiescent Current	$V^{+} = +15V, V = -15V, V_{L} = +5V$ $V_{L} = +5V$	1	1	-10	10	10	100	μА	
IT LQ 84	+ 5V Supply Quiescent Current	HISO46 DPST	1	1	10	10	10	100	μА	
IGND	Gnd Supply Quiescent Current	TP9A APST	1	1	10	10	10	100	μΑ	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Fig. 6		54 (typ)		210	50 (typ)		dB	

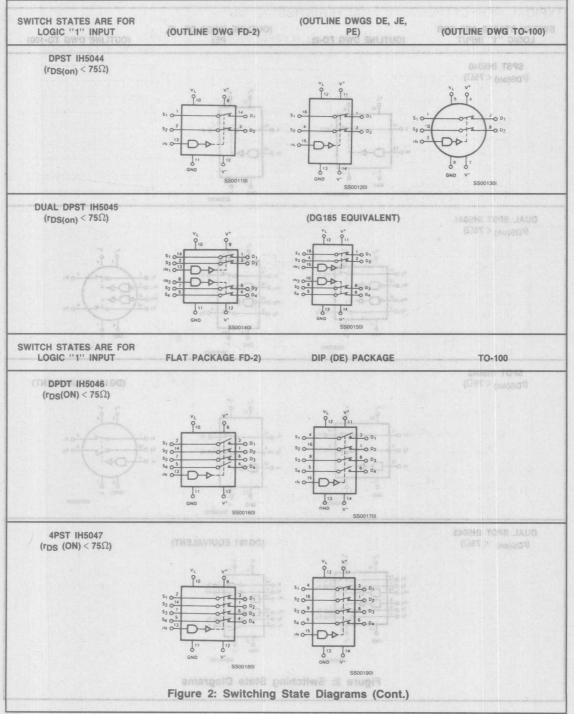
Note 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

Figure 1: Functional Driver, Typical Oriver,



#### IH5040-IH5047





#### TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) AMO 30MAMAO ABY JACKYT

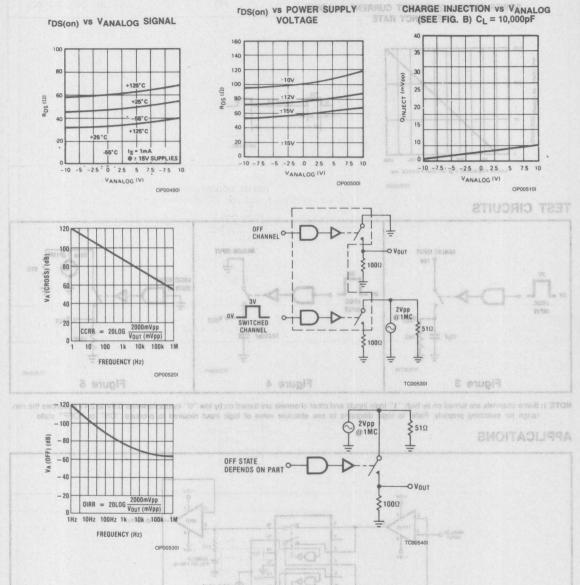
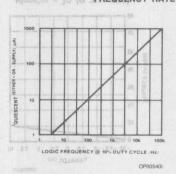
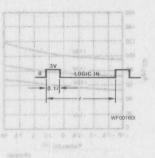


Figure 6: Improved Sample & Hold Using IH5043

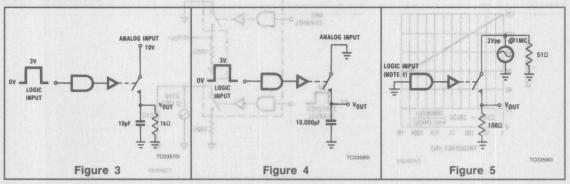
## POWER SUPPLY QUIESCENT CURRENT VS LOGIC OF BY (NO) 807





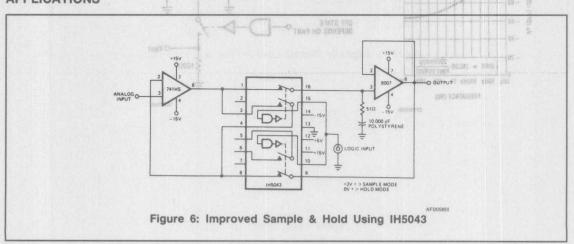


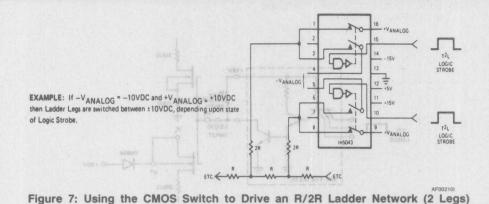
#### TEST CIRCUITS



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

#### **APPLICATIONS**





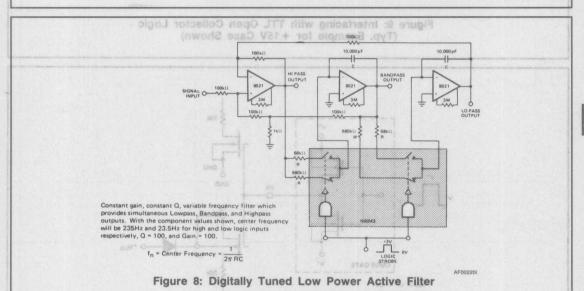
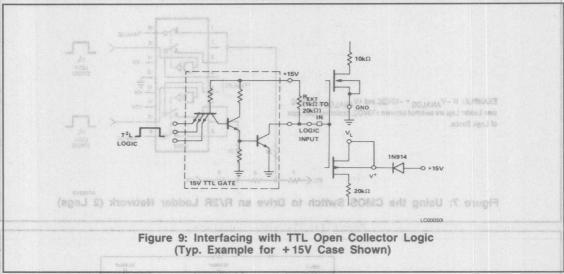


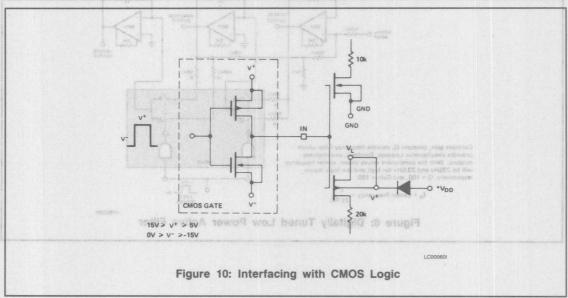
Figure 19: Interfercing with CMOS Logic

## IH5040-IH5047

## **WINTERSIL**

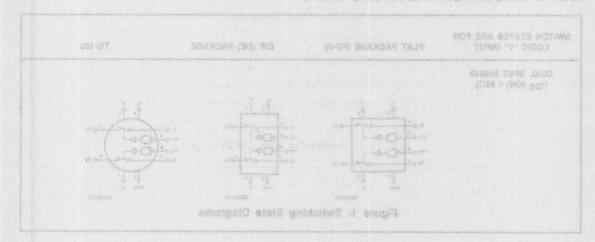
**APPLICATIONS (CONT.)** 





#### PHATUS TABR The IHSD48 family of analog switches is especial? (LgyT) Vm3--nolfgg Aut med Then tuA or low charge injection and low leakage. Const. IOS, PMOS Compatible ncludes our CMOS high level driver direaltry combin Willn Supply Turn-Off (.gyT) Oto O GND Ha With 1H5040 Family TIL LOGIC -O + 15V OR + VCC(V1 TERMINAL) 5V TTL GATE **ξ10**Ω Figure 11: TTL Logic Interface

(DS(on)	ваут	INVERSE.
Ω36 Ω36 Ω36 Ω36		PHSO4B Dust PHSO49 Dust INE050 INSO51 Dust



### **CMOS Analog Switches**

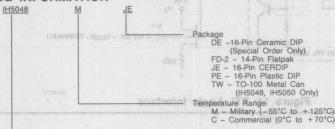
#### GENERAL DESCRIPTION

The IH5048 family of analog switches is especially made for low charge injection and low leakage. Construction includes our CMOS high level driver circuitry combined with unique ''VARAFET'' switches.

#### **FEATURES**

- Low Charge Injection—5mV (Typ.)
- Quiescent Current Less Than 1μA
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low rps(on) 35Ω (Typ.)
- Pin-Out Compatible With IH5040 Family



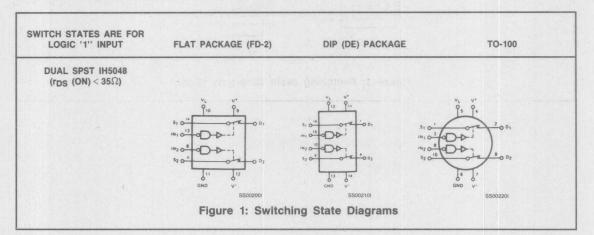


Basic Part Number

#### ORDERING INFORMATION

INTERSIL PART NO.	TYPE	rDS(on)
IH5048 Dual	SPST	35Ω
IH5049 Dual	DPST	35Ω
IH5050	SPDT	35Ω
IH5051 Dual	SPDT	35Ω

NOTE 1. See Switching State diagrams for applicable package equivalency.



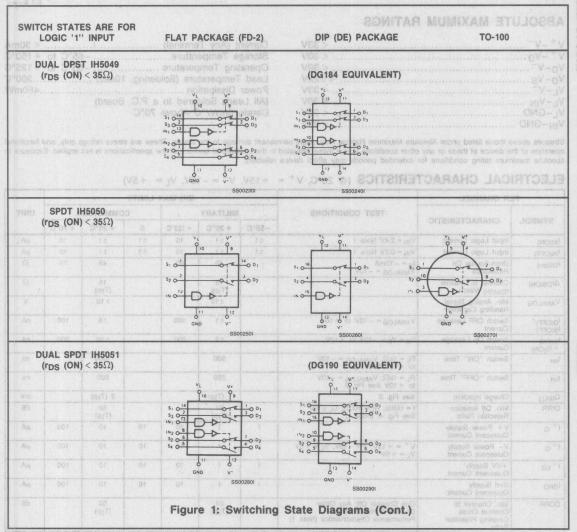


Figure 2

Figure 2

Figure 3

Figure 3

Figure 4

Figure 4

Figure 3

Figure 6

#### IH5048-IH5051



#### **ABSOLUTE MAXIMUM RATINGS**

V+-V- 601-0T EDANGE	< 33V	Current (Any Terminal)< 30mA
V <sup>+</sup> -V <sub>D</sub>	< 30V	Storage Temperature65°C to +150°C
V <sub>D</sub> -V <sup>-</sup>	< 30V	Operating Temperature55°C to +125°C
V <sub>D</sub> -V <sub>S</sub>	< ±22V	Lead Temperature (Soldering, 10sec)300°C
V <sub>L</sub> -V <sup>-</sup>		Power Dissipation450mW
VV <sub>IN</sub>	< 30V	(All Leads Soldered to a P.C. Board)
V <sub>L</sub> -GND	< 20V	Derate 6mW/°C Above 70°C
V <sub>IN</sub> -GND	< 20V	001110

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS (@ 25°C, V+ = +15V, V = -15V, VL = +5V)

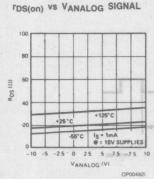
PER CHANNEL		and the second s	MIN/MAX LIMITS							
		TEST CONDITIONS	MILITARY			(	UNIT			
SYMBOL CHARACTERISTIC		-55°C	+ 25°C	+ 125°C	0	+ 25°C	+70°C			
IN(ON)	Input Logic Current	V <sub>IN</sub> = 2.4V Note 1	±1	±1	10	±.1	±1	10	μΑ	
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 0.8V Note 1	±1	±1	10	±1	±1	10	μΑ	
rDS(on)	Drain-Source On Resistance	Is = -10mA VANALOG = -10V	(0.0)	40	60		45	75	Ω	
Δr <sub>DS</sub> (ON)	Channel to Channel rDS(ON) Match	10 10 00	\$0.Qm	15 (Typ)	- 1 C SF		15 (Typ)		Ω	
VANALOG	Min. Analog Signal Handling Capability			±10			±10		٧	
ID(OFF)/ IS(OFF)	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -10V to +10V		±1	100		±5	100	nA	
ID(ON) + IS(ON)	Switch On Leakage Current	$V_D = V_S = -10V \text{ to } +10V$	pinner constitu	±2	200		±10	200	nA.	
ton	Switch "ON" Time	$R_L = 1k\Omega$ , $V_{ANALOG} = -10V$ to +10V See Fig. 2		500			1000	MC (MI)	ns	
toff	Switch "OFF" Time	$R_L = 1k\Omega$ , $V_{ANALOG} = -10V$ to +10V See Fig. 2		250			500		ns	
Q(INJ.)	Charge Injection	See Fig. 3	der Aye	1 (Typ)		KAN	2 (Typ)	Maria de	mV	
OIRR	Min. Off Isolation Rejection Ratio	$f = 1 MHz$ , $R_{L} = 100 \Omega$ , $C_{L} \le 5 pF$ See Fig. 4, (Note 1)	1000	54 (Typ)	1012		50 (Typ)		dB	
I <sup>+</sup> Q	V + Power Supply Quiescent Current	-3-C1200	1	14	10	10	10	100	μΑ	
I- Q	V - Power Supply Quiescent Current	$V^{+} = +15V, V = -15V, V_{L} = +5V$ $V_{L} = +5V$	1002	201-	10	10	10	100	μΑ	
I- rd	+ 5V Supply Quiescent Current	10 10	-1	9 1	10	10	10	100	μΑ	
IGND	Gnd Supply Quiescent Current	108500388	1 100000	1	10	10	10	100	μΑ	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Performance Characteristics (Note 1)	itching	54 (Typ)	Figur		50 (Typ)		dB	

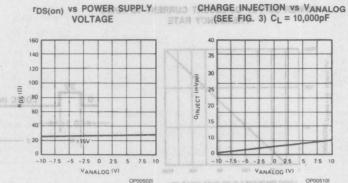
Note 1: Not tested in production.

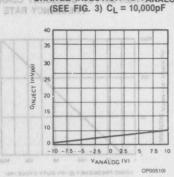
#### **TEST CIRCUITS**

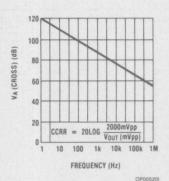
NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

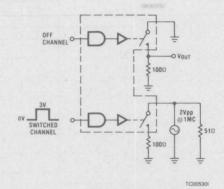
#### TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) TAHO BOMAMROTRES JACISTY

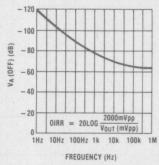


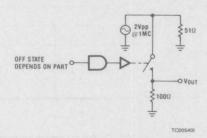






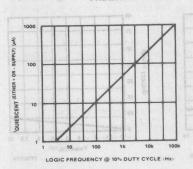


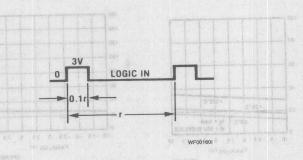


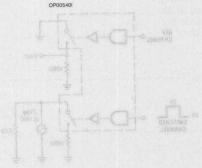


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## POWER SUPPLY QUIESCENT CURRENT VS LOGIC

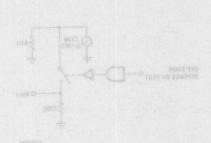


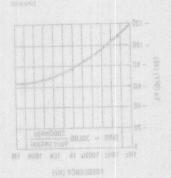






IDERCOIN VS VANALOG SIGNAL





## IH5052/IH5053 QUAD CMOS Analog Switch

#### GENERAL DESCRIPTION (SAMPLET VIA) MERLID

The IH5052/3 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem. Key performance advantages are TTL compatibility and ultra low-power operation — the quiescent current requirement is less than 10μA.

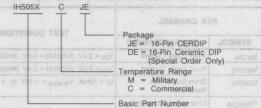
The IH5052/3 also guarantees Break-Before-Make switching. This is accomplished by extending the ton time (400ns TYP.) such that it exceeds topp time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logical "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logical "1" (2.4V or more) at its control inputs.

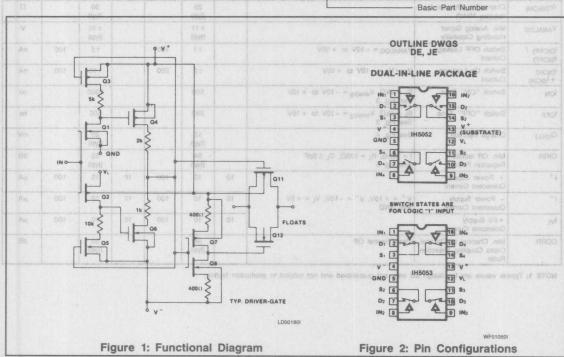


#### **FEATURES**

- Switches Greater Than 20Vpp Signals With ±15V
   Supplies
- Quiescent Current Less Than 10μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching toff 100ns, ton
   250ns Typical
- TTL, CMOS Compatible
- Non-Latching With Supply Turn-Off
- IH5052 4 Normally Closed Switches
- IH5053 4 Normally Open Switches

#### ORDERING INFORMATION JACISTOLIS





## IH5052/IH5053



#### **ABSOLUTE MAXIMUM RATINGS**

V+-V	< 33V
V <sup>+</sup> -V <sub>D</sub>	< 30V
V <sub>D</sub> -V <sup>-</sup>	< 30V
V <sub>D</sub> -V <sub>S</sub> <	±22V
V <sub>L</sub> -V <sup>-</sup>	
V <sub>L</sub> -V <sub>IN</sub>	< 30V
V <sub>L</sub> -GND	< 20V
V <sub>IN</sub> -GND	< 20V

Current (Any Terminal)	< 30mA
Storage Temperature65°C to	
Operating Temperature55°C to	
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	
(All Leads Soldered to a P.C. Board)	
Derate 6mW/°C Above 70°C	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

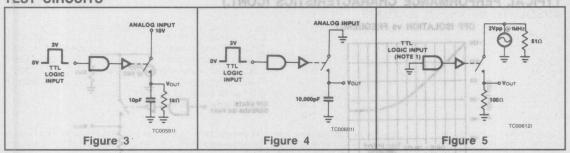
## ELECTRICAL CHARACTERISTICS (TA = 25°C, V+ = +15V, V- = -15V, VL = +5V)

DED CHANNEL		T T THE STORE	MIN/MAX LIMITS IS AN ENWERT SE							
PER CHANNEL		TEST CONDITIONS	oran tant	MILITAR	Y	C	THU H			
SYMBOL	CHARACTERISTIC	TEST CONDITIONS	-55°C	+25°C	+ 125°C	0	+ 25°C	+70°C	UNIT	
IN(ON)	Input Logic Current	V <sub>IN</sub> = 2.4V (IH5053) = 0.8V (IH5052)	10	sadi s	10	we Sa	100r	nputs, t	ιο μΑ	
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 0.8V (IH5053) = 2.4V (IH5052)	10	±10.00	10	osed v	±10	switches	μΑ	
rDS(ON)	Drain-Source On Resistance	$I_S = 10$ mA, $V_{analog} = -10V$ to $+10V$	75	75	100	80	80	100	Ω	
△rDS(ON)	Channel to Channel Can Tos(ON) Match			25 (typ)			30 (typ)		Ω	
VANALOG	Min. Analog Signal Handling Capability	2004		±11 (typ)			± 10 (typ)		V	
ID(OFF) /	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -10V to +10V		±1	100		±5	100	nA	
I <sub>D</sub> (ON) + I <sub>S</sub> (ON)	Switch On Leakage Current	V <sub>D</sub> = V <sub>S</sub> = -10V to +10V		±2	200		±10	100	nA	
ton	Switch "ON" Time	$R_L = 1k\Omega$ , $V_{analog} = -10V$ to $+10V$ See Fig. 3		500			1000		ns	
<sup>t</sup> OFF	Switch "OFF" Time	$R_L = 1k\Omega$ , $V_{analog} = -10V$ to $+10V$ See Fig. 3		250	10	31-	500	*	ns	
Q(INJ.)	Charge Injection	See Fig. 4		15 (typ)	3	es	20 (typ)		mV	
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, $R_L = 100\Omega$ , $C_L \le 5pF$ See Fig. 5		54 (typ)		(4)	50 (typ)		dB	
1+	+ Power Supply Quiescent Current	110	10	10	100	10	10	100	μΑ	
1-	- Power Supply Quiescent Current	$V^{+} = +15V, V^{-} = -15V, V_{L} = +5V$ with GND	10	10	100	10	10	100	μΑ	
IVL	+ 5V Supply Quiescent Current	G-177 an 273-033 1	10	10	100	10	10	100	μΑ	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)	1 4		50 (typ)		dB	

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

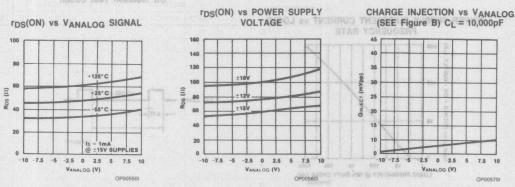
## 2

#### TEST CIRCUITS

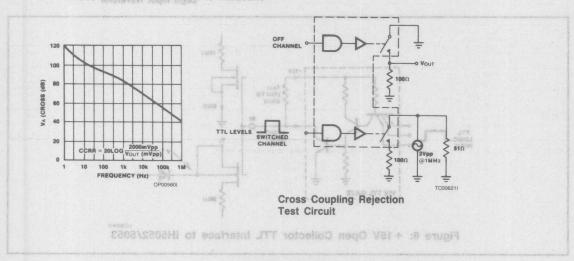


NOTE 1: The 5053 is turned on by high "1" logic inputs and the 5052 is turned on by low "0" inputs; however 0.8V to 2,4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

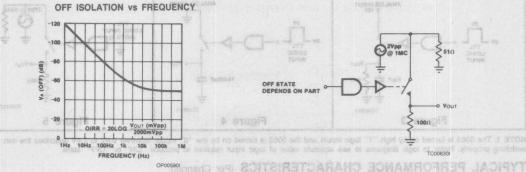
#### TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

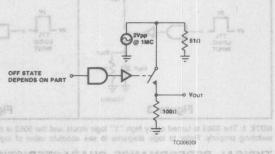


CROSS COUPLING REJECTION vs FREQUENCY



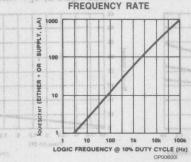


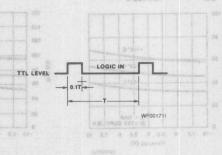




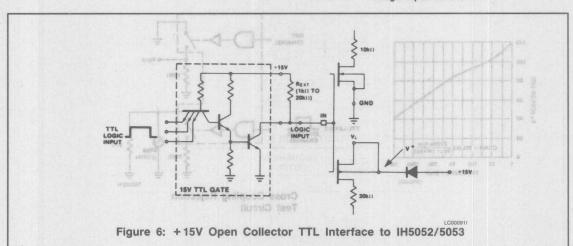
Off Isolation Test Circuit

108(ON) VE POWER SUPPLY POWER SUPPLY QUIESCENT CURRENT VS LOGIC



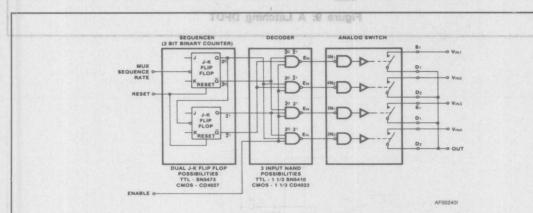


Logic Input Waveform



**BINITERS II** 





#### TRUTH TABLE (IH5052)

ENABLE	MUX SEQUENCE SEQUE			SWITCH STATES (-DENOTES OFF)				
	RATE	20	21	SW1	SW2	SW3	SW4	
0	0	0	0	_		_	_	
1	0	0	0	ON	-	_	_	
1	1 pulse	1	0	_	ON	_		
1	2 pulses	0	1		_	-	_	
1	3 pulses	1	1	_	_	_	ON	
1	4 pulses	0	0	ON	_	_	_	

Figure 8: 4-Channel Sequencing MUX

## IH5052/IH5053

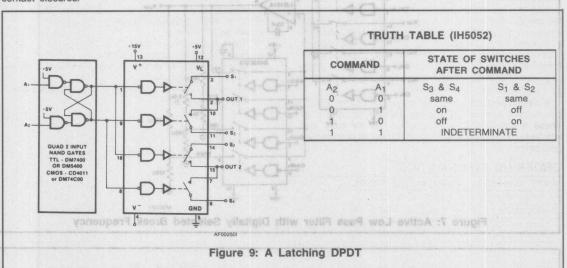


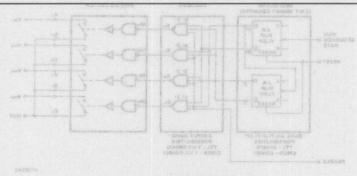
PROGRAMMABLE GAIN NON-INVERTING

**APPLICATIONS** 

#### A LATCHING DPDT SWITCH

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The  $A_1$  and  $A_2$  inputs are normally low. A HIGH input to  $A_2$  turns  $S_1$  and  $S_2$  ON, a HIGH to  $A_1$  turns  $S_3$  and  $S_4$  ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.





#### TRUTH TABLE (ME052)

			RECER	SEQUE	MUX	ENABLE
swa swa		rwa				
-			0			
	-	ИО				
			0		selug (	
		2000				
		MO				

Figure 8: 4-Channel Sequencing MUX

# 8-Channel Fault Protected CMOS Analog Multiplexer

#### GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI508A and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to  $\pm 25$ V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

A binary 3-bit address code together with the ENable input allows selection of any one channel, or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

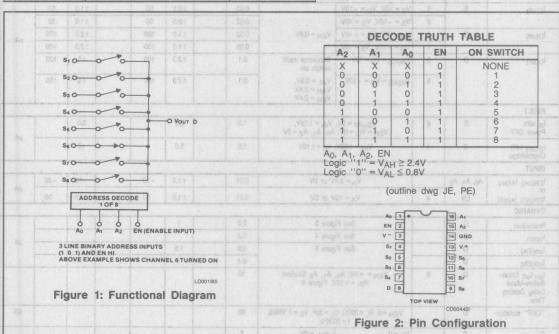
# **WINTERSIL**

#### **FEATURES**

- All Channels OFF When Power OFF, for Analog Signals up to ±25V
- Power Supply Quiescent Current Less Than 1mA
- ±13V Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- Pin Compatible With HI-508A
- Any Channel Turns OFF if Input Exceeds Supply Rails by Up to ±25V
- TTL and CMOS Compatible Binary Address and ENable Inputs

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	-55°C to +125°C	16 pin CERDIP
IH5108IJE	-20°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP



	THE STREET WAS DESIGNATED AND A STREET
V <sub>IN</sub> (A, EN)	Current (Any Terminal)
V <sub>IN</sub> (A, EN) to Ground	Operating Temperature55 to 125°C
Vs or Vp to V <sup>+</sup> +25V, -40V	Storage Temperature65 to 150°C
Vs or V <sub>D</sub> to V <sup>-</sup> 25V, +40V	Lead Temperature (Soldering, 10sec)300°C
V <sup>+</sup> to Ground	Power Dissipation*1200mW
V <sup>-</sup> to Ground -16V	*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS (V+ = 15V, V- = -15V, V<sub>EN</sub> = 2.4V, unless otherwise specified.)

Address and	e Dinary	NO	TEST CONDITIONS					MAX	LIMITS	OALU	eqme	do s
CHARACTERISTIC	MEASURED	TESTS				with the	W SUFFI	MBot epo	ress co	C SUFFI)	lary 3-)	TINU
	TERMINAL	PER TEMP		25°C	-55°C	25°C	125°C	-20°C/ 0°C	25°C	85°C/ 70°C		
SWITCH		Schools			Overtheche	9 YUN	senen	ISO TOCK	a augm s	NGISW42	TENT (B	DETTEL
fDS(on)	S to D	8	V <sub>D</sub> = 10V, I <sub>S</sub> = -1.0mA	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Ω
		8	V <sub>D</sub> = -10V I <sub>S</sub> = -1.0mA	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V	500	1000	1000	1500	1200	1200	1800	TFLAS
Δr <sub>DS(on)</sub>			$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)min}}$		5 0 0		125°d	of O°C	3		OSMJE	6HI %
			Vc=	±10V 910 steple	via. 31		0"0	01 010			10801	1115
IS(off)	S	8	$V_S = 10V, V_D = -10V$		0.02	- American district	±0.5	50		±1.0	50	
C(OII)		8	$V_S = -10V, V_D = 10V$		0.02		±0.5	50		±1.0	50	1
ID(off)	D D	THE PERSON	$V_D = 10V, V_S = -10V$	V <sub>EN</sub> = 0.8V	0.02		±1.0	100	THE SECOND	±2.0	100	-
Livernation	1000	431	V <sub>D</sub> = -10V, V <sub>S</sub> = 10V		0.05		±1.0	100		±2.0	100	nA
ID(on)	D	8		Sequence each switch on	0.1		±2.0	100	0 0	±50	100	
970		8	V <sub>S(AII)</sub> = V <sub>D</sub> = -10V	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V, V <sub>EN</sub> = 2.4V	0.1		±2.0	100	0 0	±5	100	
FAULT 8		1	0 0 1		DI-TU	1 1 1 1			-0"-0	G-man	sa sa	
ls with Power OFF	S	8		V <sub>SUPP</sub> = 0V, V <sub>IN</sub> = ±25V, V <sub>EN</sub> = V <sub>O</sub> = 0V, A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> = 0V		4	2.0		000	5.0	a	μА
S(off) with Overvoltage	S	8	V <sub>IN</sub> = ±25V	$V_0 = \pm 10V$	1.0		5.0	-	-040	10	8	μΑ
INPUT		Are	A HAV - INTERNATION						-0		-	110
IEN(on) IA(on)	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub>		V <sub>A</sub> = 2.4	4V or 0V	0.01		±1.0	-30	-0"	-100	-30	
or  EN(off)  A(off)	or EN	9W0 1	(Miluo) VA = 15	SV or OV	0.01	Louis	±1.0	30 =0	0030 888	10	30	μА
DYNAMIC		allering grow	and the same of th					Linger	9.01			
transition	D		See F	igure 3	0.3		1	6	6 6			
topen	Do M			igure 4	0.2		रधकार व	SAMBINE	7 FA 19	3/4		
ton(EN)	DV E			igure 5	0.6	3-7	1.5	STUNKI ZE	SPIGGA YE	AWIR BIRL	18	μs
toff(EN)	D				0.4	WO day	regregar la	WS CHANN	OHE BUOM	KKB BVD	BA	
t <sub>on</sub> -t <sub>off</sub> Break- Before-Make Delay Settling Time	D <sub>isc</sub> (or	8	V <sub>EN</sub> = +5V, A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> Strobed V <sub>IN</sub> = ±10V, Figure 6		10	1000000 11181	Diag	lanoito	l: Fan	อามเ	PRI	
"OFF" Isolation	D	in Co		C <sub>L</sub> = 3pF, V <sub>S</sub> = 3 VRMS, 00kHz	60				THE RES			dB
C <sub>s(off)</sub>	S	and president	V <sub>S</sub> = 0	V <sub>EN</sub> = 0V,	5		the car proper					
C <sub>D(off)</sub>	D		V <sub>D</sub> = 0	f = 140kHz	25							pF
C <sub>DS(off)</sub>	D to S		$V_S = 0, V_D = 0$	to 1 MHz	1	13.150					HE K	

		NO	CTMOST	STILL THE STIMES MAX LIMITS THE STATE OF							
	MEASURED	TESTS	TEST CONDITIONS	TYP	M SUFFIX			C SUFFIX			UNIT
	TERMINAL PER TEMP			25°C	-55°C	25°C	125°C	-20°C/ 0°C	25°C	85°C/ 70°C	
SUPPLY						(A.  41)		e I oA			Tallet.
Supply	1+	7:00	V <sub>EN</sub> = 5V	0.5	0.7	0.6	0.5	[2] V8 o	1.0		
Current	1-	1	All V <sub>ADD</sub> = 0V/5V	0.02	0.7	0.6	0.5	E Ver-	1.0	ALC: N	mA

Note 1. Readings taken 400ms after the overvoltage occurs.

#### SWITCHING TIME TEST CIRCUITS

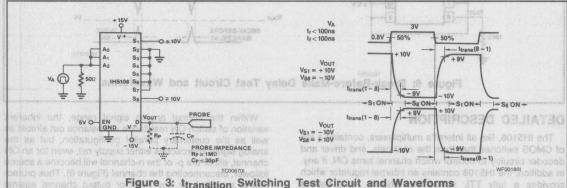


Figure 3: t<sub>transition</sub> Switching

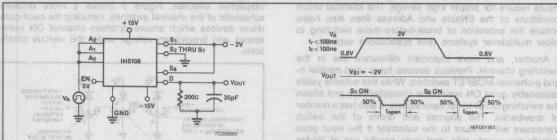
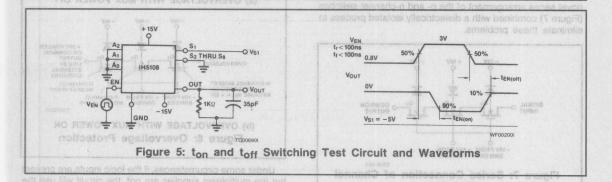
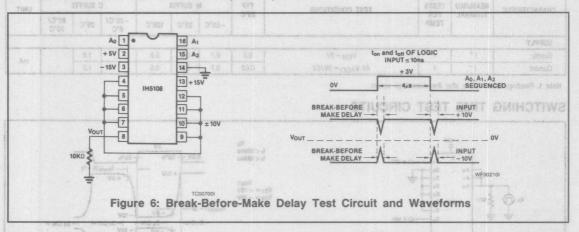


Figure 4: topen (Break-Before-Make) Switching Test Circuit and Waveforms



3-101

#### SWITCHING TIME TEST CIRCUITS (CONT.)



#### **DETAILED DESCRIPTION**

The IH5108, like all Intersil's multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n-and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with a dielectrically isolated process to eliminate these problems.

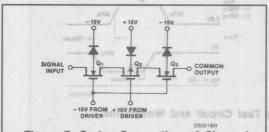
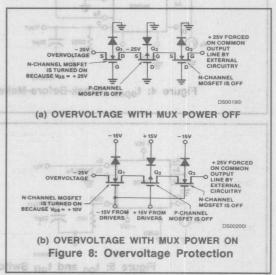


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from

3

#### **DETAILED DESCRIPTION (CONT.)**

occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

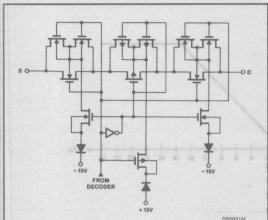
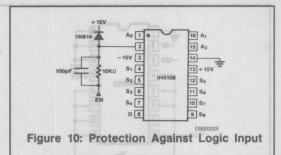


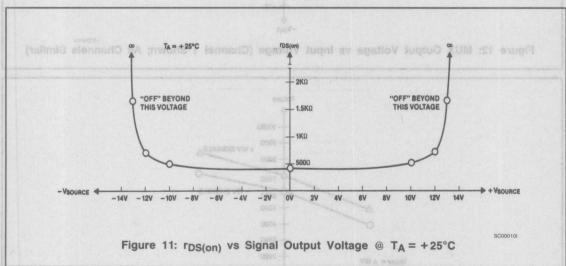
Figure 9: Detailed Channel Switch Schematic

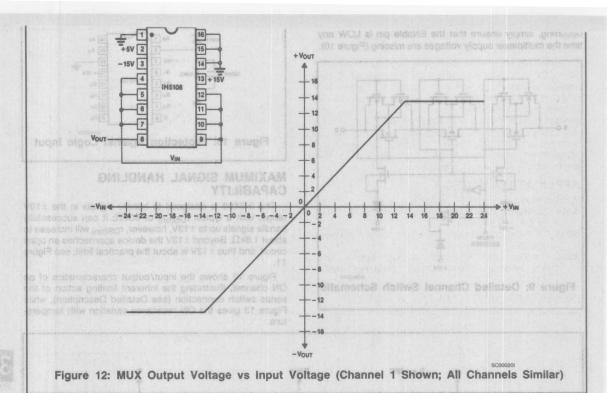


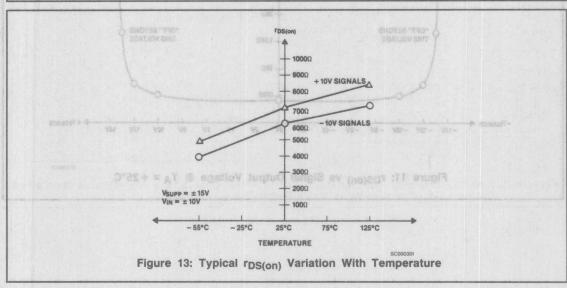
## MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the  $\pm 10V$  range, with a typical  $r_{DS(on)}$  of  $600\Omega$ ; it can successfully handle signals up to  $\pm 13V$ , however,  $r_{DS(on)}$  will increase to about  $1.8k\Omega$ . Beyond  $\pm 13V$  the device approaches an open circuit, and thus  $\pm 12V$  is about the practical limit, see Figure 11

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.







## USING THE IH5108 WITH SUPPLIES OTHER THAN $\pm 15 \text{V}$

The IH5108 will operate successfully with supply voltages from  $\pm 5V$  to  $\pm 15V$ , however  $r_{DS(on)}$  increases as supply voltage decreases, as shown in Figure 14. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of  $r_{DS(on)}$  and leakage current remains reasonably constant.  $r_{DS(on)}$  also decreases as signal levels decrease. For high system accuracy [acceptable levels of  $r_{DS(on)}$ ] the maximum input signal should be 3V less than the supply voltages. The logic levels remain TTL compatible.

#### **APPLICATION NOTES**

Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliener

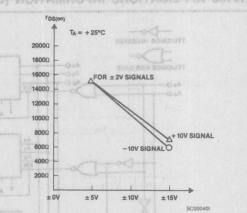
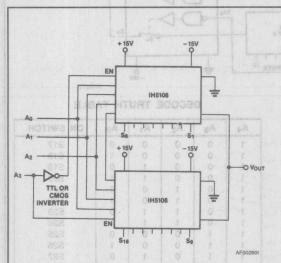


Figure 14: Typical r<sub>DS(on)</sub> Variation With Supply Voltages

#### **IH5108 APPLICATIONS INFORMATION**



#### DECODE TRUTH TABLE

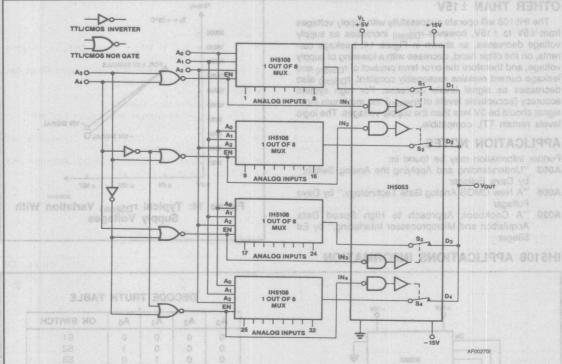
A3	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON	SWITC	Н
0	0	0	0	PK 5	S1	11.2
0	0	0	1		S2	
0	0	1	0	1	S3	
0	0	工 村田	E FER	CODE	S4	
0	1	0	0	-	S5	
0	1901	0.0	11	SA.	S6	
0	1	1	0	0	S7	
0	1	1	1	0	S8	
1:2	0	0	0	0	S9	
1a	0	0	1	0	S10	
1a	0	01	0	1	S11	
188	0	1	.01	1	S12	
18	1	0	0	1	S13	
18	1	10	11	1	S14	
18	1	01	0	0	S15	
98	1	1	01	0	S16	. 0

Figure 15: 1 of 16 Channel Multiplexer Using Two IH5108s. Overvoltage Protection Is Maintained Between All Channels, As Is Break-Before-Make Switching.

igure 16:1 Of 32 Multiplexer Using 4 IHS108s and An IHS053 As A Submultiplexer. Note That The IHS083 Is Protected Against Overvoltages By The IHS108s. Submultiplexing Reduces

IH5108

#### **IH5108 APPLICATIONS INFORMATION (CONT.)**



#### DECODE TRUTH TABLE

A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON	SWITCH
0	0	0	0	0		S1
0	0	0	0	1		S2
0	0	0	9	0		S3
0	0	0	11	91		S2 S3 S4
0	0	1	0	0		S5
0	0	-1	0	1		S6
0	0	1	01	0		S7
0	0.3	1	11	01		S8
0	- ata :	0	0	0		S9
0	atra	0	0	1		S10
0	1	0	1	0		S11
0	1	0	1	1		S12
0	mints a	el Anii	0	0		S13
0	1	1	0	1 m		S14
0	1	11	1	0		S15
0	1	1	1	1		S16

#### DECODE TRUTH TABLE

A <sub>4</sub>	A3	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	21	S18
0° c1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1 0	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1/2	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
nidi.	no him	0	nosta.	o br	S28
1	1	inter	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 16: 1 Of 32 Multiplexer Using 4 IH5108s and An IH5053 As A Submultiplexer. Note That The IH5053 Is Protected Against Overvoltages By The IH5108s. Submultiplexing Reduces Output Leakage and Capacitance.

3

# 16-Channel Fault Protected NAR CMOS Analog Multiple

#### GENERAL DESCRIPTION

The IH5116 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI506A and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5116MJI	-55°C to +125°C	28 pin CERDIP
IH5116CJI	0°C to +70°C	28 pin CERDIP
IH5116CPI	0°C to +70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH5116MDI/CDI)

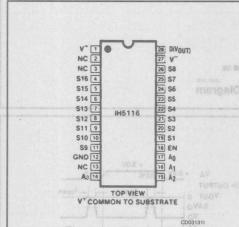


Figure 1: Pin Configuration (Outline dwg JE, PE)

#### **FEATURES**

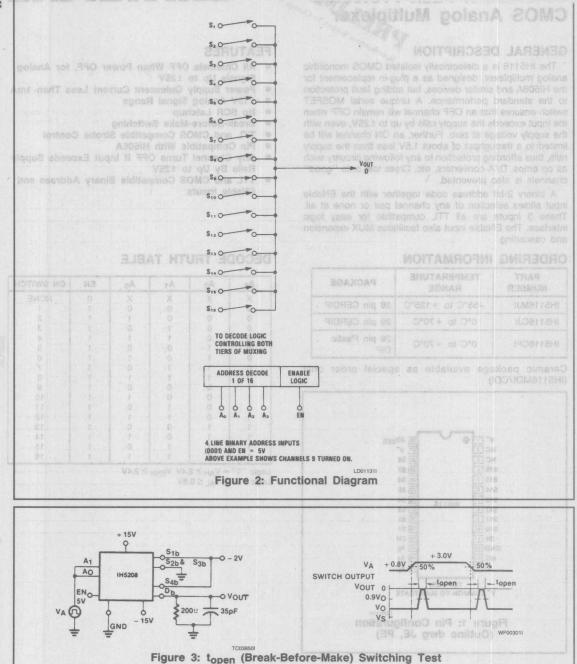
- All Channels OFF When Power OFF, for Analog Signals Up to ±25V
- Power Supply Quiescent Current Less Than 1mA
- ±13V Analog Signal Range
- No SCR Latchup
- **Break-Before-Make Switching**
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI506A
- Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V
- TTL and CMOS Compatible Binary Address and **ENable Inputs**

#### **DECODE TRUTH TABLE**

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	X	0	NONE
0	0.0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
0 1 6	0 0	1	0	1	11
the of the	0	1	1	1	12
1	1	0	0	1	13
1	1 .	0	1	1	14
NO. 2 THE CO.	A COST	1	0	- 1	15
coie Monax	resort.	1	1	1	16

Logic "1" = V<sub>AH</sub> ≥ 2.4V V<sub>ENH</sub> ≥ 2.4V Logic "0" = V<sub>AL</sub> ≤ 0.8V

Figure 3: totale (Break-Before-Make) Switching Test



#### IH5116

#### **ABSOLUTE MAXIMUM RATINGS**

V <sub>IN</sub> (A, EN) to Ground15V to +15V
Vs or Vp to V <sup>+</sup> +25V to -40V
Vs or VD to V <sup>-</sup> 25V to +40V
V <sup>+</sup> to Ground
V <sup>-</sup> to Ground16V

Current (Any Terminal)
Operating Temperature
Storage Temperature65 to +150°C
Lead Temperature (Soldering, 10sec)300°C
Power Dissipation*1200mW
*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS** (V<sup>+</sup> = 15V, V<sup>-</sup> = -15V, V<sub>EN</sub> = 2.4V, unless otherwise specified.)

	Assets a	NO	sider Than 1889iz	marih e		MAX LIMITS						1110
CHARACTERISTIC	MEASURED TERMINAL	TESTS	TEST CONDITIONS		TYP 25°C		SUFFI	X	C SUFFIX			UNIT
		TEMP			25 0	-55°C	25°C	125°C	0°C	25°C	70°C	AND NA
SWITCH	Agmica	портись.	CHIUS IMPECT C	es e til	olveb e	asrit ae	olarn ri	ge which	nen And	If adi	s are in	Inemu
RDS(on)	S to D	16	V <sub>D</sub> = 10V, I <sub>S</sub> = -1.0mA	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Isel
		16	$V_D = -10V$ $I_S = -1.0 \text{mA}$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V	500	1000	1000	1500	1200	1200	1800	Ω (V3
			R <sub>DS</sub> (	on)max-RDS(on)min	5	naj terras	Assessment	is all a	II S IIS II	viime	1.0617	%
ΔR <sub>DS</sub> (on)			$\Delta R_{DS(on)} = \frac{S_{VS}}{V_{S}} = \frac{S_{VS}}{V_{S}}$	RDS(on)avg. ±10V	5	Managa San			runta or	Yamana	Chart	emen
IS(off)	S	16	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V		0.02		±0.5	50		±1.0	50	
		16	V <sub>S</sub> = -10V, V <sub>D</sub> = 10V		0.02		±0.5	50	MALE CO.	±1.0	50	ORG
I <sub>D(off)</sub>	D	1	$V_D = 10V, V_S = -10V$	V <sub>EN</sub> = 0.8V	0.05	HEAT	±1.0	100	not	±2.0	100	O .
	200	1	$V_D = -10V, V_S = 10V$		0.05	TYPE	±1.0	100	20	±2.0	100	nA
ID(on)	D	16	V <sub>S(AII)</sub> = V <sub>D</sub> = 10V	Sequence each switch on	0.1	01 0°0 0°C (6	±2.0	100	118	±4.0	100	95140 95140
		16	$V_{S(AII)} = V_D = -10V$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V	0.1	0 86-1 0 66-1	±2.0	100	8)- 12	±4.0	100	48140
FAULT		Lien			0101	01 014		HILIPISIU IN	871 18	46 1500	300	INE
Is with Power OFF	S	16	$V_{SUPP} = 0V, V_{IN} = \pm 25V, V_{EN} = V_O = 0V, A_0, A_1, A_2 = 0V \text{ or } 5V$		1.0	0°08- d 5°01	2.0	Fin Fint Pai	ST 14	5.0	OPI With	μΑ
Is(off) with Overvoltage	S	16	$V_{IN} = \pm 25V$ , $V_0 = \pm 10V$		1.0	0.48	2.0	(00) Pin OERDH	31 18	5.0	Will	μΑ
INPUT						01 271		NURBU III		17092	30	) SETU
IEN(on) IA(on)	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub>	4	V <sub>A</sub> = 2.4	V or 0V	0.01	0/88-1 N 0'0 IX	-10	-30	LI FOT	-10	-30	SATE
or  EN(off)  A(off)	or EN	4	V <sub>A</sub> =	15V	0.01	3733-1	10	30	OT	10	30	μА
DYNAMIC					CHOICE AND	D 400 -		THE CHARGE	27	1000 to 17	300	20101
ttransition	D	110	The second		0.3	at 0*0	190	Pic Plantic	at 10	Dust St	340	25143
topen	D	THE STATE OF THE S	0735		0.2	7.65	A.		21	AS PROP	QH)	8×164
ton(EN)	D		ELECYTHICA		0.6	2702 E	1.5	(KDRSD IV)	25	15001	SHA	μs
toff(EN)	D				0.4	or 310	100	Par Parence	200	TERE	300	Large
ton-toff Break- Before-Make	D	16	V <sub>EN</sub> = +5V, A <sub>0</sub> , V <sub>IN</sub> =	A <sub>1</sub> , A <sub>2</sub> Strobed ±10V.	25	0100 lb	**	So Fint Pu	Mr ST	1890	WIT	ns
Delay Settling Time	Tmare	siO is	re 1: Function	mora -		24.50	-	DIFFICIENT AND	OIL TO	TERGI	Wik	15144
"OFF" Isolation	D	11 - 0	V <sub>EN</sub> = 0, R <sub>L</sub> = 2 V <sub>S</sub> = 3VRMS	$000\Omega$ , $C_L = 3pF$ , $f = 500kHz$	60	65 070 m 65 079	910	Pin CERDA Pin Plastic	81 18	G IsuC	300	dB
C <sub>s(off)</sub>	S		V <sub>S</sub> = 0	V <sub>EN</sub> = 0V,	5	2 96-1	- 2	BH JEST MIT	4F) T8	O BUCK	0.35	62/45
C <sub>D(off)</sub>	D	THE STATE OF	$V_D = 0$	f = 140kHz	25	120 E	00 (0)0,0	SAN OFIE	solveti (se	10 obia)	Notes of	pF
C <sub>DS(off)</sub>	D to S		$V_S = 0, \ V_D = 0$	to 1 MHz	1				000 0100	Spirit W		1
Supply +	1+	1	All V <sub>A</sub> =	= 0V/5V	0.5		0.6	-		1.0		
Current -	1-	1	VEN		0.02		0.6	-	-	1.0		mA

## IH5140-IH5145 Family

## High-Level **CMOS Analog Switch**

#### GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with super fast ton times (80ns typical) and faster toff times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 200pA at 25°C. Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1 µA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Intersil's IH5040 family and part of the DG180/190 family as shown in the switching state diagrams.



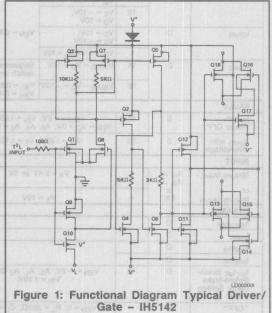
#### **FEATURES**

- Super Fast Break-Before-Make Switching
- ton 80ns Typ, toff 50ns Typ (SPST Switches)
- Power Supply Currents Less Than 1µA
- OFF Leakages Less Than 100pA @ 25°C Guaranteed
- Non-latching With Supply Turn-off
- Single Monolithic CMOS Chip
- Plug-in Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and
- Greater Than 1MHz Toggle Rate
- Switches Greater Than 20Vp-p Signals With ±15V Supplies
- TTL, CMOS Direct Compatibility

#### ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

1. Ceramic (side braze) devices also available; consult factory. 2. MIL temp range parts also available with MIL-STD-883 processing.



### IH5140-IH5145

## **BINITERSIL**

#### **ABSOLUTE MAXIMUM RATINGS**

V <sup>+</sup> - V <sup>-</sup>	< 33V
V + - V <sub>D</sub>	< 30V
VD - V	
VD - VS	±22V
V <sub>1</sub> - V <sup>2</sup>	< 33V
V <sub>I</sub> - V <sub>IN</sub>	< 30V
VL – V <sub>IN</sub>	< 20V
V <sub>IN</sub>	

Current (Any Terminal)	< 30mA
Storage Temperature65°C to	+150°C
Operating Temperature55°C to	+125°C
Lead Temperature (Soldering 10sec)	300°C
Power Dissipation	.450mW
(All Leads Soldered to a P.C. Board)	
Derate 6 mW/°C Above 70°C	0 8

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS (@ 25°C, V+ = +15V, V- = -15V, V<sub>I</sub> = +5V)

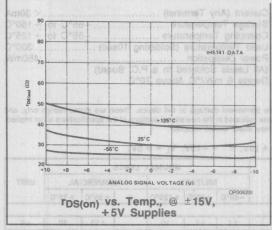
PER CHANNEL			MIN/MAX LIMITS							
		TEST CONDITIONS		MILITARY			OMMERC	IAL	UNIT	
SYMBOL	CHARACTERISTIC	1 12201		+25°C	+ 125°C	0	+25°C	+70°C	100	
LOGIC INPUT	[				anticio	W Sun	28 -4- (170-)			
INH	Input Logic Current	V <sub>IN</sub> = 2.4V Note 1	±1	±1	10		±10	10	μΑ	
INL	Input Logic Current	V <sub>IN</sub> = 0.8V Note 1	±1 -	±1	10		±10	10	μА	
SWITCH	essium en la	COLUMN TO SERVICE PROPERTY OF								
rDS(on)	Drain-Source On Resistance	Is = -10mA VANALOG = -10V to +10V	50	50	75	75	75	100	Ω	
Δr <sub>DS</sub> (on)	Channel to Channel rDS(on) Match	100		25 (typ)	SILJINIUS VIII	10:1	30 (typ)		Ω	
VANALOG	Min. Analog Signal Handling Capability	1/1: 8	9783-	±11 (typ)	No.		±10 (typ)		٧	
I <sub>D(off)</sub> + I <sub>S(off)</sub>	Switch OFF Leakage Current	$V_D = +10V, V_S = -10V$ $V_D = -10V, V_S = +10V$		±.5 ±.5	100 100		±5 ±5	100 100	nA	
ID(on) + IS(on)	Switch On Leakage Current	$V_D = V_S = -10V \text{ to } +10V$		±1	200		±2	200	nA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches See Performance Characteristics		54 (typ)	Si Jerri S. Vici cantifica e e e e	Mary .	50 (typ)		dE	
t <sub>on</sub>	Switch "ON" Time Switch "OFF" Time	See switching time specifications ar	nd timing d	liagrams.	1 10 to 10 t	ANDIS SOL	F- 31	di i		
Q <sub>(INJ.)</sub>	Charge Injection	See Performance Characteristics	1 ESSARO	10 (typ)	108 TO	void .	15 (typ)	503	pC	
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$ , $R_L = 100\Omega$ , $C_L \le 5pF$ See Performance Characteristics		54 (typ)			50 (typ)	10.00	dB	
SUPPLY		THE RESERVE OF THE PARTY OF THE							102	
utara a per	+ Power Supply Quiescent Current	Thurst T	1.0	1.0	10.0	10	10	100	μΑ	
ı -	- Power Supply Quiescent Current	$V^{+} = +15V, V^{-} = -15V, V_{L} = +5V$	1.0	1.0	10.0	10	10	100	μΑ	
IL	+5V Supply Quiescent Current	See Performance Characteristics	1.0	1.0	10.0	10	10	100	μΑ	
IGND	Gnd Supply Quiescent Current	+	1.0	1.0	10.0	10	10	100	μΑ	

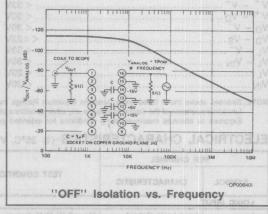
NOTES: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.

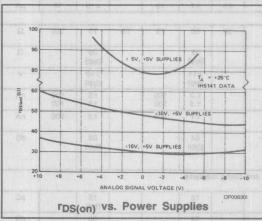
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

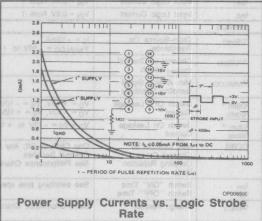
Channel to Channel Cross Coupling Rejection vs. Frequency

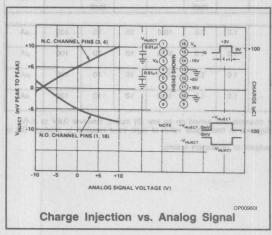
Charge Injection vs. Analog Signal

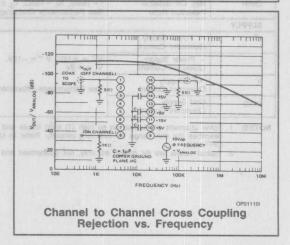












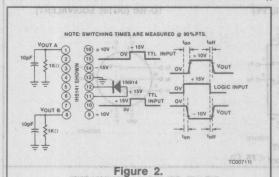
#### SWITCHING TIME SPECIFICATIONS

(ton, toff are maximum specifications and ton-toff is minimum specifications)

			TEST		MILITARY		C	OMMERCIA	\L	
PART NUMBER	SYMBOL	CHARACTERISTIC	CONDITIONS		+ 25°C	+ 125°C	0	+ 25°C	+70°C	UNI
	ton	Switch "ON" time		Ren	100	227		150		
	toff	Switch "OFF" time	Figure 2		75		M	125		ns
IH5140-	ton-toff	Break-before-make			10			5		
5141	ton toff ton-toff	Switch "ON" time Switch "OFF" time Break-before-make	Figure 3		150 125 *10 (typ)	×-0-	er com	175 150 5		ns
IH5142-	ton toff ton-toff	Switch "ON" time Switch 'OFF" time Break-before-make	Figure 2*		175 125 10	dro		250 150 5		ns
	ton toff ton-toff	Switch "ON" time Switch "OFF" time Break-before-make	Figure 3	MSTAI	200 125 *10 (typ)			300 150 5		ns
5143	ton	Switch "ON" time Switch "OFF" time	Figure 4		175 125		(2-03)	250 150		ns
	ton-toff	Break-before-make			10			5		
	ton	Switch "ON" time	11 317		200	B. B. J.		300		100
	toff	Switch "OFF" time	Figure 5		125		ST STORY	150		ns
	ton-toff	Break-before-make	1 500		10		1-0	5		
	ton de	Switch "ON" time	2000	(0) (0)	175			250	W.	
	toff	Switch "OFF" time	Figure 2		125		124000	150		ns
IH5144-	ton-toff	Break-before-make	4		10		THE STREET	5		
5145.	ton toff ton-toff	Switch "ON" time Switch "OFF" time Break-before-make	Figure 3		200 125 *10	1877.0	500	300 150 5		ns

NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS.

\* Typical values for design aid only, not guaranteed nor subject to production testing.

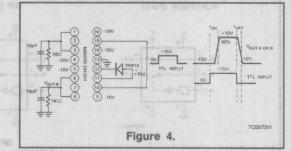


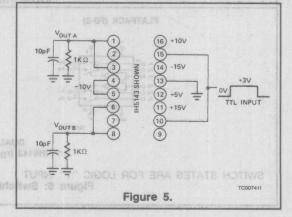
10pF 1K:12 (3) (16) -15V -3V TTL INPUT

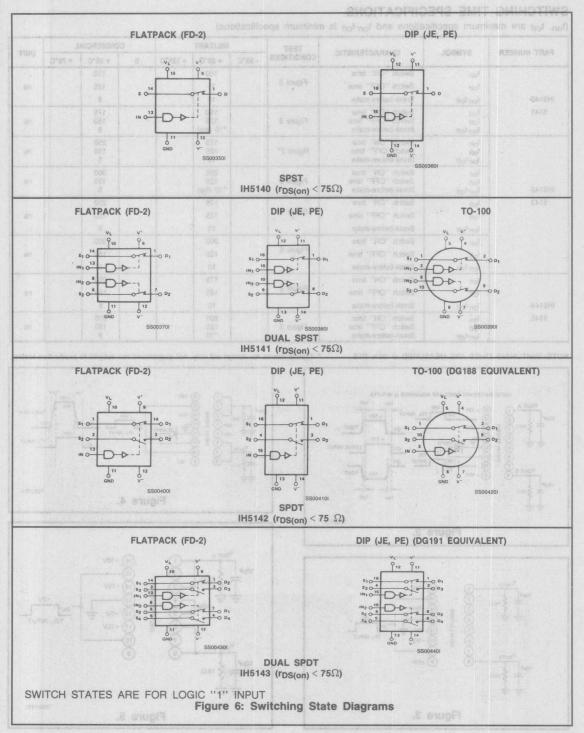
Vouts (8) 12 +5V = 0 TTL INPUT

Vouts (8) 2 110V

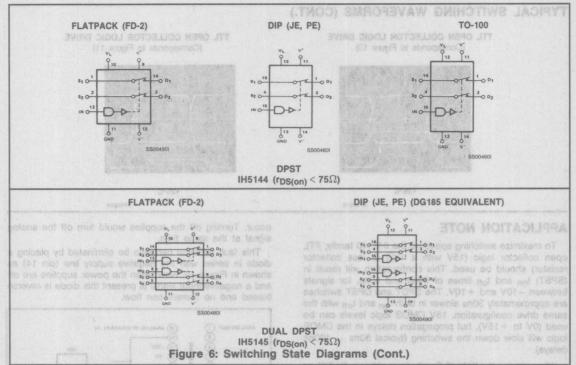
Figure 3.









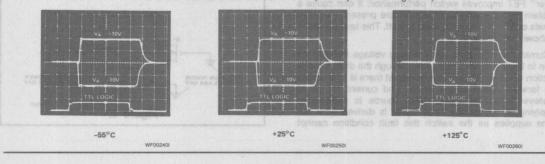


#### TYPICAL SWITCHING WAVEFORMS SCALE: VERT. = 5V/DIV. HORIZ. = 100ns/DIV.

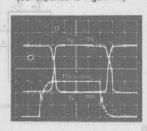
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



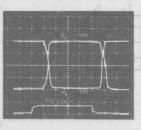




#### TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 10)



## (Corresponds to Figure 11)



+25°C

+25°C

(SAS) 3(2ASTA WF00280)

#### **APPLICATION NOTE**

To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1k $\Omega$  or less collector resistor) should be used. This configuration will result in (SPST)  $t_{OR}$  and  $t_{Off}$  times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both  $t_{OR}$  with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns  $\rightarrow$  100ns delays).

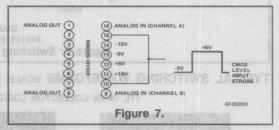
When driving the IH5140 Family from either  $\pm 5V$  TTL or CMOS logic, switching times run 20ns slower than if they were driven from  $\pm 15V$  logic levels. Thus  $t_{OR}$  is about 105ns, and  $t_{OR}$  75ns for SPST switches, and 135ns and 105ns ( $t_{OR}$ ,  $t_{OR}$ ) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if  $\pm 5V$  strobe levels are used instead of the usual  $0V \rightarrow \pm 3.0V$  drive. Pin 13 is taken to  $\pm 5V$  instead of the usual GND and strobe input is taken from  $\pm 5V$  to  $\pm 5V$  levels as shown in Figure 7.

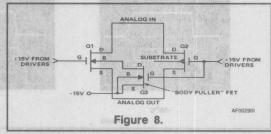
The typical channel of the IH5140 family consists of both P and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to -15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 8). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant RDS(ON) with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 9.

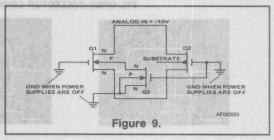
Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot

occur. Turning off the supplies would turn off the analog signal at the same time.

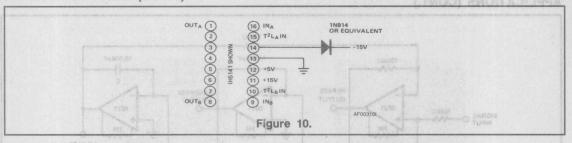
This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 10. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.







#### APPLICATION NOTE (CONT.)



#### **APPLICATIONS**

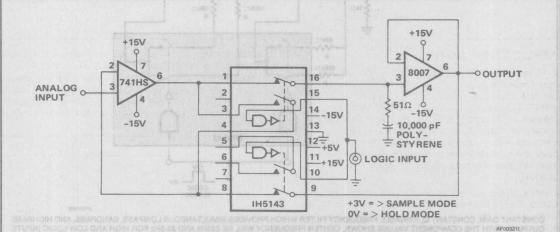


Figure 11: Improved Sample and Hold Using IH5143

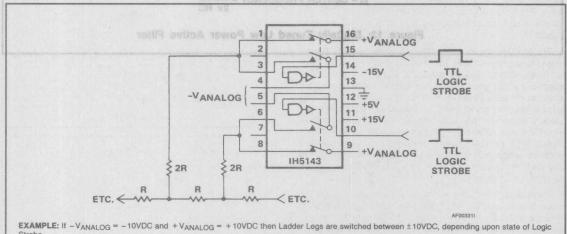
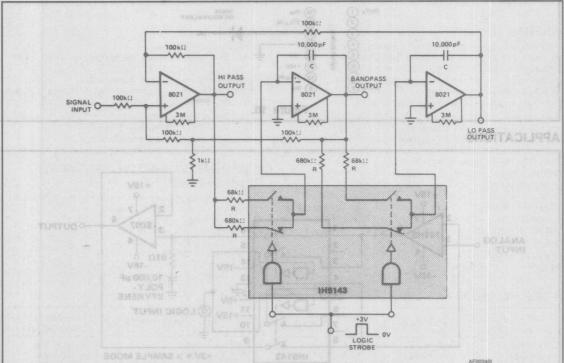


Figure 12: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

#### IH5140-IH5145

## **BINTERSIL**

#### **APPLICATIONS (CONT.)**



CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

 $f_n = CENTER FREQUENCY = \frac{1}{2\pi RC}$ 

Figure 13: Digitally Tuned Low Power Active Filter

## IH5148-IH5151 **High-Level CMOS Analog Switches**

#### GENERAL DESCRIPTION

The IH5148 family of solid state analog switches are designed using an improved, high voltage CMOS technology. Destructive latchup has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present; the IH5148 CMOS technology has eliminated this problem.

Key performance advantages of the 5148 series are TTL compatibility and ultra low-power operation. RDS(on) Switch resistance is typically in the  $14\Omega$  To  $18\Omega$  Area, for Signals in the -10V to +10V range. Quiescent current is less than 10μA. The 5148 also guarantees Break-Before-Make switching which is logically accomplished by extending the ton time (200nsec typ.) such that it exceeds toff time 120nsec typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Many of the devices in the 5148 series are pin-for-pin compatible with other analog switches, and offer improved electrical characteristics.



#### FEATURES

- Low Rps(ON) 25Ω
- Switches Greater Than 20Vpp Signals With ±15V
- Quiescent Current Less Than 100µA
- Break-Before-Make Switching toff 120nsec, Typ. ton 200nsec Typical on betalf ecody eved assessib 2170M
- TTL, CMOS Compatible above all to not
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- ±5V to ±15V Supply Range

#### CMOS ANALOG SWITCH PRODUCT CONDITIONING

- The Following Processes Are Performed 100% in Accordance With MIL-STD-883
- Precap Visual Method 2010, Cond. B
- Stabilization Bake Method 1008 Temperature Cycle Method 1010
- Centrifuge Method 2001, Cond. E
- Hermeticity Method 1014, Cond. A, C
- (Leak Rate < 5 x 10<sup>-7</sup> atm cc/s)

#### ORDERING INFORMATION

ORDER PART NUMBER	FUNCTION	PACKAGE	TEMPERATURE RANGE	HARRIS EQUIVALENT
IH5148MJE IH5148CJE IH5148CPE IH5148MFD IH5148CTW IH5148MTW	Dual SPST	16 Pin CERDIP 16 Pin CERDIP 16 Pin Plastic DIP 14 Pin Flat Pack TO-100 TO-100	-55°C to 125°C 0°C to 70°C 0°C to 70°C -50°C to 125°C 0°C to 70°C -55°C to 125°C	HI-5048 HI-5048 HI-5048 HI-5048 HI-5048 HI-5048
IH5149MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C	HI-5049
IH5149CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C	HI-5049
IH5149CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C	HI-5049
IH5149MFD	Dual DPST	14 Pin Flat Pack	-50°C to 125°C	HI-5049
IH5150MJE	SPDT	16 Pin CERDIP	-55°C to 125°C 0°C to 70°C 0°C to 70°C -50°C to 125°C 0°C to 70°C -55°C to 125°C	HI-5050
IH5150CJE	SPDT	16 Pin CERDIP		HI-5050
IH5150CPE	SPDT	16 Pin Plastic DIP		HI-5050
IH5150MFD	SPDT	14 Pin Flat Pack		HI-5050
IH5150CTW	SPDT	TO-100		HI-5050
IH5150MTW	SPDT	TO-100		HI-5050
IH5151MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C	HI-5051
IH5151CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C	HI-5051
IH5151CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C	HI-5051
IH5151MFD	Dual SPDT	14 Pin Flat Pack	-50°C to 125°C	HI-5051

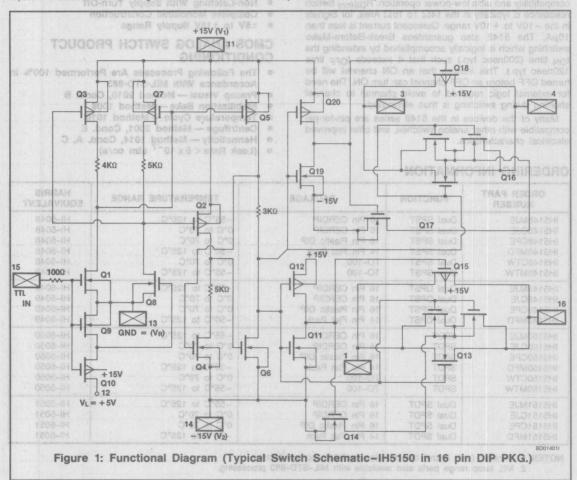
NOTES: 1. Ceramic (side braze) devices also available; consult factory.

2. MIL temp range parts also available with MIL-STD-883 processing.

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V <sup>+</sup> . V <sup>-</sup>	Current (Any Terminal) < 50mA
V <sup>+</sup> , V <sub>D</sub> <30V	Storage Temperature65°C to +150°C
V <sub>D</sub> , V <sup>-</sup> <30V	Operating Temperature55°C to +125°C
V <sub>D</sub> , V <sub>S</sub> < ±22V	Lead Temperature (Soldering, 10sec)300°C
VL, V <sup>2</sup> < 33V VL, V <sub>IN</sub> < 30V	Power Dissipation450mW
V <sub>L</sub> , V <sub>IN</sub> < 30V	(All Leads Soldered to a P.C. Board)
V <sub>L</sub> < 20V	Derate 6mW/°C Above 70°C
V <sub>L</sub>	switches were destroyed when power supplies were re-

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



PER	CHANNEL	DIP (DE) PADICAGE	MIN/MAX LIMITS						11
		TEST CONDITIONS		MILITARY	,	- (	UNIT		
SYMBOL CHARACTERISTIC		- 55°C	+ 25°C	+ 125°C	0	+ 25°C	+ 70°C	10	
IN(ON)	Input Logic Current	V <sub>IN</sub> = 2.4V (Note 1)	±1	±1	# ±10		±1	±10	μΑ
IN(OFF)	Input Logic Current	V <sub>IN</sub> = 0.8V (Note 1)	±1	±1	±10		±1	±10	μΑ
RDS(ON)	Drain-Source On Resistance	$V_D = \pm 10V$ , $I_S = -10mA$	25	25	50		30		Ω
ΔR <sub>DS</sub> (ON)	Channel to Channel RDS(ON) Match	r-sO-For		10 (Typ)	Q0-120 M		15 (Typ)		Ω
VANALOG	Min. Analog Signal Handling Capability	10-12-0-10-2	20-	±14 (Typ)	enterest 10		±14 (Typ)		V
ID(OFF) IS(OFF)	Switch OFF Leakage Current	V <sub>ANALOG</sub> = -10V to +10V		±0.5	50		±1.0	100	nA
ID(ON) + IS(ON)	Switch On Leakage Current	V <sub>D</sub> = V <sub>S</sub> = -10V to +10V		±1.0	100		±2.0	100	nA
Q <sub>(INJ)</sub>	Charge Injection	See Figure 4		(10) (Typ)			(10) (Typ)	AL OPST	JØ mV
OIRR	Min. Off Isolation Rejection Ratio	I = 1MHz, R <sub>L</sub> = 100 $\Omega$ , C <sub>L</sub> $\leq$ 5pF See Figure 5		54 (Typ)	N 0		50 (Typ)		dB
SUPPLY		19 playouthor		Principle and	The second				
1+	+ Power Supply Quiescent Current	40 120 10 10 10 10 10 10 10 10 10 10 10 10 10	10	10	100		10		μА
1-	- Power Supply Quiescent Current	V <sub>1</sub> = + 15V, V <sub>2</sub> = -15V.	10	10	100		10		μΑ
IL.	+ 5V Supply Quiescent Current	$V_L = +5V, V_R = 0$	10	10	100		10		μА
IGND	Gnd Supply Quiescent Current	0 0	10 1097	10	100		10		μΑ
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Figure 8		54 (Typ)			50	ні таяа	dB

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minrange for switching properly. Refer to logic diagrams to find logical value of logic input required to produce "ON" or "OFF" state.

## SWITCHING TIME SPECIFICATION IH5148 SPST SWITCH

SYMBOL	PARAMETER	TEST CONDITIONS MIN	MAX	UNIT
ton	Switch "on" time	$R_L = 1K\Omega$ , $V_{ANALOG} = -10V$	250	ns
toff	Switch "off" time	T <sub>O</sub> + 10V; See Figures 3 and 6	200	ns

#### **IH5149 DPST SWITCH**

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
ton	Switch "on" time		$R_L = 1K\Omega$ , $V_{ANALOG} = -10V$		350	ns
toff	Switch "off" time	9 49	T <sub>O</sub> +10V; See Figures 3 and 6	and the least	250	ns

#### IH5150 & IH5151 SPDT SWITCH

SYMBOL	PARAMETER	44-0	TEST CONDITIONS	MIN	MAX	UNIT
ton	Switch "on" time	v3-(	$R_L = 1K\Omega$ , $V_{ANALOG} = -10V$		500	ns
toff	Switch "off" time	0	To +10V; See Figures 3 and 6	A	250	ns

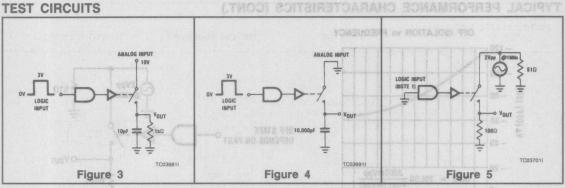
NOTE 2: For IH5150 & IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 & 4 on 5150, & Pins 3 & 4, 5 & 6 on 5151) have slower ton time, than channels on Pins 1, 16, & 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

### IH5148-IH5151

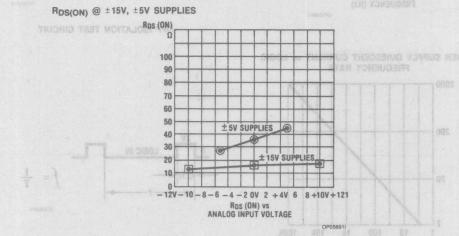


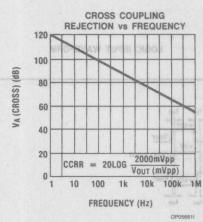
LOGIC "1" INPUT FLAT PACK		PACKA	DIP (DE) PACKAGE			(TW) PACKAGE					
DU	AL SPST	IH5148	0	+ 125°C	1777 H	0°85 -	GMUITI	enos test	OFFERISTO	RAHO	JOSMYS
	011			01 ± VL		14.	V <sub>L</sub>	(10H) VAS = 10	1	· Jugar	040940
00				s <sub>1</sub> 0 14	10 10	1 001		(1 St. 9) V6.0 = m/	Instruct 96	1.	
		30		m1 0 13 0	-	38	\$1 0 16 M1 0 15	01 00	\$10 1 W10 3 0 D D	ole ,	-0 01 10 BUR
				W2 0 0	D-0-1		W2 010 OH	>1	1120 100 D	HADISO )	
				\$2 0	0/2	0 02	S2 0 8	0 02	\$2010	of of.	O 02
				09 cm	11 J12		Vol Ju	M DO JAMA	spanish 1 6	J' wa	
					0.1±	S00740I	GBD	V- SS007501		SS007	760I - Brond
	AL DPST	70013		3001	(01)			See From 4		trices O. I	naisone)
	AL DIST	98			(T)(D) 64		308 ≥ 4, 3				
36		(ayT)		VI.	N.		912	0	n Ratio		
			-	\$1 0 14 \$3 0 2 \$1 0 13	OTE	13001	\$1 0 16 \$3 0 4	OT 0 01			
					)-D	T	"10-10-	D. 1			
4				82 0 5 \$4 0	) Dora	5 0 02	\$102 0 10 \$2 0 5	012 002			
					11 12	10%	54 0	0 04		8 V8 +	
				680	V-		]13	14			
					SS	5007701	GAID	SS00780I	InemuO to		
ib	SPDT IH	5150			S4 (Typ)		190 S	Training Switches a Training Switches a Tigore 8		Channel Coupling	GCRB
	livrapidy V/L	and Vill One	name and	result 1/3 · VE	V*	uhamana	V <sub>L</sub>	Yn deled 7 del		ottafi.	
			ecubang i	of beniup 9	10 9	t to eulay	looigal by	b agat of te	P property Her	9.	
				810	ore	14 0 01	\$1 O	012 100,	8101	Long	2 01
		nterores en el consperio		\$20	- ale	3 O D <sub>2</sub>	82 C 4	3002	S2 O 10	20	0 02
	ment by consistency of		lated	m 0 <sup>13</sup>	) <del>-</del>	T CONT	15 DC	ETER	"03/DI	>: /	
				J.				14	emis "Ito"	J,	
				GNO		30117FT 06	GMO	, ·	emis no oc	y- SS00	8101
								SS008001	WITCH	9 159	is 149 Di
DU	AL SPDT		20134						PARAW		SYMBOL
				V <sub>I</sub>	a bru Vi		ν Ει = 1ΚΩ. V	v* Q 11	ch "on" line		
				S <sub>1</sub> O 14	10 9	100	S <sub>1</sub> O 16	200	3 T/12/20 11	PERMI	
THUL			14138	\$3 0 13 M1 0 13	200	1 0 03	53 0 4 m1 0 15	01000	DARAS IS		
80		501	and for the same	HI 2 0 8	) D = 1	7 0 02	W2 0 10	D: 1	and the state of the state of the state of		
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						SS00820I	ewo O	A. Quod si sitti .e.			

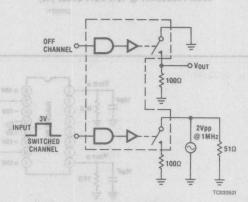
**TEST CIRCUITS** 



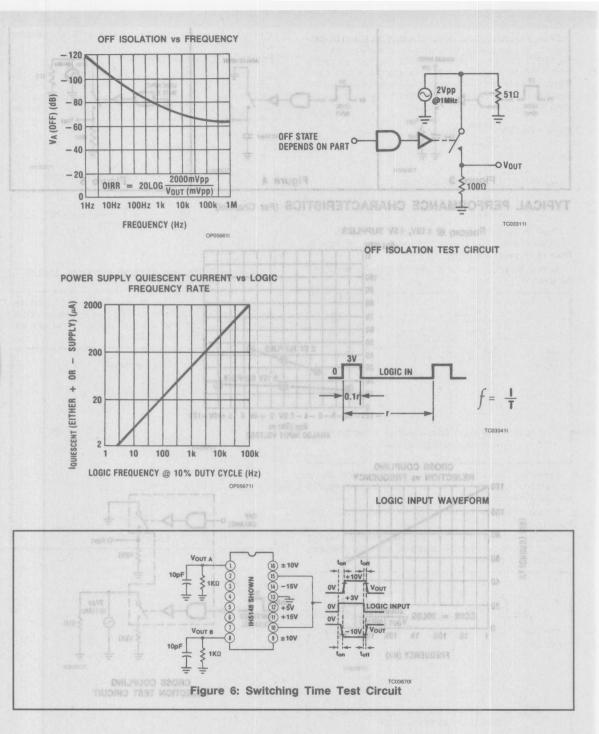
#### TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)







**CROSS COUPLING** HEONIX test emil premonwa : 8 ST REJECTION TEST CIRCUIT



#### Nulling Out Charge Injection:

Charge injection (Qinv. on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFET. The gates of these MOSFETs typically swing from -15V to +15V as a rapidly changing pulse; thus this 30Vpp pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$\mbox{Qinject (Vpp)} \cong \frac{\mbox{$C_{gate}$}}{\mbox{$C_{Load}$}} \, \mbox{$x$ 30V step.}$$

i.e.

$$C_{gate} = 1.5pF$$
,  $C_{Load} = 1000pF$ , then

$$Qinject(Vpp) = \frac{1.5pF}{1000pF} \times 30V \text{ step} = 45mVpp$$

Thus if you are using switch in a Sample & Hold application with C<sub>sample</sub> = 1000pF, a 45mVpp ''Sample to Hold error step'' will occur.

To null this error step out to zero the following circuit can be used:

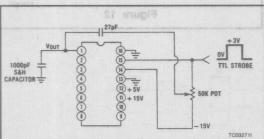
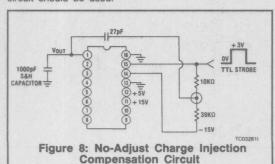


Figure 7: Adjustable Charge Injection Compensation Circuit

The circuit shown above nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until  $V_{OUT} = 0$ mVpp pulse, with  $V_{ANALOG} = 0$ V.

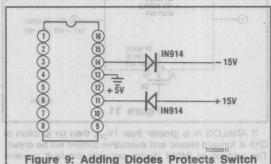
If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the following circuit should be used:



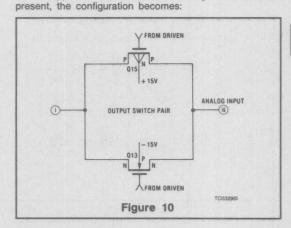
This configuration will produce a typical charge injection of  $V_{OUT} \le 10 mVpp$  into the 1000pF S & H capacitor shown.

#### **Fault Condition Protection**

If your system has analog voltage levels which are independent of the ±15V (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown below:



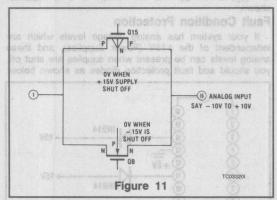
If the analog input levels are below ±15V, the pn junctions of Q13 & Q15 are reversed biased. However if the ±15V supplies are shut off and analog levels are still



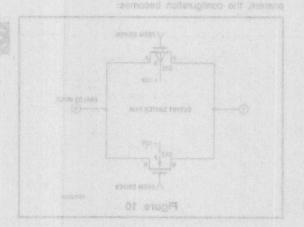
SIDES

#### IH5148-IH5151

The need for these diodes, in this circumstance, is shown below:



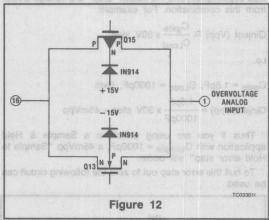
If ANALOG in is greater than 1V<sub>pn</sub>, then pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG in was less than or equal to -1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 & Q15 bodies.

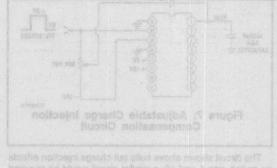




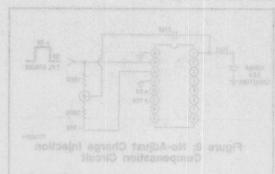
This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about ±18V ANALOG overvoltages. Beyond this drain(N) to P(body) breakdown VOLTAGE of Q13 limits overvoltage protection.





VANALOG = 0V
If you do not deene to do any adjusting, but wish the least
amount of charge intention possible, then the following
crout should be used:



3

### IH5208

## 4-Channel Differential Fault Protected CMOS Analog Multiplexer

#### GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI509A and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to  $\pm 25\mathrm{V}$ , even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5208MJE	-55°C to +125°C	16 pin CERDIP
IH5208IJE	-20°C to +85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP



#### **FEATURES**

- All Channels OFF When Power OFF, for Analog Signals Up to ±25V
- Power Supply Quiescent Current Less Than 1μA
- ±13V Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI-509A
- Any Channel Turns OFF If Input Exceeds Supply Rails by Up to ±25V
- TTL and CMOS Compatible Binary Address and ENable Inputs

#### DECODE TRUTH TABLE

A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	-	2a, 2b
04 V4 - 0V	1	1	3a, 3b 4a, 4b

A<sub>0</sub>, A<sub>1</sub>, EN Logic ''1'' = V<sub>AH</sub> ≥ 2.4V Logic ''0'' = V<sub>AL</sub> ≤ 0.8V

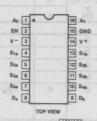
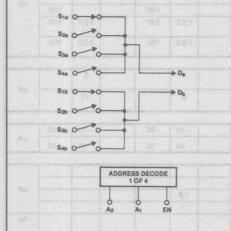


Figure 2: Pin Configuration (Outline dwg JE, PE)



2 LINE BINARY ADDRESS INPUTS (0 0) AND EN = 1 ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

Figure 1: Functional Diagram

#### ADSULUIE MAXIMUM RATINGS

VIN (A, EN) to Ground	_15V +15V	
Vs or VD to V+		
Vs or V <sub>D</sub> to V <sup>-</sup>		
V <sup>+</sup> to Ground		
V <sup>-</sup> to Ground	16V	
Current (Any Terminal)	20mA	

Operating Temperature55	to	125°C
Storage Temperature65		
Lead Temperature (Soldering, 10sec)		.300°C
Power Dissipation (Package)*	. 12	200mW

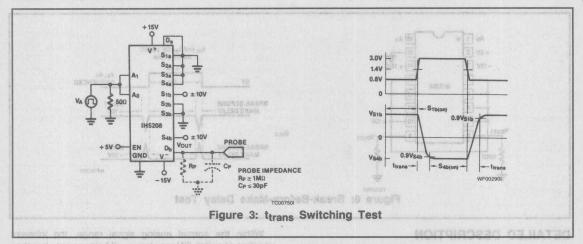
<sup>\*</sup>All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

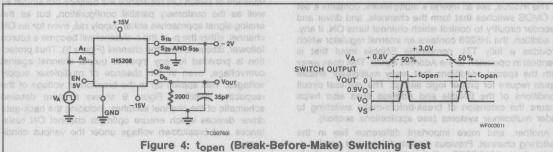
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V, V<sub>EN</sub> = 2.4V, unless otherwise specified.

SWITCH  rDS(on)  ArDS(on)  Is(off)  ID(off)  FAULT  Is with	S to D	TESTS PER TEMP 8	V <sub>D</sub> = 10V, I <sub>S</sub> = 1.0mA V <sub>D</sub> = -10V I <sub>S</sub> = -1.0mA	NDITIONS	700	-55°C	SUFFI 25°C	125°C	-20°C/ 0°C	SUFFI 25°C	85°C/ 70°C	UNI
SWITCH TDS(on)  ArDS(on)  Is(off)  ID(off)  FAULT Is with	S to D	TEMP 8	V <sub>D</sub> = 10V, I <sub>S</sub> = 1.0mA V <sub>D</sub> = -10V	Sequence each switch on	s ta en	86 101	25°C	125°C		25°C		
rDS(on)  ΔrDS(on)  IS(off)  ID(off)  FAULT Is with			$I_S = 1.0 \text{mA}$ $V_D = -10 \text{V}$	switch on	700	101 98	elditst	TOTAL	P. T. Table	Name and Address of the Owner, where the Owner, which is the Owner, where the Owner, which is the Owner, where the Owner, which is the Owner, w	-	
ΔrDS(on)  Is(off)  ID(off)  FAULT Is with			$I_S = 1.0 \text{mA}$ $V_D = -10 \text{V}$	switch on	700	4000		A THE STATE OF	# 4 SF2%	870 E	ugni E	986
ID(off)  ID(off)  FAULT Is with	S	8		VAL = 0.8V		1000	1000	1500	1200	1200	1800	Ω
ID(off)  ID(off)  FAULT Is with	S			$V_{AH} = 0.6V,$ $V_{AH} = 2.4V$	500	1000	1000	1500	1200	1200	1800	id.
ID(off) ID(on) FAULT Is with	S		$\Delta r_{DS(on)} = \frac{r_{DS(on)}}{}$	on)max <sup>-r</sup> DS(on)min rDS(on)avg.	5	PAGIG		RATURE	TEMPE	State	BIAUM	%
ID(off) ID(on) FAULT Is with	S		V <sub>S</sub> = :		PIORE	O nig 8	1 15	2014 /	s orde		LMBOS	15-31
FAULT Is with		8	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V		0.02	3 pin C	±0.5	50	-20°C	±1.0	50	H
FAULT Is with		8	$V_S = -10V$ , $V_D = 10V$		0.02	sig nig	±0.5	50	100	±1.0	50	HI
FAULT Is with	D	1	V <sub>D</sub> = 10V, V <sub>S</sub> = -10V	V <sub>D</sub> = 10V, V <sub>EN</sub> = 0.8V			±1.0	100		±2.0	100	
FAULT Is with	IBAT H	FM418	$V_D = -10V, V_S = 10V$		0.05	Feyndan 3		100			100	n/
FAULT Is with	40 D	8	V <sub>S(AII)</sub> = V <sub>D</sub> = 10V	Sequence each switch on	0.1	SHET	±2.0	100		±5.0	100	
Is with		8	$V_{S(AII)} = V_D = -10V$ $V_{AL} = 0.8V$ , $V_{AH} = 2.4V$		0.1		±2.0	100		±5.0	100	
Is with												
Power OFF	S	8	$V_{SUPP} = 0V, V_{IN} = \pm 25V, V_{EN} = V_O = 0V, A_0, A_1, A_2 = 0V$ $V_{IN} = \pm 25V, V_O = \pm 10V$		1.0		2			5	med-	
IS(off) with Overvoltage	S	8			1.0		5			10		μΑ
INPUT		V	40 "0" = VAL ≤ 0.8	20.1					-4			
IEN(on) IA(on) A	Ao, A <sub>1</sub> , A <sub>2</sub>	4	V <sub>A</sub> = 2.4	V or 0V	0.01		-10	-30	4	-10	-30	μΑ
or IEN(off) IA(off)	or EN	- 4	V <sub>A</sub> = 15	V or OV	0.01		10	30		10	30	
DYNAMIC	1000 FEE	100.00	150					201				
transition	D		See Fi	gure 3	0.3			annows s	CRROOK			
topen	D		See Fi	gure 4	0.2	1.20		9.80				1 3
ton(EN)	D	11 6 18	See Fi	gure 5	0.6	E 1883	1.5					μ
toff(EN)	D		B = -		0.4		1	13 4	W. Lak			
t <sub>on</sub> -t <sub>off</sub> Break- Before-Make Delay Settling	D	8	V <sub>EN</sub> = +5V, A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> Strobed V <sub>IN</sub> = ±10V, Figure 6		10			STURIN	EBBNOGA Y			ns
"OFF"	D	100	V <sub>EN</sub> = 0, R <sub>L</sub> = 200Ω, C <sub>L</sub> = 3pF, V <sub>S</sub> = 3VRMS,		60	2407.01	Carrier St	пания с		MARKET BY	U1924	dE
The second secon	S	oo ar	$V_S = 0$ $V_{EN} = 0V$		5	MEST	DEIGE	Isnoin	inuA :	998	25%	
C <sub>S(off)</sub>	D	All and and	$V_D = 0$	f = 140kHz	25	43119	archel .	1000		4 100	3. 3	pF
	D to S		$V_S = 0, V_D = 0$	to 1 MHz	1							bi
SUPPLY	2 10 3		VS - 0, VD - 0	TO T WITTE								
Supply +												
Current -	1+	1	All VA, V	(FN = 5\/	0.5	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.





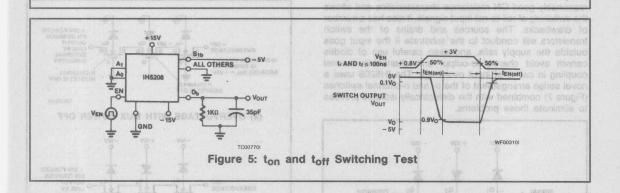


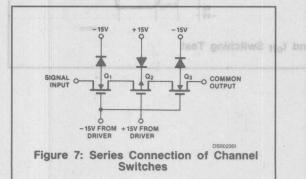
Figure 6: Break-Before-Make Delay Test

#### **DETAILED DESCRIPTION**

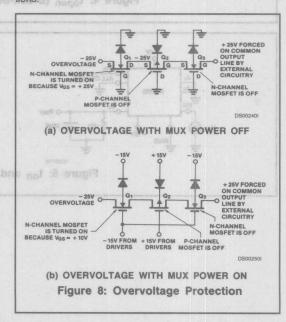
The IH5208, like all Intersil's multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

TC00780

Another, and more important difference lies in the switching channel. Previous devices have used parallel n-and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.



Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



3

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

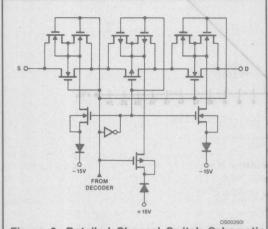
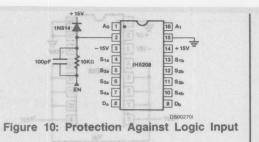


Figure 9: Detailed Channel Switch Schematic



## MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the  $\pm 10V$  range, with a typical  $r_{DS(on)}$  of  $600\Omega$ ; it can successfully handle signals up to  $\pm 13V$ , however,  $r_{DS(on)}$  will increase to about  $1.8k\Omega$ . Beyond  $\pm 13V$  the device approaches an open circuit, and thus  $\pm 12V$  is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

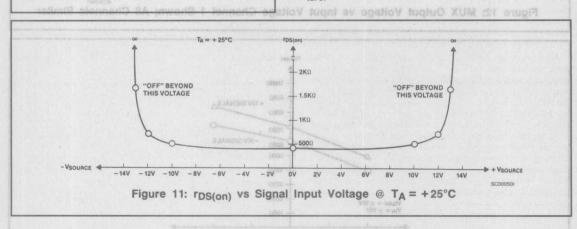


Figure 13: Typical roston) Variation vs Temperature

3-131

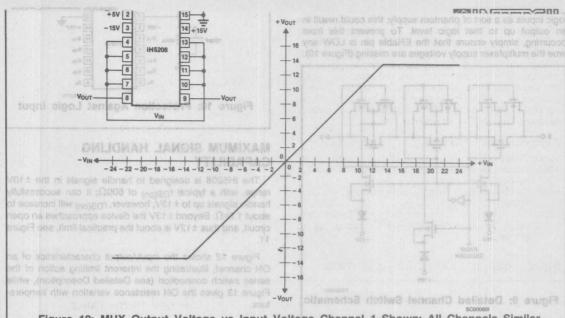
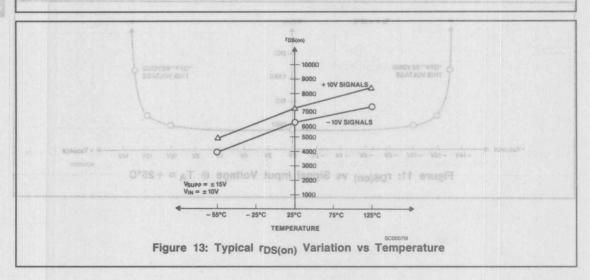


Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar



## USING THE IH5208 WITH SUPPLIES OTHER THAN ±15V

The IH5208 will operate successfully with supply voltages from  $\pm5V$  to  $\pm15V$ , however  $r_{DS(on)}$  increases as supply voltage decreases, as shown in Figure 14. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of  $r_{DS(on)}$  and leakage current remains reasonably constant.  $r_{DS(on)}$  also decreases as signal levels decrease. For high system accuracy [acceptable levels of  $r_{DS(on)}$ ] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.



Further information may be found in:

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 ''A Čookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

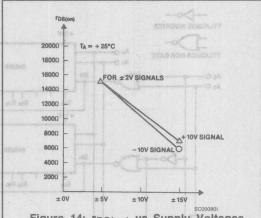


Figure 14: rDS(on) vs Supply Voltages

#### **IH5208 APPLICATIONS INFORMATION**

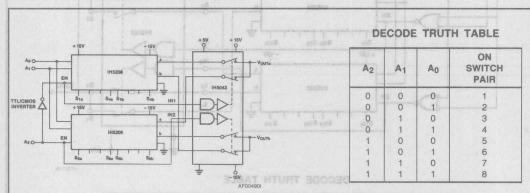
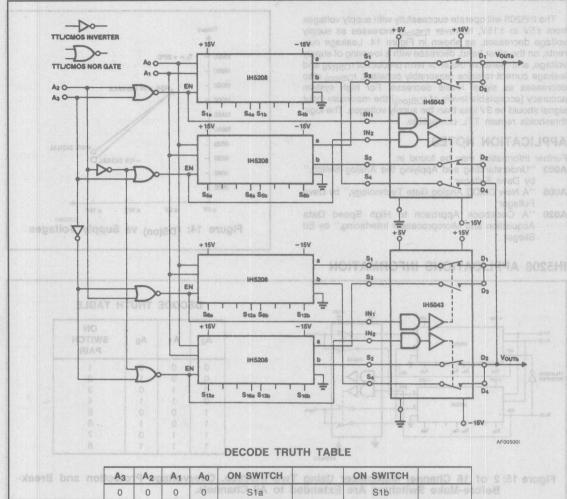


Figure 15: 2 of 16 Channel Multiplexer Using Two IH5208s. Overvoltage Protection and Break-Before-Make Switching Are Extended to All Channels.

Before-Make Switching Are Extended to All Channels.

H5208

#### **IH5208 APPLICATIONS INFORMATION (CONT.)**



0 0 0 S2a S2b 0 0 0 S3a S3b 1 0 0 S4a S4b 1 1 0 0 0 S5a S5b 0 0 S6a S6b 0 0 S7a S7b 0 S8a S8b VouTa Voutb 0 0 0 S9a S9b 0 0 S10a S10b 0 0 S11a S11b 0 S12a S12b 0 0 S13a S13b 0 S14a S14b 1 0 S15a S15b S16a S16b

Figure 16: Submultiplexed 2 of 32 System. The Two IH5043s Are Overvoltage Protected By The IH5208s. Submultiplexing Reduces Output Capacitance and Leakage Currents.

## IH5216

## 8-Channel Differential Fault Protected CMOS Analog Multiplexer

#### **GENERAL DESCRIPTION**

The IH5216 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI507A and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE			
IH5216MJI	-55°C to +125°C	28 pin CERDIP			
IH5216CJI	0°C to +70°C	28 pin CERDIP			
IH5216CPI	0°C to +70°C	28 pin Plastic DIP			

Ceramic package available as special order only (IH5216MDI/CDI)

## **WINTERSIL**

#### **FEATURES**

- All Channels OFF When Power OFF, for Analog Signals Up to ±25V
- Power Supply Quiescent Current Less Than 1mA
- ±13V Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI507A
- Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V
- TTL and CMOS Compatible Binary Address and ENable Inputs

#### DECODE TRUTH TABLE

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH PAIR		
X	X	X	0	NONE		
0	0	0	1	1		
0	0	1	1	2		
0	1	0	1	3		
0	1	1	1	4		
11	0	0	1	5		
a 1a a	0	1	1	6		
1	1	0	1	7		
1	1	1	1	8		

Logic "1" = V<sub>AH</sub> > 2.4V V<sub>ENH</sub> > 2.4V Logic "0" = V<sub>AL</sub> < 0.8V

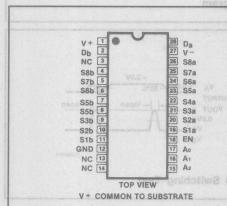
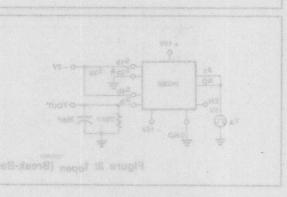
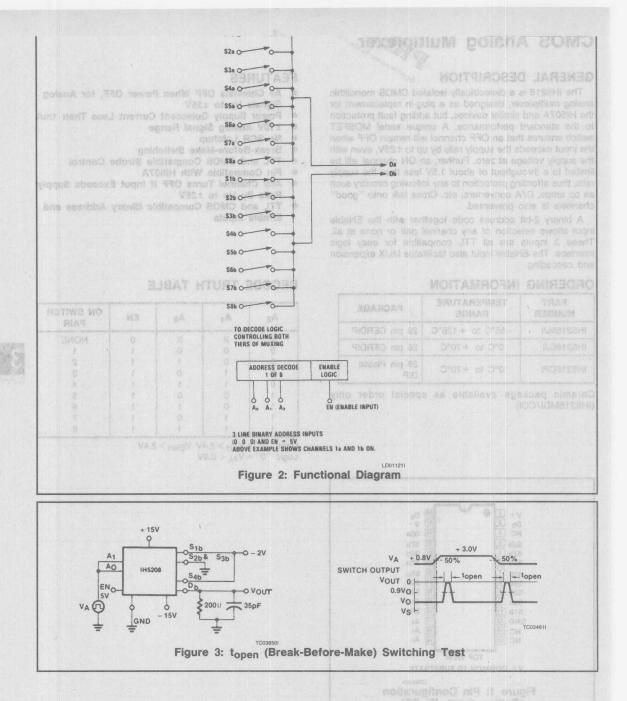


Figure 1: Pin Configuration (Outline dwgs JE, PE)





#### ABSOLUTE MAXIMUM RATINGS

V <sub>IN</sub> (A, EN) to Ground15V to	+15V
Vs or Vp to V+ +25V to	-40V
Vs or VD to V25V to	+40V
V to Ground	16V
V <sup>-</sup> to Ground	16V

Current (Any Terminal)	OmA
Operating Temperature55 to +12	25°C
Storage Temperature65 to +15	50°C
Lead Temperature (Soldering, 10sec)30	)0°C
Power Dissipation* 1200	
*All leads soldered or welded to PC board. Derate 10mW/°C above	70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS (V+ = 15V, V- = -15V, V<sub>EN</sub> = 2.4V, unless otherwise specified.)

CHARACTERISTIC MEASUR	Adka e	NO	TEST CONDITIONS		10 ± 15							Switch
	MEASURED	EASURED TESTS ERMINAL PER			TYP 25°C	MATH SUFFIX () OF		C SUFFIX			UNI	
		TEMP	0		d 14-ph	-55°C	25°C	125°C	0°C	25°C	70°C	silge
SWITCH										saction.	one m	1 18
RDS(on)	S to D	16	$V_D = 10V,$ $I_S = -1.0 \text{mA}$	Sequence each switch on	700	1000	1000	1500	1200	1200	1800	Ω
		16	$V_D = -10V$ $I_S = -1.0 \text{mA}$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V	500	1000	1000	1500	1200	1200	1800	TRA
			RDS(	on)max-RDS(on)min	Marin Brazil		PRESENTA IN		Principle Company	anced horse		
ΔR <sub>DS</sub> (on)			$\Delta R_{DS(on)} = \frac{1}{2}$	RDS(on)avg.	IA-SIN	1.19		0005+	0.10		040116	%
			V <sub>S</sub> =				-			-		
IS(off)	S	16	$V_S = 10V, V_D = -10V$	, 00	0.02	10-01	±0.5	50	U"OS -	±1.0	50	Eaur
		16	$V_S = -10V, V_D = 10V$		0.02		±0.5	50		±1.0	50	- feathers
ID(off)	D	1	V <sub>D</sub> = 10V, V <sub>S</sub> = -10V	V <sub>EN</sub> = 0.8V	0.05	Eddin Assessed	±1.0	100	National Control	±2.0	100	n/
		1	$V_D = -10V, V_S = 10V$		0.05		±1.0	100		±2.0	100	
ID(on)	D	16	$V_{S(AII)} = V_D = 10V$	Sequence each switch on	0.1		±2.0	100		±4.0	100	
	4	16	V <sub>S(AII)</sub> = V <sub>D</sub> = -10V V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V		0.1	±	±2.0	100		±4.0	100	1
FAULT	The same	Z III		and the second s	8.4 15.0		1			- Control		
Is with Power OFF	S	16	V <sub>SUPP</sub> = 0V, V <sub>EN</sub> = V <sub>O</sub> = 0V, A <sub>0</sub> ,	$V_{1N} = \pm 25V$ , A <sub>1</sub> , A <sub>2</sub> = 0V or 5V	1.0		2.0			5.0	-0,	03
Is(off) with Overvoltage	S	16	$V_{IN} = \pm 25V$	$V_0 = \pm 10V$	1.0		2.0			5.0		μ
INPUT	9	11				y	-><					1
IEN(on) IA(on)	Ao, A <sub>1</sub> , A <sub>2</sub>	4	V <sub>A</sub> = 2.4	V or 0V	0.01		-10	-30		-10	-30	18
or IEN(off) IA(off)	or EN	4	V <sub>A</sub> =	15V	0.01		10	30	DE SI	10	30	μΑ
DYNAMIC	tor over	-	D.R. C.	1) 24	0.01		10	- 00		10	00	
transition	T D		The second secon		0.3		1		100			
topen	D		THE PER !		0.2				The same		-	at .
ton(EN)	D				0.6		1.5			1		μ
toff(EN)	D	C. 12. 37.34			0.4		1		100000			
ton-toff Break- Before-Make	o aPillu	16	V <sub>EN</sub> = +5V, A <sub>0</sub> , V <sub>IN</sub> =	A <sub>1</sub> , A <sub>2</sub> Strobed	25							n
Delay Settling Time	disrugi	noo r	Figure 2: Pi				Contract No.	gal0 i	eriolio	with:	grure	F
"OFF" Isolation	D		$V_{EN} = 0$ , $R_L = 200\Omega$ , $C_L = 3pF$ , $V_S = 3VRMS$ , $f = 500kHz$		60	inter	solge	8 10	t base	do b	in jui	d
C <sub>s(off)</sub>	S	/ SI 1 3	V <sub>S</sub> = 0	V <sub>EN</sub> = 0V,	5						(3)/30	1735
C <sub>D(off)</sub>	D		$V_D = 0$	f = 140kHz	25	N. E. O. S.			The state	1		pl
C <sub>DS(off)</sub>	D to S		$V_S = 0, V_D = 0$	to 1 MHz	1							
Supply +	1+	1	All V <sub>A</sub> =	= 0V/5V	0.5		0.6			1.0		
Coppij	1-	1	VEN		0.02		0.6	2		1.0	-	m

2

# IH5341 Dual SPST CMOS RF/Video Switch



#### GENERAL DESCRIPTION

The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically  $t_{\rm on}=150{\rm ns}$  and  $t_{\rm off}=80{\rm ns}$ , and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically  $40\Omega$ – $50\Omega$  with  $\pm 15V$  power supplies, increasing to typically  $175\Omega$  for  $\pm 5V$  supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

#### **FEATURES**

- RDS(on) < 75Ω
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation > 60dB @ 10MHz
- Cross Coupling Isolation > 60dB @ 10MHz
- Compatible With TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current < 1μA
- "Break-Before-Make" Switching
- Fast Switching (80ns/150ns Typ)

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0 to +70°C	14-pin PLASTIC DIP
IH5341ITW	-20°C to +85°C	10-pin TO-100
IH5341MTW	-55°C to +125°C	10-pin TO-100

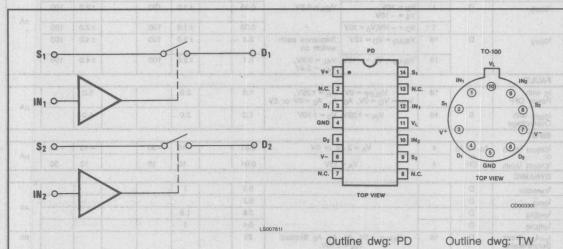


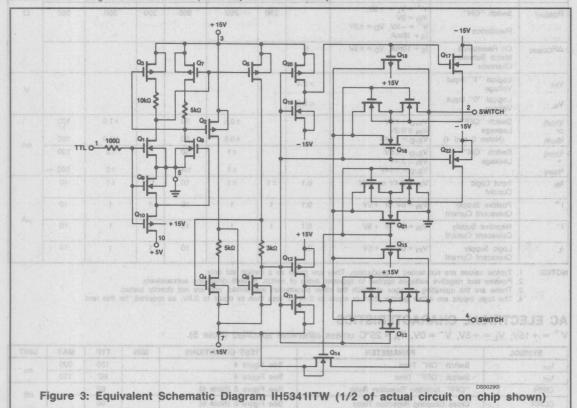
Figure 1: Functional Diagram (Switches are open for a logical "0" control input, and closed for a logical "1" control input.)

Figure 2: Pin Configurations

3

Operating Temperature:	
	55°C to +125°C
(I Version)	25°C to +85°C
(C Version)	0°C to +70°C
Storage Temperature	65°C to +150°C
	ng, 10sec)300°C
Power Dissipation	250mW
Derate above 25°C	@7.5mW/°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



5. All AC parameters are semple rested only.

5. Test ontrult should be built on cepper diad groun

		iling Temperature:	педО	1	A GRADE DI	EVICE	1/	C GRADE DE	EVICE	OI
SYMBOL	PARAMETER	TEST CONDITIONS	TYP	-55°C	+ 25°C	+ 125°C	-25/ 0°C	+ 25°C	+85/ +70°C	UNIT
.o *150°C 250'JV 7.5mW7V	Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	ge Temperature (Solden Temperature (Solden Dissipation (6 stot) Dergte above 25°C	4.5 > 16 4.5 > V <sup>+</sup> -4 > -16	-V Am				gst)	Input Vo (any Te	
RDS(on)	Switch "ON" Resistance (Note 4)	$V_D = \pm 5V$ $I_S = 10 \text{mA}, \ V_{IN} \ge 2.4V$ $V_D = \pm 10V$	permanent of	75	75 125	100	75 150	75 150	100	eogyad noilthac
R <sub>DS(on)</sub>	Switch "ON" Resistance	$V^{+} = V_{L} = +5V,$ $V_{IN} = 3V$ $V^{-} = -5V, V_{D} = \pm 3V$ $I_{S} = 10 \text{mA}$		250	250	350	300	300	350	Ω
ΔR <sub>DS(on)</sub>	On Resistance Match Between Channels	$I_S = 10 \text{mA}, \ V_D = \pm 5 \text{V}$	5	. I	410		L			
V <sub>IH</sub>	Logical ''1'' Input Voltage Logical ''0'' Input Voltage	WILL THE	> 2.4			15	300			٧
ID(off) or IS(off)	Switch "OFF" Leakage (Notes 2 and 4)	$V_{S/D} = \pm 5V$ $V_{IN} \le 0.8V$ $V_{S/D} = \pm 14V$	H		±0.5	50	Lie	±1.0	100	
ID(on) + IS(on)	Switch ''ON'' Leakage	$V_{S/D} = \pm 5V$ $V_{IN} \ge 2.4V$ $V_{S/D} = \pm 14V$			±1	50 100		±2 ±2	100	nA
IIN	Input Logic Current	V <sub>IN</sub> ≥ 2.4V or < 0V	0.1	±1	±1	10	±1	±1	10	
1+	Positive Supply Quiescent Current	V <sub>IN</sub> = 0V or +5V	0.1	1	1	10	1	1	10	
1-	Negative Supply Quiescent Current	V <sub>IN</sub> = 0V or +5V	0.1	1	1	10	1	1	10	μΑ
IL.	Logic Supply Quiescent Current	V <sub>IN</sub> = 0V or +5V	0.1	otes	18.5	10	W841	1	10	

- Typical values are not tested in production. They are given as a design aid only.
   Positive and negative voltages applied to opposite sides of switch, in both directions successively.
   These are the operating voltages at which the other parameters are tested, and are not directly tested.
   The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

#### AC ELECTRICAL CHARACTERISTICS

 $V^{+} = +15V$ ,  $V_{L} = +5V$ ,  $V^{-} = 0V$ ,  $T_{A} = 25^{\circ}C$  unless otherwise specified (Note 5).

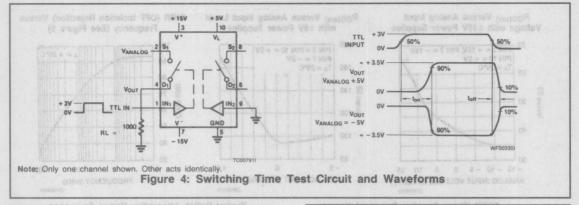
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ton	Switch "ON" Time	See Figure 4		150	300	
toff	Switch "OFF" Time	See Figure 4		80	150	ns
OIRR	"OFF" Isolation Rejection Ratio	See Figure 5 (Note 6)		60		dB
CCRR	Cross Coupling Rejection Ratio	See Figure 6 (Note 6)	PO EXPONEN	60	o comp	UD
f <sub>3dB</sub>	Switch Attenuation 3dB Frequency	See Figure 7 (Note 6)		100		

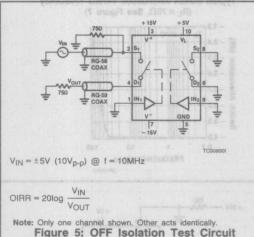
NOTES:

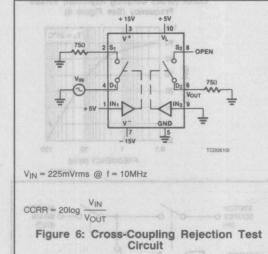
5. All AC parameters are sample tested only.6. Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

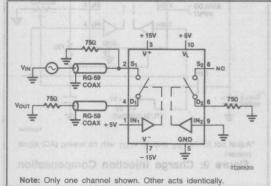
3

#### TEST CIRCUITS









Nominally, at DC, this ratio is equal to -4dB. When the attenuation reaches -1dB, the frequency at which this occurs is f<sub>3dB</sub>.

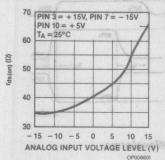
ATTN: = 20  $log_{10} \frac{1}{RDS(on) + RL}$ 

Figure 7: Switch Attenuation Versus Frequency, Test Circuit

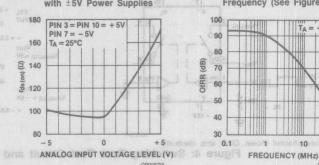
3-141

#### TYPICAL PERFORMANCES CHARACTERISTICS

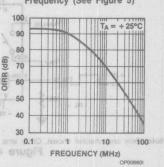
RDS(on) Versus Analog Input Voltage with ±15V Power Supplies



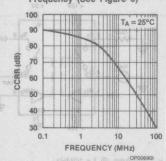
R<sub>DS(on)</sub> Versus Analog Input Level with ±5V Power Supplies



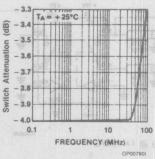
**OIRR (OFF Isolation Rejection) Versus** Frequency (See Figure 5)



CCRR (Cross Coupling Rejection) Versus Frequency (See Figure 6)



Typical Switch Attenuation Versus Frequency  $(R_L = 75\Omega, See Figure 7)$ 



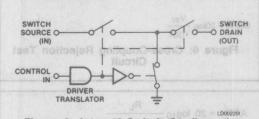
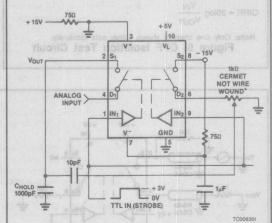


Figure 8: Internal Switch Configuration



\*Adjust pot for 0mV<sub>p-p</sub> step @ V<sub>OUT</sub> with no analog (AC) signal

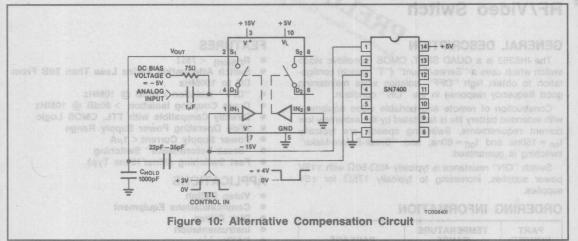
Figure 9: Charge Injection Compensation

#### DETAILED DESCRIPTION

As can be seen in Figure 8, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much better isolation between the input and the output than single series switch does, especially at high frequencies. The result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, giving very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility, and the state of t

3



#### **APPLICATIONS**

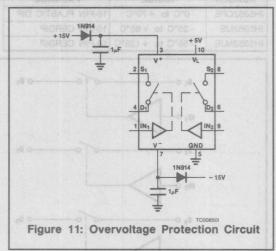
#### **Charge Compensation Techniques**

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at VS/D of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 9 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The  $1k\Omega$  potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the -5V to +5V range.

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 10. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to -5V as shown in the figure. The choice of -5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.



#### Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 11.

# \* RF/Video Switch

#### GENERAL DESCRIPTION

The IH5352 is a QUAD SPST, CMOS monolithic video switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically ton = 150ns and toff = 80ns, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically  $40\Omega$ - $50\Omega$  with  $\pm 15V$ power supplies, increasing to typically  $175\Omega$  for  $\pm 5V$ supplies.

#### ORDERING INFORMATION

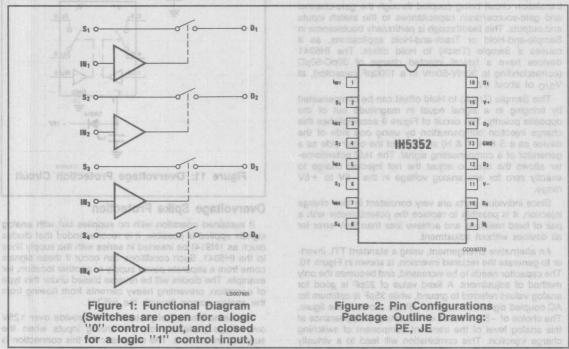
PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5352CPE	0°C to +70°C	16-PIN PLASTIC DIP
IH5352IJE	-25°C to +85°C	16-PIN CERDIP
IH5352MJE	-55°C to +125°C	16-PIN CERDIP

#### **FEATURES**

- RDS(on)  $< 75\Omega$
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation > 60dB @ 10MHz
- Cross Coupling Isolation > 60dB @ 10MHz
- Directly Compatible with TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current < 1µA
- "Break-Before-Make" Switching
- Fast Switching (80ns/150ns Typ)

#### **APPLICATIONS**

- Video Switch
- **Communications Equipment**
- Disk Drives
- Instrumentation
- CATV



#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C Unless Otherwise Noted)

V <sup>+</sup> to Ground	+ 17V	Storage Temperature	-65°C to +160°C
V <sup>-</sup> to Ground	–17V	Lead Temperature	
V <sub>L</sub> to Ground	V <sup>+</sup> to V <sup>-</sup>	(Soldering, 10sec)	300°C
Logic Control Voltage	V <sup>+</sup> to V <sup>-</sup>	Power Dissipation:	
Analog Input Voltage	V <sup>+</sup> to V <sup>-</sup>	CERDIP	450mW
Current (any terminal) Operating Temperature:		derate 4mW/°C above 25°C	990 350mW
(M Version)		derate 3mW/°C above 25°C	REQU
(I Version)(C Version)	20°C to +85°C 0°C to +70°C	Switch Attenuation 3dB Frequency	ene <sup>†</sup>

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $V^+ = +15V$ ,  $V^- = -15V$ ,  $V_L = +5V$ ,  $T_A = 25^{\circ}C$  unless otherwise noted.

						OO	MAXIMUN	RATING	S	(TERM)	10002	
SYMBOL	SYMBOL PARAMETER	TEST CONDITIONS		TYP	M G	RADE DE	VICE	I/C G	RADE DE	DEVICE		
en ans ne willion doe weellent o	mer soletion betwe la simple series s des The result is a			@ 25°C	-55°C	+ 25°C	+ 125°C	-25/0°C	+ 25°C	+ 85/ + 70°C	HTHEO I	
offw segrative +	Supply Voltage - Positive Supply	ns oebiV s	ation in the	and the local division in the local division			ĺ		NSLATOR -	ur		
	Logic Supply			5 to 15	Igusti	29					V	
s and give	Negative Supply	140 senes	3HI erti lo .	-5 to -15	i i			PROPERTY.	HIEL OF	WIG 1 .3	гои	
villidited	Switch "ON"	Is = 10mA	$V_D = \pm 5V$	50	75	75	100	75	75	100		
RDS(on)	Resistance (Note 4)	V <sub>IN</sub> ≥ 2.4V	$V_D = \pm 10V$	100	125	125	175	150	150	175		
R <sub>DS(on)</sub>	Switch "ON" Resistance	+5V V = -	I <sub>S</sub> = 10mA, V <sup>+</sup> = V <sub>L</sub> = +5V V <sup>-</sup> = -5V, V <sub>D</sub> = ±3V, V <sub>IN</sub> = 3V		250	250	350	300	300	350	Ω	
ΔR <sub>DS(on)</sub>	On Resistance Match Between Channels	I <sub>S</sub> = 10mA,	$V_D = \pm 5V$	5	W 1001 + 10	8) at		9-1				
ViH	Logical ''1'' Input Voltage	75+ JTT 100001 +31		> 2.4		Al	permi	d				
VIL	Logical "0" Input Voltage	VO.S+		< 0.8	W	13	-0,0	-   3		T	V	
ID(off) or IS(off)	Switch 'OFF' Leakage (Note 2 and 4)	$V_{S/D} = \pm 5V$ $V_{S/D} = \pm 14V$ $V_{IN} \le 0.8V$			V ACTO - A	±1.0	50		±2.0 ±2.0	100		
ID(on)	Switch 'ON' Leakage	V <sub>S/D</sub> = ±5V V <sub>S/D</sub> = ±14V		1990 P		a ± 1.0	100	d- -	±2.0	100	nA	
IS(on)	Logic Control Input Current	V <sub>IN</sub> ≥ 2.4V V <sub>IN</sub> ≥ 2.4V o	r < 0V	0.1	±1	±1.0	100	±1	±2.0	100		
1+	Positive Supply Quiescent Current	V <sub>IN</sub> = 0V or	+ 5V	0.1	1	1	10	1	1	10	100	
1-	Negative Supply Quiescent Current	V <sub>IN</sub> = 0V or	+ 5V	0.1	1	1	10	1	1,0000	10	μА	
L	Logic Supply Quiescent Current	V <sub>IN</sub> = 0V or	+ 5V	0.1	mil t	nidasiwi	10	Figu	1	10		

#### **AC ELECTRICAL CHARACTERISTICS**

 $V^+ = +15V$ ,  $V_L = +15V$ ,  $V^- = -15V$ ,  $T_A = 25$ °C unless otherwise specified (Note 5).

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
ton	Switch "ON" Time	-V of	W. Andrews	150	300	Vi to Gradu
moda, toff	Switch "OFF" Time OREO	"V of	*V	80	150	ns
OIRR	"OFF" Isolation Rejection Ratio	AVIIUG	Laborator Com-	60	(EGM19)	Autrent (87)
CCRR	Cross Coupling Rejection Ratio	125°C	- 56°C to -	60	(noiste	dB
f <sub>3dB</sub>	Switch Attenuation 3dB Frequency	- U-68 +	01 U'US	100	Land Land St.	MHz

- 1. Typical values are not tested in production. They are given as a design aid only.
- Positive and negative voltages applied to opposite sides of switch, in both directions successively.
- These are the operating voltages at which the other parameters are tested, and are not directly tested.
- 4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.
- 5. All AC parameters are sample tested only.

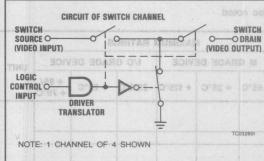
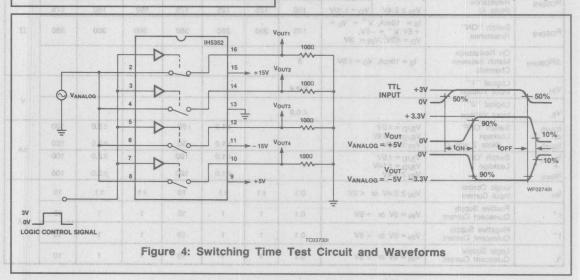


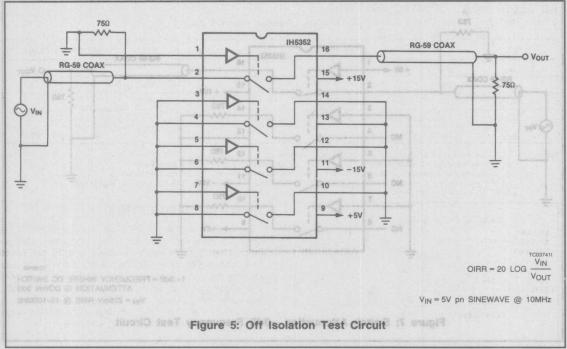
Figure 3: Internal Switch Configuration

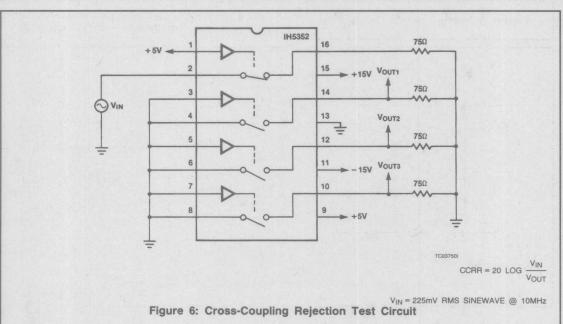
#### DETAILED DESCRIPTION

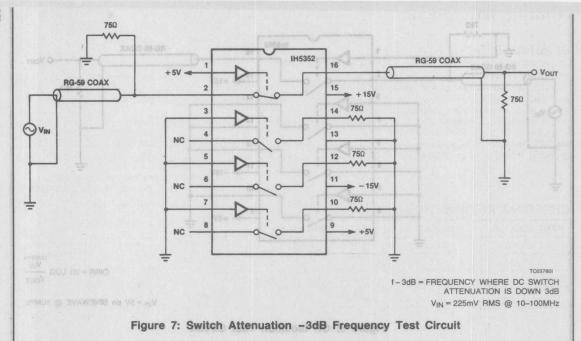
Figure 3 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent offisolation in the Video and RF frequency ranges when compared to conventional analog switches.

The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.









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# IH6108 8-Channel CMOS **Analog Multiplexer**

# GENERAL DESCRIPTION STATES OF THE PROPERTY OF

The IH6108 is a CMOS monolithic, one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided for use as a system enable. When the ENable input is high (5V), a channel is selected by the three Address inputs, and when low (0V) all channels are off. The 3 Address inputs are TTL and CMOS logic compatible, with a "1" corresponding to any voltage greater than 2.4V.

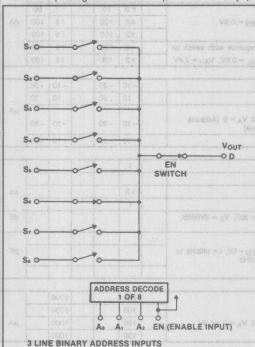
### FEATURES +V of gV to gV

- Ultra Low Leakage ID(off) ≤ 100pA
- rDS(on) < 400 Ohms Over Full Signal and Temperature Range
- Power Supply Quiescent Current Less Than
- ±14V Analog Signal Range at 18 solved and to resize and
- No SCR Latchup to not another profes murrous to the back to
- No SCR Latenup Break-Before-Make Switching
- Binary Address Control (3 Address Inputs Control 8 Channels)
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With DG508, HI-508 & AD7508

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MJE	-55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

Ceramic package available as special order only (IH6108MDE/CDE)



(1 0 1) AND EN @ 5V ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

Figure 1: Functional Diagram

#### DECODE TRUTH TABLE

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
×	×	×	0	NONE
0	0	0	1	
S 0 V	0	1 1 5	1 80 ph d	210) AT 10 (M
0	10.01	0	studet 1	3 moral res
0	1	1	A LA	4
1	0	0	1	5
19	0	1	199	6
. 1.	1	0	1 1	7
1	1	1-1-	1	8

A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub> Logic ''1'' = V<sub>AH</sub> ≥ 2.4V V<sub>ENH</sub> ≥ 4.5V Logic ''0'' = V<sub>AL</sub> ≤ 0.8V

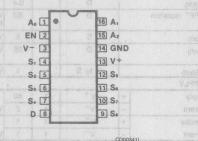


Figure 2: Pin Configuration

305530-002



#### **ABSOLUTE MAXIMUM RATINGS**

VIN (A, EN) to Ground       -15V to 15V         VS or VD to V+       0, -32V         VS or VD to V-       0, 32V         V+ to Ground       16V	Current (Analog Source or Drain)
V- to Ground	Power Dissipation (Package)*
Current (Any Terminal)30mA	*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

V+ = 15V, V- = -15V, V<sub>EN</sub> = +5V (Note 1), Ground = 0V, unless otherwise specified.

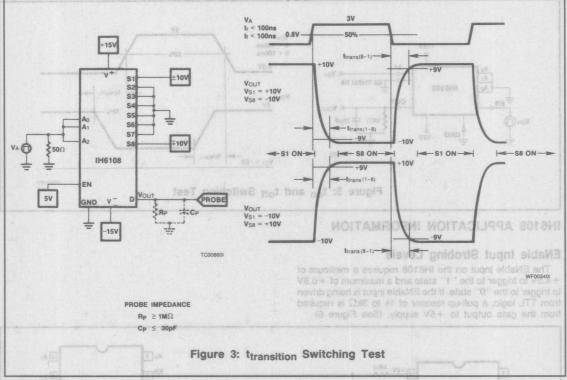
obe Control	DE MUNISON	NO	FINES 1	data all a			1	WAX L	IMITS			
CHARACTERISTIC	MEASURED TERMINAL	TESTS PER	TYP 25°C	TEST CONDITIONS			SUFF	-		SUFF		UNI
		TEMP						125°C	0°C	25°C	70°C	FFE
SWITCH				TESAM	SAR ROMAN S	61173	<b>原型的</b>	3727	10	Jacket .	166 T	BAG
		8	180	C. C	Sequence each switch on	300	300	400	350	350	450	13
rDS(ON)	S to D	8	150	$V_D = -10V$ , $I_S = -1.0 \text{m/s}$	$V_{AL} = 0.8V, V_{AH} = 2.4V$	300	300	400	350	350	450	Ω
Δr <sub>DS</sub> (ON)			20	$\triangle r_{DS(on)} = \frac{\triangle r_{DS}}{r_{DS}}$	$\frac{S(on)min}{(on)avg.} V_S = \pm 10V$	S of S	20			390	3013	%
		8	0.002	$V_S = 10V, V_D = -10V$	ecial order only (IHI	DE 88	±.5	50	0082	±1	50	ea
IS(OFF)	S	8	0.002	$V_S = -10V, V_D = 10V$	Control of the Contro	Control of the last	±.5	50		±1	50	-
	23 142 3 7	1	0.03	$V_D = 10V, V_S = -10V$	V <sub>EN</sub> = 0.8V		±2	100		±5	100	nA
ID(OFF)	D	1	0.03	$V_D = -10V, V_S = 10V$		100	±2	100		±5	100	
The second second second second		8	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	100	770	±5	100	
ID(ON)	D	8	0.1	$V_{S(ALL)} = V_D = -10V$			±2	100		±5	100	
INPUT			A I			34.	KI		4			
IAN(ON) or IA(on)	A <sub>0</sub> , A <sub>1</sub> or A <sub>2</sub>	3	0.01	V <sub>A</sub> = 2.4V or 0V	The Day of the Control of the Contro		-10	-30	3 6	-10	-30	100
IAN(OFF) IA(off)	Inputs	3.	0.01	V <sub>A</sub> = 15V or 0V	V		10	30		10	30	
I <sub>A</sub>	A <sub>0</sub> , A <sub>1</sub> A <sub>2</sub>	3	0 1	V <sub>EN</sub> = 5V	All V <sub>A</sub> = 0 (Address pins)		-10	-30		-10	-30	1 38
	EN	1	T	V <sub>EN</sub> = 0			-10	-30	70	-10	-30	
DYNAMIC			1		C Chimenon des Calman	-				1111		
transition	D		0.3	See Fig. 1	# #		1		-			
topen	D	STA	0.2	See Fig. 2		OF REAL PROPERTY.						
ton(EN)	D		0.6	See Fig. 3			1.5				183	μs
toff(EN)	D		0.4				1		P-1-0		G :	
"OFF" Isolation	A BY D	ēb.	60	$V_{EN} = 0$ , $R_L = 200\Omega$ , $C_{en} = 500$ kHz	$C_L = 3pF$ , $V_S = 3VRMS$ ,							dB
C <sub>s(off)</sub>	S	ISJ#	5	V <sub>S</sub> = 0								
C <sub>d(off)</sub>	D	13.1	25	V <sub>D</sub> = 0	V <sub>EN</sub> = 0V, f = 140kHz to 1MHz		Ĺ				-0.	pF
C <sub>DS(off)</sub>	D to S	i in l	, 1	$V_S = 0, V_D = 0$								
SUPPLY	2 171	la.				3000	55.00	SECOND IN	1			
Supply +	V+	1	40		*		200			1000		
Current -	V-	1	2	V <sub>EN</sub> = 5V	4	-6	100			1000		
Standby +	V+	1	1		All V <sub>A</sub> = 0 or 5V	363	100	1		1000		μA
Current -	V-	1	1	V <sub>EN</sub> = 0	A SECOND PARTY OF THE PROPERTY		100		1	1000		1

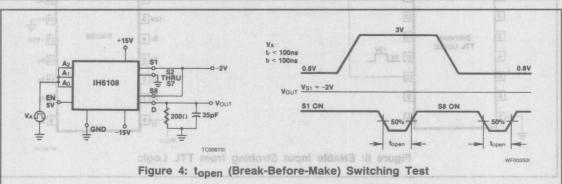
NOTE 1: See Enable Input Strobing Levels, in Application Section.

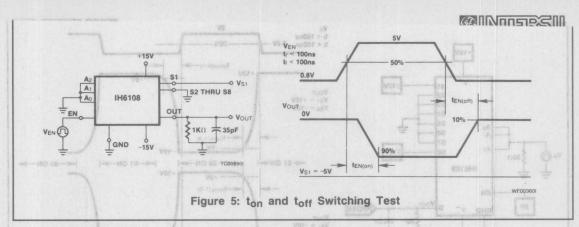
SWITCHING INFORMATION (CONT.)

3

#### SWITCHING INFORMATION



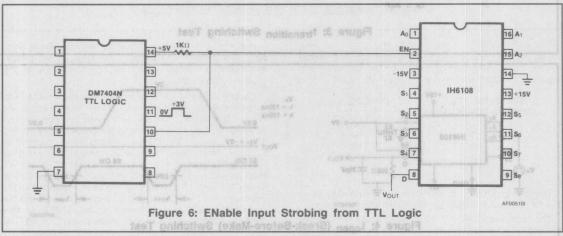




#### **IH6108 APPLICATION INFORMATION**

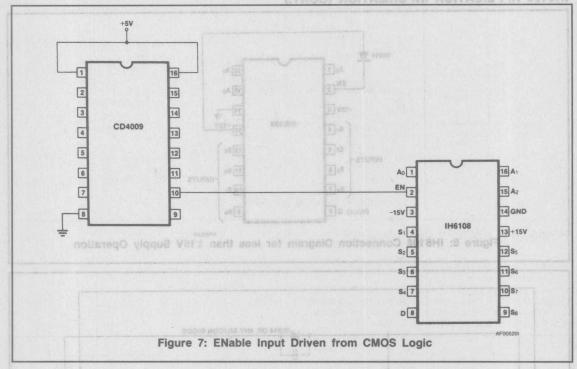
#### **ENable Input Strobing Levels**

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the ''1'' state and a maximum of +0.8V to trigger to the ''0'' state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to  $3k\Omega$  is required from the gate output to +5V supply. (See Figure 6)



When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 7.

# IH6108 APPLICATION INFORMATION (CONT.)



The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The following chart shows the effect, on  $t_{trans}$  for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL t <sub>trans</sub>
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than eight channels is required. In these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

Using the IH6108 with supplies other than ±15V

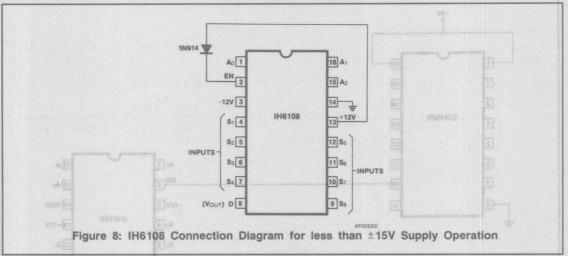
The IH6108 can be used with power supplies ranging from  $\pm 6V$  to  $\pm 16V$ . The switch rDS(on) will increase as the

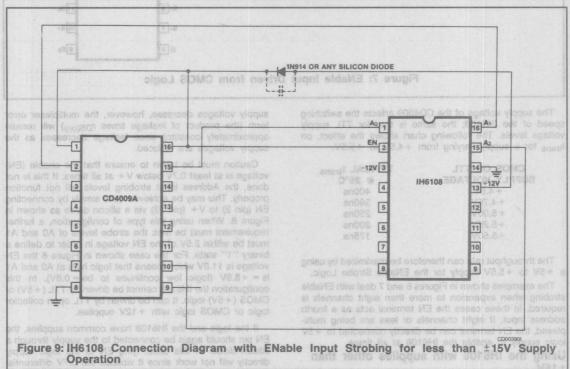
supply voltages decrease, however, the multiplexer error term (the product of leakage times r<sub>DS(on)</sub>) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V+ at all times. If this is not done, the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V+ (pin 13) via a silicon diode as shown in Figure 8. When using this type of configuration, a further requirement must be met: the strobe levels of A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V+ and EN, (See Figure 9). A  $1\mu F$  capacitor can be placed across the diode to minimize switching glitches.

3





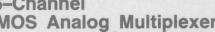
#### Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to  $\pm$ 14V (actually -15V to +14.3V because of the input protection diode) when using  $\pm$ 15V supplies.

The electrical specifications of the IH6108 are guaranteed for  $\pm 10V$  signals, but the specifications have very minor changes for  $\pm 14V$  signals. The notable changes are slightly lower r<sub>DS(on)</sub> and slightly higher leakages.

## IH6116

# 16-Channel **CMOS Analog Multiplexer**



#### GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to be used as a system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.



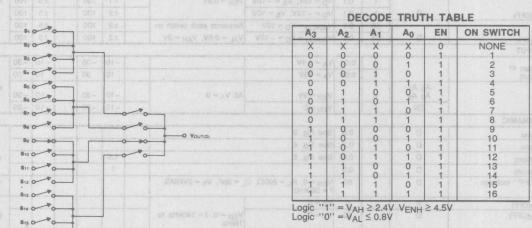
# FEATURES +V of gV 10 gV

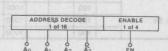
- Pin Compatible With DG506, HI-506 & AD7506
- Ultra Low Leakage ID(off) ≤ 100pA
- ±11 Analog Signal Range
  rDS(on) < 700 Ohms Over Full Signal and Temperature Range
- Break-Before-Make Switching
- TTL and CMOS Compatible Address Control
- Binary Address Control (4 Address Inputs Control 16 Channels)
- Two Tier Submultiplexing to Facilitate Expandability
- **Power Supply Quiescent Current Less Than** 100 µA
- No SCR Latchup

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MJI	-55°C to +125°C	28 pin CERDIP
IH6116CJI	0°C to 70°C	28 pin CERDIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6116MDI/CDI)





**4 LINE BINARY ADDRESS INPUTS** (0 0 0 1) AND EN & 5V ABOVE EXAMPLE SHOWS CHANNEL 9 TURNED ON

Figure 1: Functional Diagram



Figure 2: Pin Configuration

V <sub>IN</sub> (A, EN) to Ground15V to 15V	Current (Analog Source of Drain)
Vs or Vp to V+	Operating Temperature55 to 125°C
Vs or VD to V	Storage Temperature65 to 150°C
V+ to Ground	Lead Temperature (Soldering, 10sec)300°C
V- to Ground16V	Power Dissipation (Package)* 1200mW
Current (Any Terminal)30mA	*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

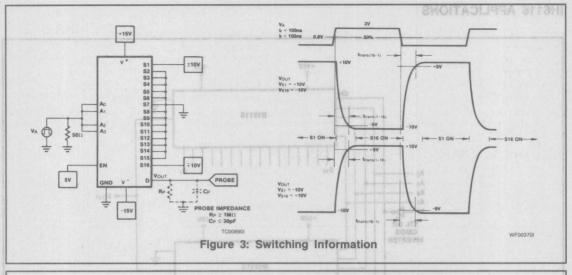
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

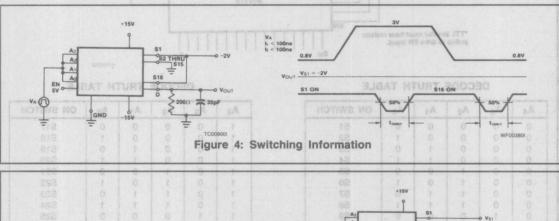
ELECTRICAL CHARACTERISTICS

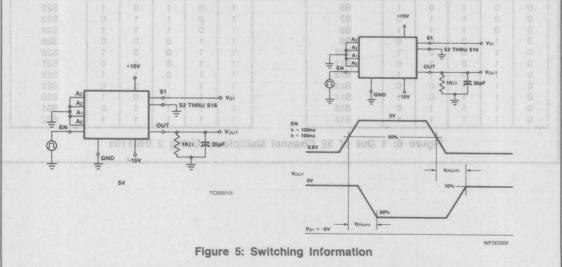
V+=15V, V-=-15V,  $V_{EN}=+5V$  (Note 1), Ground = 0V, unless otherwise specified.

		NO	Assista	ENDERGE © Power S	HB, 10		MAX L	IMITS	FRETT		Iden	
CHARACTERISTIC	MEASURED	TESTS	TYP 25°C	AUGOS TEST C	M	M SUFFIX			SUFF	1X	UNIT	
	TERMINAL	TEMP	Lated	908 old 4.		-55°C	25°C	125°C	0°C	25°C	70°C	
SWITCH			J. I.				- A -	25 400 400	-		a and one	
		16	480	$V_D = 10V$ , $I_S = -1mA$	Sequence each switch on	600	600	700	650	650	750	Call E S.
rds(ON)	S to D	16	300	$V_D = -10V$ , $I_S = 1mA$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 3V	600	600	700	650	650	750	Ω
Δr <sub>DS(ON)</sub>			20	$\Delta r_{DS(on)} = \frac{r_{DS(on)ma}}{r_{DS}}$	$\frac{1}{(\text{on})^{\text{avg.}}} \text{V}_{\text{S}} = \pm 10 \text{V}_{\text{S}}$	of C	00-			ILO ILO	8118	%
		16	0.01	$V_S = 10V, V_D = -10V$	id asi	C) C	±.5	50		±1	50	11
IS(OFF)	S	16	0.01	$V_S = -10V, V_D = 10V$	at order only (iH811)	seas	±.5	50	/G S	no#lbi	50	nave
WHILE THE PARTY		1	0.1	$V_D = 10V, V_S = -10V$	V <sub>EN</sub> = 0.8V		±1	100		±5	100	nA
ID(OFF)	D	anthon	0,1	$V_D = -10V, V_S = 10V$		100871.	±2	100		±5	100	
pro-distance of the second second	The second second	16	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on	AL S	±2	100	TAIL	±5	100	
ID(ON)	M3 DOA	16	0.1	$V_{S(ALL)} = V_D = -10V$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 3V		±2	100		±5	100	
INPUT	1 4	1 6	A						6		1.30	
IA(on) or	1111	4	0.01	V <sub>A</sub> = 2.4V		1	-10	-30	-	-10	-30	
IA(off)	1 0	4	0.01	V <sub>A</sub> = 15V			10	30	-	10	30	
I <sub>A</sub>	A <sub>0</sub> A <sub>1</sub> A <sub>2</sub> A <sub>3</sub>	4	T. F.	V <sub>EN</sub> = 5V	All V <sub>A</sub> = 0		-10	-30		-10	-30	μΑ
	EN	1		V <sub>EN</sub> = 0		1000	-10	-30	730 3	-10	-30	
DYNAMIC .	1 1		1	0						162		
ttrans	D	U	0.6	See Fig. 3	and the same	0					7	
t <sub>open</sub>	Do		0.2	See Fig. 4		100 mm				200	950	
tEN(on)	D		0.8	See Fig. 5		10	1.5		1	1	110	μs
tEN(off)	D	0	0.3	Bleefall Breeze			1		-	1000	120	
"OFF" Isolation	Do	T.	60	$V_{EN} = 0$ , $R_L = 200\Omega$ , $C_{f} = 500$ kHz	$C_L = 3pF, V_S = 3VRMS,$					100	518	dB
C <sub>s(OFF)</sub>	S	N C - C	5	V <sub>S</sub> = 0					100	4		
C <sub>d</sub> (OFF)	D .	V8.0≥	40	$V_D = 0$	V <sub>EN</sub> = 0, f = 140kHz to 1MHz				-	9-	8/2	pF
C <sub>ds</sub> (OFF)	D to S	17	1	$V_S = 0, V_D = 0$					1	18-19	8.6	
SUPPLY	A 20	Fe 247							Olipio.	STREET, STREET	0.03	
Supply	+ V+	1.1	55		PERSONAL PROPERTY.		200		G5-612	1000	1927	
Current	- V-	1	2	V <sub>EN</sub> = 5V			100	21/1		1000	1888	
Standby	+ V+	1	1	District September	All VA = 0 or 5V		100	Dag Ba	BOULE	1000		μΑ
Current	- V-	1	1	V <sub>FN</sub> = 0	1 191		100			1000		

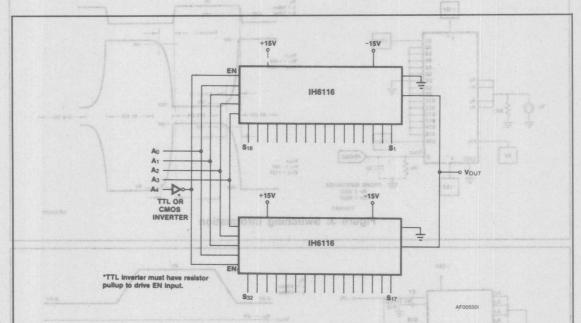
NOTE 1: See Section V. Enable Input Strobing Levels.







### **IH6116 APPLICATIONS**



#### DECODE TRUTH TABLE

DECODE T	RUTH	TABLE
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A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S2 S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	11	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
100	0	₹1	1	S12
1	1	0	0	S13
1	1	0	1911	S14
1	1	1	0	S15
1	1	1,	1 20	S16
	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 0 1 0 1 1 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 0 1 1 0 0 1 1 1 1 0 0 1 1 1 1 0 0 1 1 1 1 0 0 1 1 1 1 0 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0

A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
34 97	0	0	1	0	S19
1	0	0	1	1	S20
-1	0	-1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	Alex	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1.70	1	1	0	1	S30
1	aca year	11	1	0	S31
1	1	1	1	1	S32

Figure 6: 1 Out of 32 Channel Multiplexer Using 2 IH6116s

#### **IH6116 APPLICATIONS (CONT.)**

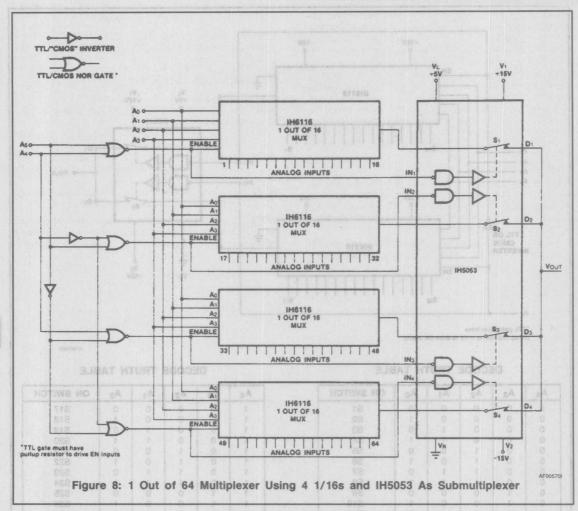
-15V IH6116 +15V IH5041 Di o Vout -15V +15V D2 Ī CMOS IH6116 EN -15V \*TTL gate must have pullup resistor to +5V to drive EN inputs

#### DECODE TRUTH TABLE

#### DECODE TRUTH TABLE

A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH		A <sub>4</sub>	A3	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH
0	0	0	0	0	S1	BY SO TUD 1	1	0	0	0	0	S17
0	0	0	0	1	S2	25294	1	0	0	0	1	S18
0	0	0	1	0	S3		1	0	0	1	0	S19
0	0	0	1	1	S4		11	0	0	1	1	S20
0	0	1	0	0	S5	ANALOG THE	1	0	1	0	0	S21
0	0	1	0	1	S6		1	0	1	0	1	S22
0	0	1	1	0	S7		1	0	1	1	0	S23
0	0	11.	state o	a tec	S8 S9	t a comptt	natal	0	\$8 <sup>1</sup> to	nito	1 0	S24
0	1	0	0	0	S9	A STATE OF	1	1	0	0	0	S25
0	1	0	0	-1-	S10	-	1	1	0	0	1	S26
0	1	0	. 1	0	S11 S12		.1	1	0	. 1	0	S27 S28
U	eria alpi	U				10	9419	HI TO	0	SC 450	NE 134	S28
0	191911	aria er	0	0	S13	ΦY nod	ni desh	de <b>1</b> neri	w. Jexe	0.0	0 W	s 218S29HI e
0	Ference	MA SIN	0	mayor i	S14	(a)	to abloo	o A is	catub ra	0	s di b	S30 den
0	d dans	111	on't le	00	0 1 515	All A LICE STORY	muito e		tentor a	a tenn		
0	uods to	dente	I M bri	diam	S16		1	1-00	ate 1	1 1 00	alter i	S32

Figure 7: 1 Out of 32 Channel Multiplexer Using 2 IH6116s; Using An IH5041 for Submultiplexing



### General note on expandability of IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacitance and leakage than would be possible with a system using all 16 channels tied to one common output. Also the expandability into 32, 64, 128, channels etc. is facilitated. Figures 6, 7, and 8 show how the IH6116 can be expanded.

Figure 6 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each

6116 are tied together so that 8 channels are tied to the  $V_{OUT}$  common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7  $I_{D(offs)}$  and 1  $I_{D(on)}$ , or about 1.0nA of typical leakage at room temperature. Throughput speed will be typically 0.8 $\mu$ s for  $t_{on}$  and 0.3 $\mu$ s for  $t_{off}$ . Throughput channel resistance will be in the 500 $\Omega$  area.

Figure 7 shows the 1 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacitance. The IH5041 has typical ON resistances of  $50\Omega$  (max. is  $75\Omega$ ) so it only increases thruput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about  $0.5\mu s$  for both ON and OFF time, and output leakage is about 0.2nA.

Figure 8 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5053 is used to get the third tier of MUXing. The  $V_{\rm OUT}$  point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Throughput channel resistance will be in the 550 ohm area with throughput switching speeds about 1.3 $\mu$ s for ON time and 0.8 $\mu$ s for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of  $1\text{-}2\mu\text{A}$ , so that no excessive system power is dissipated. Note that the logic of the 5053 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra circuitry being required.

#### Enable input strobing levels

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX. However, when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V  $\pm$ 5% for the high state and less than 0.8V for

the low state. When using TTL logic, a pull-up resistor of  $1 \mathrm{k} \Omega$  or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V + at all times. See IH6108 data sheet for details.

# APPLICATION NOTES

Further information may be found in:

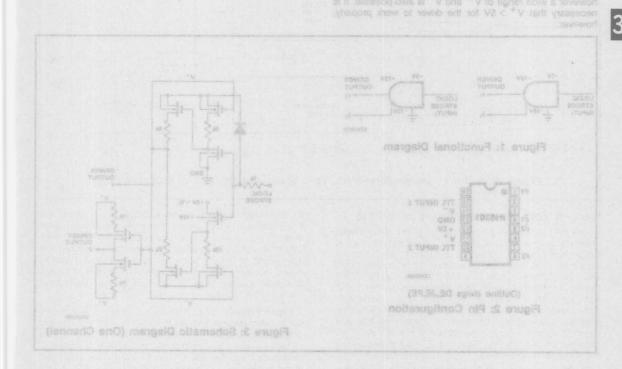
A003 "Understanding and Applying the Analog Switch,"

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliener

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection," by Dick Wilenken

**NOTE:** This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the rDS(ON) of the switch is maintained at specified values.



When used in conjunction with the Intersil IH401 family of Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. toff time < ton time). The combination has typical  $t_{off} \approx 80$ ns and typ.  $t_{on} \approx 200$ ns for signals up to 20Vpp in amplitude.

A TTL "1" input strobe will force the  $\theta$  driver output up to V<sup>+</sup> level; the ₱ output will be driven down to the V<sup>-</sup> level. When the TTL input goes to ''0'', the  $\theta$  output goes to V' and  $\overline{\theta}$  goes to V'; thus  $\theta$  and  $\overline{\theta}$  are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive N and P channel MOSFETs, to make a complete CMOS analog gate.

The driver typically uses +5V and ±15V power supplies, however a wide range of V + and V - is also possible. It is necessary that V+ > 5V for the driver to work properly, however.



## FEATURES sets mito 0.55 orb nl ed like eanstaleer

- Driven Direct From TTL or CMOS Logic
- Translates Logic Levels Up to 30V Levels
- Switches 20VACPP Signals When Used in Conjunction With Intersil IH401A Varafet (As An Analog Gate)
- toN ≤ 300ns & toFF ≤ 200ns for 30V Level Shifts
- Quiescent Supply Current ≤ 100µA for Any State (D.C.)
- Provides Both Normal & Inverted Outputs

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANG				
*IH6201CDE	A B 0°C to 70°C TOH				
*IH6201MDE	-55°C → +125°C				
IH6201CJE	Juga 0°C to 70°C bases				
IH6201MJE	-55°C to 125°C				
IH6201CPE	0°C to 70°C				

<sup>\*</sup>Special Order Only

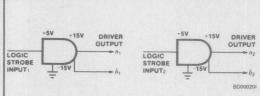
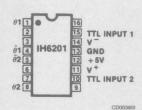


Figure 1: Functional Diagram



(Outline dwgs DE,JE,PE) Figure 2: Pin Configuration

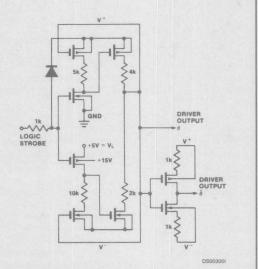


Figure 3: Schematic Diagram (One Channel)

#### ABSOLUTE MAXIMUM RATINGS

V+	to V-no that a melaya ent to	very useful feature	35V
V+	t an irratir can compine to mak		35V
V-	See pient ned Turrens end 1986	T SWEED, OF AR 1710	35V
V+	to VINI	HOLLING BOIRUR II	40V

Operating Temperature		to	+125°C
Storage Temperature			
Lead Temperature (Soldering, 10sec)	mingre		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL SPECIFICATIONS V+ = +15V, V- = -15V, V<sub>1</sub> = +5V

Var. Ed. ITEMORII		IH6201CDE			girl, en r	uarter of a		
ITEM®	TEST CONDITIONS	-25°C	+ 25°C	+85°C	-55°C	+ 25°C	+ 125°C	UNIT
$\theta$ or $\overline{\theta}$ driver output swing	V <sub>IN</sub> = 0V _ TL + 3V Fig. 5B		28		v o vet+	28		V <sub>pp</sub>
V <sub>IN</sub> strobe level ("1")for proper translation	$\frac{\theta \ge 14V}{\overline{\theta} \ge -14V}$	3.0	3.0	3.0	La	2.4		V <sub>D.C.</sub>
V <sub>IN</sub> strobe level ("0")for proper translation	$\frac{\theta}{\theta} \ge -14V$ $\frac{\theta}{\theta} \ge 14V$	0.4	0.4	0.4	\$ 1140	0.8		V <sub>D.C.</sub>
I <sub>IN</sub> input strobe current draw (for 0V - 5V range)	V <sub>IN</sub> = 0V or +5V	±1	±1	10	±1	±1	10,000	μА
ton time	V <sub>IN</sub> = 0V JL C <sub>L</sub> = 30pF switching turn-on time fig. 5B		400			300	HBOKT	ns
t <sub>off</sub> time	V <sub>IN</sub> = 0V JL C <sub>L</sub> = 30pF switching turn-off time fig. 5B		300	0	-4	200		ns
I + (V +) power supply quiescent current	V <sub>IN</sub> = 0V or +5V	100	100	100	100	100	100	μΑ
I (V ) power supply quiescent current	V <sub>IN</sub> = 0V or +5V	100	100	100	100	100	100	μΑ
I <sub>L</sub> (V <sub>L</sub> ) power supply quiescent current	V <sub>IN</sub> = 0V or +5V	100	100	100	100	100	100	μΑ

#### **APPLICATIONS**

#### Input Drive Capability

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V to 2.4V levels max. and min, respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to  $\pm 5 V$  line. This resistor is not critical and can be in the  $1 k \Omega$  to  $10 k \Omega$  range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

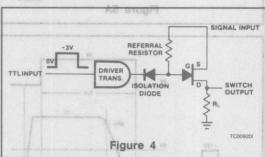
When the input strobe voltage level goes below Gnd (i.e. to -15V) the circuit is unaffected as long as V  $^+$  to V<sub>IN</sub> does not exceed absolute maximum rating.

#### Output Drive Capability

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel JFETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents a forward bias condition between the signal input and the  $\pm V_{CC}$  supply. The IH6201 will drive any JFET provided some sort of isolation is added i.e.

You will notice in Figure 4 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for the inadequate charge area curve for isolation diode (i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output JFET] switch won't function; then adding this resistor overcomes this condition. The "refer-

rall' resistor is normally in the 100k $\Omega$  to 1M $\Omega$  range and is not too critical.



# Making a Complete Solid State Switch That Can Handle 20Vpp Signals

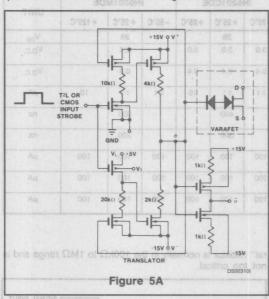
The limitation on signal handling capability comes from the output gating device. When a JFET is used, the pinch-off of the JFET acting with the V $^-$  supply does the limiting. In fact max, signal handling capability = 2 (Vp + (V $^-$ )) Vpp where Vp = pinch-off voltage of JFET chosen. i.e. Vp = 7V, V $^-$  = -15V .: max. signal handling = 2 (7V + (-15V)) Vpp = 2(7V - 15)pp = 2(-8Vpp) = 16Vpp. Obviously to get  $\geq$  20Vpp, Vp  $\geq$  5V with V $^-$  = -15V. Another simple way to get 20Vpp with Vp = 7V, is to increase V $^-$  to -17V. In fact using V $^+$  = +12V or +15V and setting V $^-$  = -18V

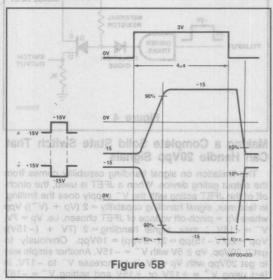
#### APPLICATIONS (CONT.)

allows one to switch 20Vpp with any member of IH401 family. The advantage of using the Vp = 7V pinch-off (along with unsymmetrical supplies), over the Vp = 5V pinch-off (and  $\pm 15V$  supplies), is that you will have a much lower RDS(ON) for the Vp = 7 JFET (i.e. for the 2N4391).

$$r_{DS(ON)} \approx 22\Omega$$
,  $r_{DS(ON)} \approx 35\Omega$ )  
 $V_p = 7V$   $V_p = 5V$ 

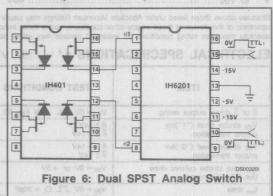
The IH6201 is a dual translator, each containing 4 CMOS FETs pairs. The schematic of one-half IH6201, driving one-quarter of an IH401, is shown in Figure 5A.

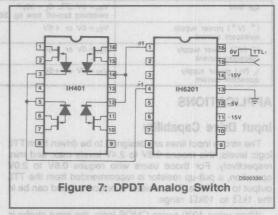




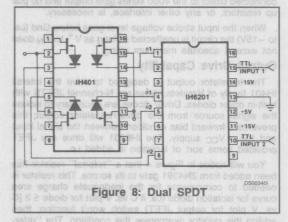
the inverse of  $\overline{\theta}$ .

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See Figure 8)





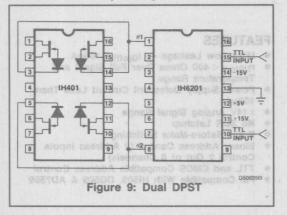
NOTE: Either switch is turned on when strobe input goes high.



4-Channel Differential

3

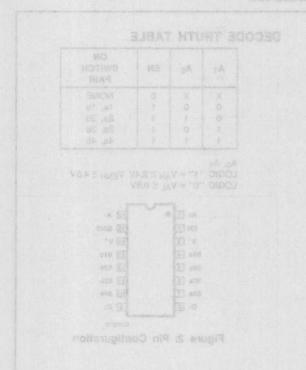
## APPLICATIONS (CONT.)

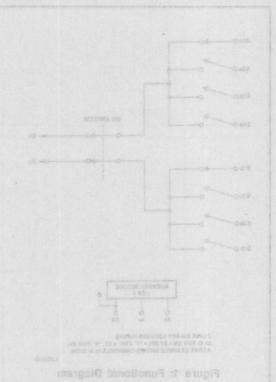


GENERAL DESCRIPTION
The linescen is a monolithic 2 of 8 CMOS multiplexer. The
part is a plug-in replacement for the DGBOS Two line binary
part is a plug-in replacement for the DGBOS. Two line binary
parts by the binary inputs additionally a third input is
provided to use as a system enable. When the ENable input
is high (5V) the channels are sequenced by the Life binary
inputs, and when low (6V) atl originate are off, the 2
inputs are controlled by TTL legic or CMOS logic
inputs are with a "O" corresponding to any voltage leas than
elements with a "O" corresponding to any voltage lease than
elements the ENable input must be laten to 5V to
season to 5V to
season to 4V to the ENable input must be laten to 5V to
season and lease than 0.00 to deable the

TEMPERATURE NAME	
	HISOSOFIE

Commis parkens available as special order only (HE208MDE/CDE)





# IH6208

# 4-Channel Differential CMOS Analog Multiplexer

#### **GENERAL DESCRIPTION**

The IH6208 is a monolithic 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

# **WINTERSIL**

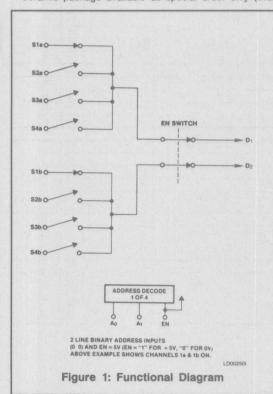
#### **FEATURES**

- Ultra Low Leakage I<sub>D(off)</sub> ≤ 100pA
- r<sub>DS(on)</sub> < 400 Ohms Over Full Signal and Temperature Range
- Power Supply Quiescent Current Less Than
   100µA
- ±14V Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- Binary Address Control (2 Address Inputs Control 2 Out of 8 Channels)
- TTL and CMOS Compatible Address Control
- Pin Compatible With HI509, DG509 & AD7509

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MJE	-55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

Ceramic package available as special order only (IH6208MDE/CDE)



#### **DECODE TRUTH TABLE**

A <sub>1</sub> A <sub>0</sub>		EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A<sub>0</sub>, A<sub>1</sub> LOGIC ''1'' =  $V_{AH} \ge 2.4V \ V_{ENH} \ge 4.5V$ LOGIC ''0'' =  $V_{AL} \le 0.8V$ 

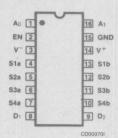


Figure 2: Pin Configuration

SWITCHING INFORMATION

#### ABSOLUTE MAXIMUM RATINGS

V <sub>IN</sub> (A, EN) to Ground	Current (Analog Source or Drain)
Vs or Vp to V <sup>+</sup>	Operating Temperature55 to 125°C
Vs or Vp to V	Storage Temperature65 to 150°C
V <sup>+</sup> to Ground	Lead Temp (Soldering, 10sec)300°C
V <sup>-</sup> to Ground16V	Power Dissipation (Package)* 1200mW
Current (Any Terminal) 30mA	*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

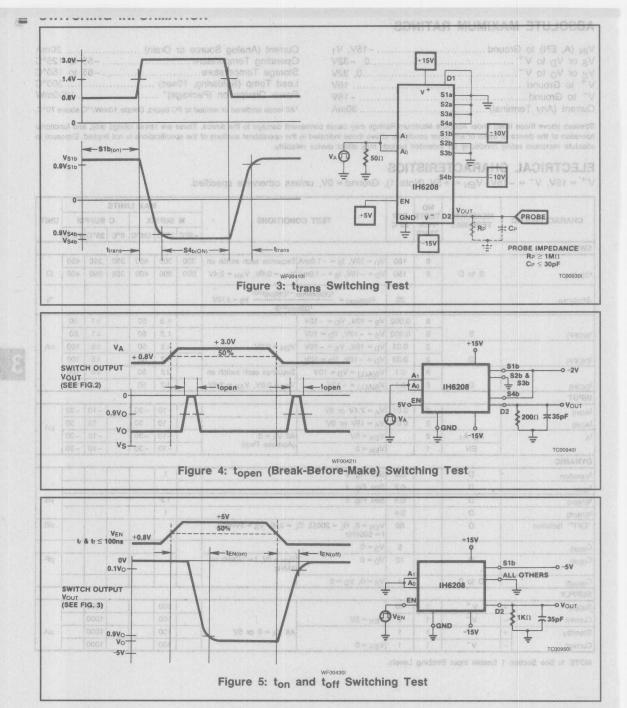
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $V^+ = 15V$ ,  $V^- = -15V$ ,  $V_{EN} = +5V$  (Note 1), Ground = 0V, unless otherwise specified.

		NO	18	Type and the same			- 1	MAX L	MAX LIMITS			
CHARACTERISTIC	MEASURED TERMINAL	TESTS	TYP 25°C	TEST CONDITIONS		-	SUFF			SUFF		UNI
		TEMP	77		Venezus	-55°C	25°C	125°C	0°C	25°C	70°C	5.0
SWITCH	187	The same			and-one of the	0.88	200	- leafin	3/69/2		16.5	
Tag5 = 40		8	180		Sequence each switch on	300	300	400	350	350	450	
rDS(ON)	S to D	8	150	The second section of the second seco	$V_{AL} = 0.8V, V_{AH} = 2.4V$	300	300	400	350	350	450	Ω
Δr <sub>DS</sub> (ON)			20	$\Delta$ rDS(on) = $\frac{\text{rDS(on)ma}}{\text{rDS}}$	$\frac{1}{(on)^{avg}}$ $V_S = \pm 10V$							%
		8	0.002	$V_S = 10V, V_D = -10V$		166	±.5	50		±1	50	
IS(OFF)	S	8	0.002	$V_S = -10V, V_D = 10V$		W. British	±.5	50		±1	50	
	7219	2	0.03	$V_D = 10V, V_S = -10V$	V <sub>EN</sub> = 0.8V	NAME OF TAXABLE PARTY.	±2	50	237	±5	100	nA
ID(OFF)	D	2	0.03	$V_D = -10V, V_S = 10V$	VEN - 0.00	-	±2	50		±5	100	
VE 0 TA 058 A		8	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	50	132%	±5	100	
ID(ON)	Dangel	8	0.1	V <sub>S(ALL)</sub> = -10V	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 2.4V		±2	50		±5	100	0.00
INPUT	-1		3			19	-		0			
I <sub>A(on)</sub>	Банараналия	2	0.01	V <sub>A</sub> = 2.4V or 0V		11	-10	-30	ove.	-10	-30	
I <sub>A(off)</sub>	must	2	0.01	V <sub>A</sub> = 15V or 0V	All V <sub>A</sub> = 0	1.1	10	30		10	30	μА
I <sub>A</sub>	Ao, A <sub>1</sub>	2	9	V <sub>EN</sub> = 5V			-10	-30		-10	-30	1
200000	EN	1		V <sub>EN</sub> = 0	(Address Pins)		-10	-30		-10	-30	
DYNAMIC				(resigna)								100
transition	D	Buse	0.3	See Fig. 3	mount magol in 9	mile.	1					
topen	D		0.2	See Fig. 4			and the last	and the second	economics and		and produ	
tEN(on)	D	of extending	0.6	See Fig. 5			1.5			linkerski		μs
tEN(off)	D		0.4		VA.		1					
"OFF" Isolation	D		60	$V_{EN} = 0$ , $R_L = 200\Omega$ , $C_{f} = 500$ kHz	$C_L = 3pF$ , $V_S = 3VRMS$ ,		4	WE OF	MEN			dB
C <sub>s(off)</sub>	S		5	V <sub>S</sub> = 0	ment .		1	(a-Citaliana)	2019914	238.0		
Cd(off)	D	Signification of the same of t	12	V <sub>D</sub> = 0	V <sub>EN</sub> = 0V, f = 140kHz to 1MHz	-	100	emerea	VO OVTU			pF
C <sub>ds(off)</sub>	D to S		771	$V_S = 0, V_D = 0$		1						
SUPPLY		The second				1			304	DAMES IN	211 100	THE BY
Supply +	V+	1	40			1	200			1000	1.330)	
Current 44 -	V-	1	2	V <sub>EN</sub> = 5V			100			1000		
Standby +	V+	1	1		All V <sub>A</sub> = 0 or 5V		100		oves	1000		μΑ
Current -	V-	1	1	$V_{EN} = 0$	Spot autocount unserview aut 1	Balls.	100		OX	1000		

NOTE 1: See Section 1 Enable Input Strobing Levels.

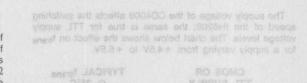


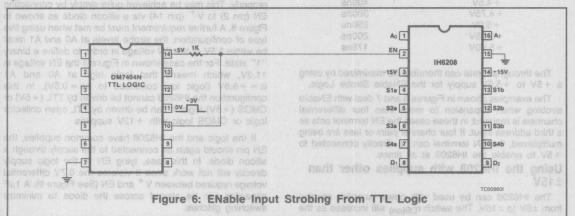
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#### **IH6208 APPLICATION INFORMATION**

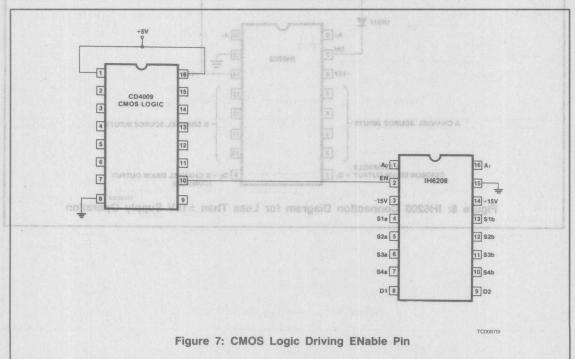
## **ENable Input Strobing Levels**

The ENable input on the IH6208 requires a minimum of +4.5 V to trigger it into the "1" state and a maximum of +0.8 V to trigger it into the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to  $3 \text{k} \Omega$  is required from the gate output to +5 V supply. (See Figure 6).





When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 7)



#### **IH6208 APPLICATION INFORMATION (CONT.)**

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on  $t_{trans}$  for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t <sub>trans</sub> @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than four differential channels is required; in these cases the EN terminal acts as a third address input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

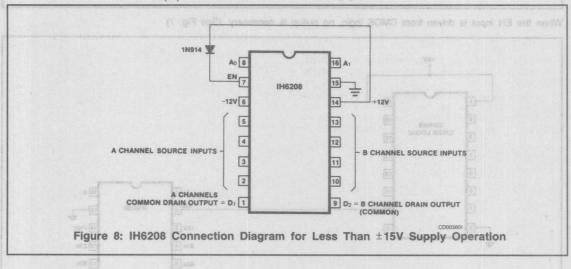
# Using the IH6208 with supplies other than $\pm 15 \text{V}$

The IH6208 can be used with power supplies ranging from  $\pm 6V$  to  $\pm 16V$ . The switch  $r_{DS(on)}$  will increase as the

supply voltages decrease, however, the multiplexer error term (the product of leakage times r<sub>DS(on)</sub>) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V  $^+$  at all times. If this is not done the Address Input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V  $^+$  (pin 14) via a silicon diode as shown in Figure 8. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V, which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V  $^{+}$  and EN (See Figure 9). A  $1\,\mu\text{F}$  capacitor can be placed across the diode to minimize switching glitches.



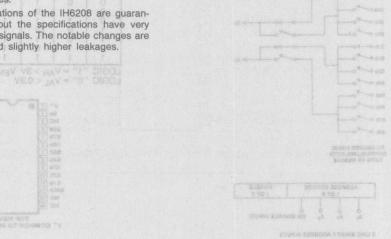
8-Channel Differential

Figure 9: IH6208 Connection Diagram With ENable Input Strobing for Less Than ±15V Supply Operation

#### Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually -15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower rDS(on) and slightly higher leakages.



#### GENERAL DESCRIPTION

The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs: additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V), all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the FNable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

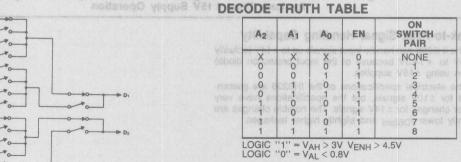
#### **FEATURES**

- Pin Compatible With HI507, DG507 & AD7507
- ±11V Analog Signal Range
- rps(on) < 700 Ohms Over Full Signal and Temperature Range
- Break-Before-Make Switching
- TTL and CMOS Compatible Address Control
- Binary Address Control (3 Address Inputs Control 2 Out of 16 Channels)
- Two Tier Submultiplexing to Facilitate Expandability
- Power Supply Quiescent Current Less Than 100 ...A
- No SCR Latchup
- Very Low Leakage ID(OFF) ≤ 100pA

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RAN	IGE PACKAGE
IH6216MJI	-55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6216MDI/CDI)



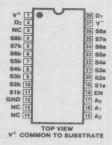


Figure 2: Pin Configuration



TO DECODE LOGIC CONTROLLING BOTH TIERS OF MUXING

**3 LINE BINARY ADDRESS INPUTS** (0 0 0) AND EN - SV ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON. LD002601

Figure 1: Functional Diagram

#### ABSOLUTE MAXIMUM RATINGS

	promount of the Vol.
V <sub>IN</sub> (A, EN) to Ground15V <sub>0</sub> -V <sub>1</sub>	Current (Analog Source or Drain)
Vs or Vp to V+	Operating Temperature55 to 125°C
Vs or Vp to V	Storage Temperature65 to 150°C
V+ to Ground	Lead Temperature (Soldering, 10sec)300°C
V- to Ground16V	Power Dissipation (Package)* 1200mW
Current (Any Terminal)30mA	*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

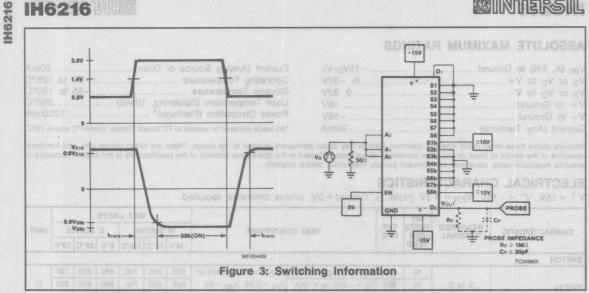
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

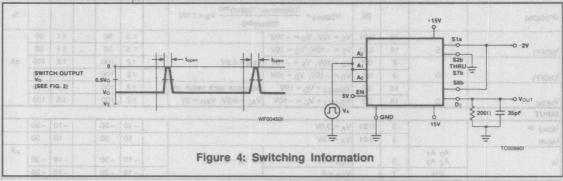
#### **ELECTRICAL CHARACTERISTICS**

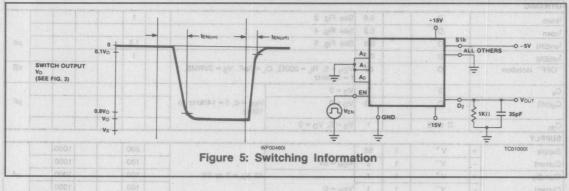
 $V^{+} = 15V$ ,  $V^{-} = -15V$ ,  $V_{EN} = +5V$  (Note 1), Ground = 0V, unless otherwise specified.

	91 3 an h	NO	10003		TEST CONDITIONS		1/1	MAX L	IMITS			
CHARACTERISTIC	MEASURED	TESTS	TYP 25°C	TEST CO			SUFF	IX	C	SUFF	ix	UN
ASSESSED AND ASSESSED AND ASSESSED ASSESSED	PERMINAL	TEMP	250			-55°C	25°C	125°C	0°C	25°C	70°C	
SWITCH PROPERTY					04/00/09	7						
		16	480	$V_D = 10V, I_S = -1mA$	Sequence each switch on	600	600	700	650	650	750	
rds(ON)	S to D	16	300	$V_D = -10V$ , $I_S = 1mA$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 3V	600	600	700	650	650	750	2
Δrds(ON)	981-		20	$\Delta r_{DS(on)} = \frac{r_{DS(on)ma}}{r_{DS}}$	$\frac{1}{(ax-rDS(an)min} V_S = \pm 10V$ $\frac{1}{(an)avg}$							9/
	ati gamanan	16	0.01	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V		100	±.5	50		±1	50	
IS(OFF)	S	16	0.01	$V_S = -10V, V_D = 10V$			±.5	50	4.50	±1	50	
	USETY -	2	0.1	$V_D = 10V, V_S = -10V$	V <sub>EN</sub> = 0.8V	197	±2	100		±5	100	n
ID(OFF)	ette D	2	0.1	$V_D = -10V, V_S = 10V$			±2	100	.70	±5	100	
	-0	16	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	100	18 19	±5	100	
ID(ON)	D	16	0.1	$V_{S(ALL)} = V_D = -10V$	V <sub>AL</sub> = 0.8V, V <sub>AH</sub> = 3V		±2	100		±5	100	
INPUT		Quis	6	W (1)								
I <sub>A(on)</sub> or	VSI	3	0.01	V <sub>A</sub> = 3.0V			-10	-30		-10	-30	
I <sub>A</sub> (off)		3	0.01	V <sub>A</sub> = 15V			10	30		10	30	
IA	A <sub>0</sub> A <sub>1</sub> A <sub>2</sub> A <sub>3</sub>	3	not	V <sub>EN</sub> = 5V	All V <sub>A</sub> = 0		-10	-30		-10	-30	μ
	EN	11	A CONTRACTOR OF THE PARTY OF TH	$V_{EN} = 0$			-10	-30	indaininin	-10	-30	
DYNAMIC	THE STREET OF STREET, STREET, SA	STATE OF THE STATE OF	and an area	rendered to the large of the second of				TO DESCRIPTION (NO.)	001/12/21		-	
trans	Der		0.6	See Fig. 3			1					
topen	D		0.2	See Fig. 4								
ton(EN)	D		0.8	See Fig. 5		completes	1.5	nol- 5				μ
toff(EN)	D		0.3				1	1 040				
"OFF" Isolation	D		60	$V_{EN} = 0$ , $R_L = 200\Omega$ , $C_{f} = 500$ kHz	$C_L = 3pF, V_S = 3VRMS,$				710	24 GUVP	QV QV 1358)	d
Cs	S		5	$V_S = 0$								
Cd(off)	d D	CHES	20	$V_D = 0$	$V_{EN} = 0$ , $f = 140$ kHz to 1MHz			+- 549				p
C <sub>ds</sub>	D to S		1	$V_S = 0, V_D = 0$	Department of the control of the con			104				
SUPPLY			12	1000			191	1 0			THE R	900
Supply +		1	55	108400	40 -2 mme <sup>24</sup>		200	1		1000		
Current -	V-	1	2	V <sub>EN</sub> = 5V	ne to ambia		100			1000		
Standby +	V +	1	1		All $V_A = 0$ or $5V$		100		nle ven	1000	- Water	μ
Current -	V-	1	1	$V_{EN} = 0$			100			1000		

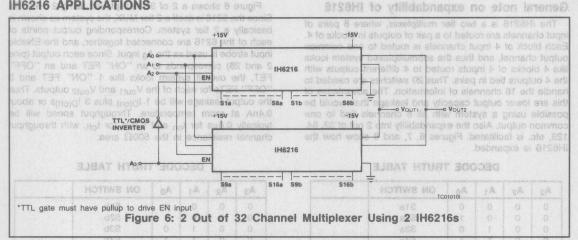
NOTE 1: See Enable Input Strobing Levels, Section 1.





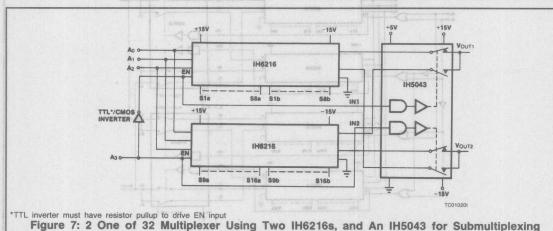


#### IH6216 APPLICATIONS to S a awords & anugin



			DEC	ODE	TRUTH TABLE	1 0		
1	A3	A <sub>2</sub>	A <sub>1</sub>	Ao	ON SWITCH	1 1 9	A3	A <sub>2</sub>
	0 0 0 0 0 0 0 0 0 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0	0 0 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 1 1	0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 0 0 0 1 0	S1a S2a S3a S4a S5a S6a S7a S8a S9a S10a S11a S12a S13a S14a S15a	Vout1	0 0 0 0 0 0 0 0 0 0 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH		0
000000000000000000000000000000000000000	0 0 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 1	0 0 0 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1	S1b S2b S3b S4b S5b S6b S7b S8b S9b S10b S11b S12b S12b S13b S14b S15b	Vo	UT2



The IH6216 is a two tier multiplexer, where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacity and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 6, 7, and 8 show how the IH6216 is expanded.

basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the ENable input strobe is used as the A3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the Vout1 and Vout2 outputs. Thus the output leakage will be 1 lp(on) plus 3 lp(off)s or about 0.4nA at room temperature. Throughput speed will be typically 0.8  $\mu$ s for  $t_{On}$  and 0.3  $\mu$ s for  $t_{Off}$ , with throughput channel resistance in the 500  $\Omega$  area.

#### DECODE TRUTH TABLE

DECODE TRUTH	TABLE
--------------	-------

dara	ON SWITCH	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>
	S1a	0	0	0	0
	S2a S2a	188	0	0	0
	S3a	0	1	0	0
	S4a	1	1	0	0
	UST S5a	0	0	1	0
eA LeA	S6a	i swi	0	1	0
20 1.20	S7a	0	1	-1	0
VouT1	S8a	dia	1	1	0
	S9a	0	0	0	1
	S10a	date	0	0	1
	S11a 0	0	1	0	1
	S12a	98 J	1	0	1
1 1 2	S13a	0	0	.1	1
	S14a	oot	0	1	1
	S15a	0	1	1	1
	S16a	112	1	1	1

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ON SWITCH	
0	0	0	0	with of S1b, even from a	ulap JTT
0	10	0	:8 e	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	al in the season in
0	1	0	0	WAT S5b	
0	1	0	and a	S6b	Attention to the
0	1	1	0	S7b	DA
0	1	1	811	S8b V	OUT2
1	0	0	0	S9b	
1	0	0	801	S10b	
1	0	1	0	S11b	
1	0	1	888	S12b	
1	1	0	0	S13b	
17	04	0	884	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

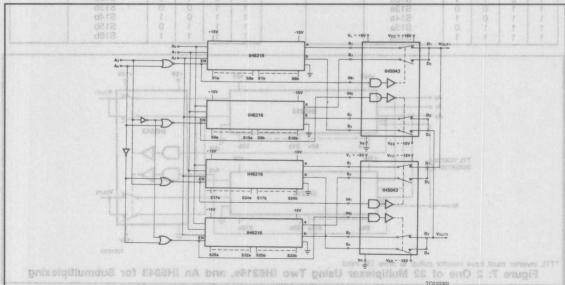


Figure 8: 2 One of 64 Multiplexer Using 4 IH6216s and 2 IH5043s as Submultiplexers

Figure 7 shows the 2 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacity. The IH5043 has typical ON resistance of  $50\Omega$  (max. is  $75\Omega$ ) so it only increases throughput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about  $0.5\mu s$  for both ON and OFF time, and output leakage is about 0.2nA.

Figure 8 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5043 is used for the third tier of MUXing. Each  $V_{out}$  point will see 3 OFF channels and 1 ON channel at anytime, so that the typical leakages will be about 0.4nA. Throughput channel resistance will be in the  $550\Omega$  area and throughput switching speeds about  $1.3\mu s$  for ON time and  $0.8\mu s$  for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2 $\mu$ A so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

#### Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A<sub>3</sub> input.

For the system to function properly the EN input (pin 18) must go to 5V  $\pm 5\%$  for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of  $1k\Omega$  or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V+ at all times. See IH6208 data sheet for details.

#### APPLICATION NOTES well as (allow on a) annive

Further information may be found in: Wall and a second

A003 "Understanding and Applying the Analog Switch," by Dave Fullagar

A006 "A New CMOS Analog Gate Technology," by Dave Fullagar

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Slieger

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection." by Dick Wilenken

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the rds(ON) of the switch is maintained at specified values.

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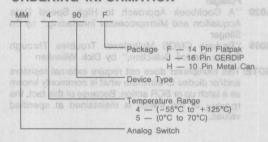
# MM450/451/452/455 MM550/551/552/555 High Voltage Analog Switch

#### GENERAL DESCRIPTION

The MM450, and MM550 series each contain p channel MOS enhancement mode transistors. These devices are useful in airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V<sub>TH</sub> = 2 volts) permits operations with large analog input swings (±10 volts) at low gate voltages (–20 volts).

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

#### ORDERING INFORMATION





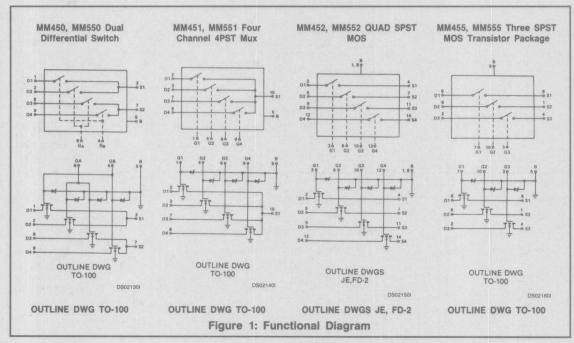
#### FEATURES a lamando hugripuoni T. X anupi not amilio

- Large Analog Input ±10V = 400 100ds vd 16Wolls
- Low Supply Voltage V<sub>BULK</sub> = +10V V<sub>GG</sub> = −20V
- Typical ON Resistance  $V_{IN} = -10V$ ,  $150\Omega$  $V_{IN} = +10V$ ,  $75\Omega$
- Low Leakage Current 200pA @ 25°C
- Input Gate Protection And O foods ed

The IHSO43 was chosen as the third tier of the MUX ecause it will switch the same AC signals as the IHS216 lypically plus and minus 15V) and uses break before make witching. Also power supply quisecent currents are typically 12A. So that no excessive system power is generated total that the logic of the 5043 is such that it can be field licetly to the ENable input (us shown in the figures) with no other logic being required.

Enable input strobing levels

The ENable input acts as an enabling or disabiling pin for the IH6216 when used as a 2 out of 18 channel MUX, however when expanding the MUX to more than 16



#### **ABSOLUTE MAXIMUM RATINGS** (Note 1)

Gate Voltage (VGG)       + 14.5V to -30V         Bulk Voltage (VBULK)       + 14V         Analog Input (VIN)       + 14V to -20V	Operating Temperature  MM450, MM451, MM452, MM45555°C to +125°C  MM550, MM551, MM552, MM5550°C to 70°C
Power Dissipation	Storage Temperature65°C to +150°C Lead Temperature (Soldering, 10sec)300°C

NOTE 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C for FD package and 6.5 mW/°C for TW package.

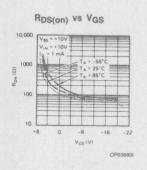
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

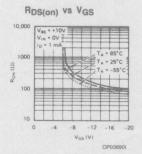
#### **ELECTRICAL CHARACTERISTICS** (per channel unless noted)

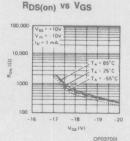
							LIMITS		
SYMBOL	CHARACTERISTIC	TYPE	TEST CONDITIONS		25°C	70°C	125°C	MIN	UNIT
VIN	Analog Input Voltage	All			±10			Max	V
			$V_{DG} = 0$		1.0			Min	
VGS(Th)	Threshold Voltage	All	$I_D = 10\mu A$		3.0			Max	V
RDS(ON)	Drain-Source On Resistance	All	$V_{IN} = -10V$	I <sub>D</sub> = 10mA V <sub>R</sub> = 10V	600		700	Max	Ω
00(014)			V <sub>IN</sub> = +10V	V <sub>GS</sub> = -20V	200		250	Max	Ω
IGBS	Gate Leakage Current	All	$V_{GS} = -25V$ ,	$V_{BS} = V_{DS} = 0$	±5	T WILL	100	Max	nA
I <sub>D(OFF)</sub>	Drain Leakage Current	MM450, MM451 MM452, MM455	$V_{DB} = -25V$ $V_{GB} = V_{SB} = 0$		±0.5		200	Max	nA
		MM550, MM551 MM552, MM555			20	100		Max	nA
		MM450, MM451 MM452, MM455	V <sub>SB</sub> = -25V V <sub>DB</sub> = V <sub>GB</sub> = 0		±0.5		400	Max	nA
IS(OFF)	Source Leakage Current	MM550, MM551 MM552, MM555				100		Max	nA
CDB	Drain-Body Capacitance	All			10	40	IN THE ST	Тур	pF
		MM450, MM550			14			Тур	pF
		MM451, MM551			24			Тур	pF
CSB	Source-Body Capacitance	MM452, MM552			11			Тур	pF
		MM455, MM555	VDB = VGB = V	/ <sub>SR</sub> = 0	11			Тур	pF
		MM450, MM550	f = 1MHz		13			Тур	pF
	0.0.0	MM451, MM551	(Note 1)		8			Тур	pF
CGB	Gate-Body Capacitance	MM452, MM552			9			Тур	pF
		MM455, MM555			9		TO SEE	Тур	pF
CGS	Gate-Source Capacitance	All			5	108218	7000	Тур	pF

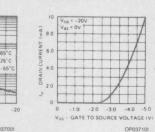
NOTE 1: Typical characteristics not tested in production

#### TYPICAL PERFORMANCE CHARACTERISTICS









DRAIN CURRENT VS GATE

TO SOURCE VOLTAGE

3-179

#### ABSOLUTE MAXIMUM RATINGS (Note 1)

V00- of			

4125°C			
	MMISSS	Mixigs	

NOTE 1. Dissipason rating assumes device in mounted with all leads welded or soldered to printed dirouit board in embiant furnicerature below 70°C. For higher

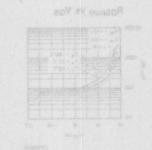
Strasses above hose fisted under Absolute Maximum Ratings may cause permanent damage to the device. There are chear painting only and functional population of the device at those or my other conditions stove those indicated in the operations or the specifications is not implied, Exposure to be solution at my other conditions for extended selections are affect device reliability.

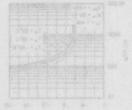
#### ELECTRICAL CHARACTERISTICS (per channel unless noted)

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							V
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	Source Lealunge Current						
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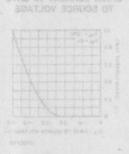
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#### TYPICAL PERFORMANCE CHARACTERISTICS









# Section 4 — Amplifiers — Operational and Special Purpose

Section 4 - Amplifiers - Operational and Special Purpose

# ICH8500/A Ultra Low Input-

# Ultra Low Input-Bias Operational Amplifier

## GENERAL DESCRIPTION

The ICM8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external  $20 \mathrm{k}\Omega$  potentiometer. The input bias current for the inverting and noninverting inputs is 0.1pA maximum for the ICH8500, and 0.01pA maximum for the ICH8500A and are constant over the operating temperature range of  $-25^{\circ}\mathrm{C}$  to  $+85^{\circ}\mathrm{C}$ .

Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential. This is the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.



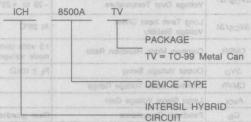
## FEATURES (1) notingered news familia

- Input Diode Protection
- Input Bias Current Less Than 0.01pA (8500A) at All Operating Temperatures
- No Frequency Compensation Required
- Offset Voltage Null Capability
- Short Circuit Protection
- Low Power Consumption

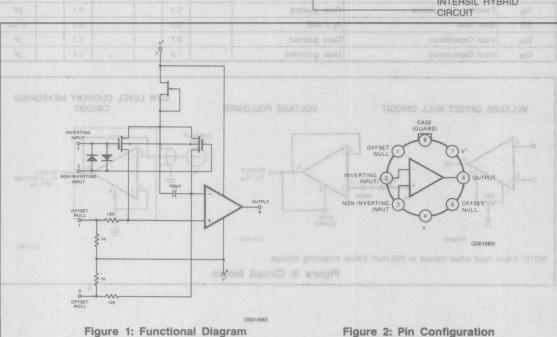
#### **APPLICATIONS**

- Femto Ammeter
- Electrometers
- Long Time Integrators
- Flame Detectors
- pH Meters
- Proximity Detector
- Sample and Hold Circuits

#### ORDERING INFORMATION



(Outline dwg TV)



# S. F.

#### ABSULUTE MAXIMUM HATINGS

Supply Voltage±18V	Operating Ten
Internal Power Dissipation (1)500mW	Lead Tempera
Differential Voltage±0.5V	Output Short (
Storage Temperature65°C to +150°C	a cursa wesigned

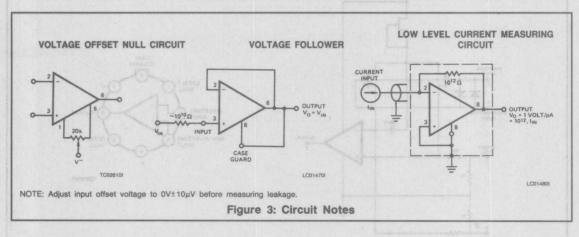
Operating Temperature25°C	to +85°C
Lead Temperature (Soldering, 10sec)	300°C
Output Short Circuit Duration	Indefinite

Note: 1. Rating applies for ambient temperature to +70°C

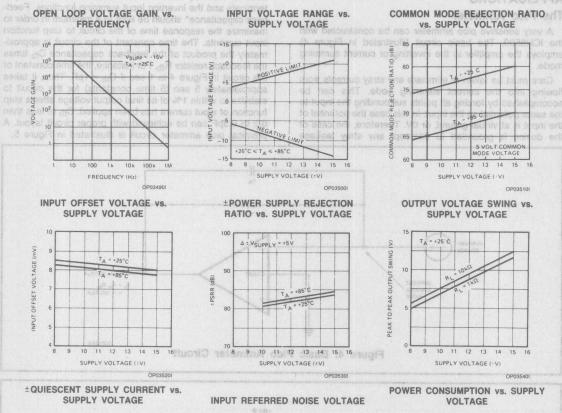
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

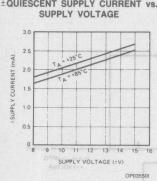
#### ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise specified, VSUPPLY = ±15V) a different and the state of the state o

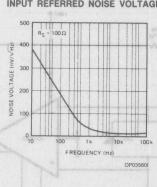
	American	O LOA TEST PERMA	IC	H8500		ICH	18500A	n an e	aro with
SYMBOL	CHARACTERISTICS	TEST	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
IBIAS	Input Bias Current (Inverting and Non-Inverting)	Case at same potential as inputs	Canan Bio		±0.1	-3°e8+	of O	±0.01	рА
Vos	Input Offset Voltage	minore services	Colonia Car	nitrata	±75	poly uno b	DISERTED AND A	±50	mV
	Offset Voltage Adjustment Range	20kΩ Potentiometer	usedciate	±50	uo his	mi wat n	±50	t grite	sidmV d
ΔV <sub>OS</sub> /ΔT	Change in Input Offset Voltage Over Temperature	T 20 10 T 00 0	s sema p	±200	ne cas it flow	Foreing to	±100	o ang Pating	mV
ΔV <sub>OS</sub> /Δt	Long Term Input Offset Voltage Stability	At 25°C	and the	±3.0	ito en	lanya of	±3.0	d beta	mV
CMRR	Common Mode Rejection Ratio	±5 volts common mode voltage		75			75		dB
Δ۷ο	Output Voltage Swing	$R_L \ge 10k\Omega$	±11	19916		±11			٧
CMVR	Common Mode Voltage Range		±10			±10		,	V
AVOL	Large Signal Voltage Gain		20,000	10 <sup>5</sup>		20,000	10 <sup>5</sup>		
Cfb	Feedback Capacitance	Case guarded		0.1			0.1		pF
SR	Slew Rate	$R_L \ge 2k\Omega$	- Armerican	0.5	-	-	0.5	and the same	V/µs
CIN	Input Capacitance	Case guarded		0.7			0.7		pF
CIN	Input Capacitance	Case grounded	F 3 14	1.5	1		1.5		pF



#### TYPICAL PERFORMANCE CHARACTERISTICS







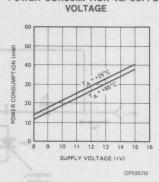


Figure 5: Plop Ammeter Chrouff

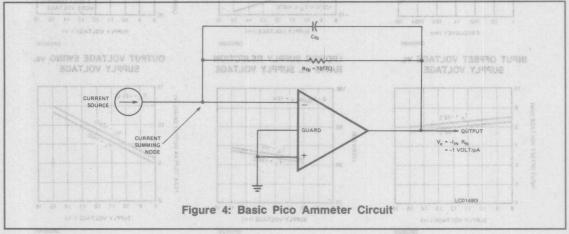
# ICH8500/A

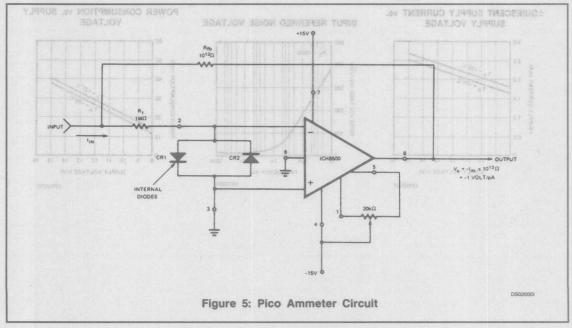
# APPLICATIONS The Pico Ammeter

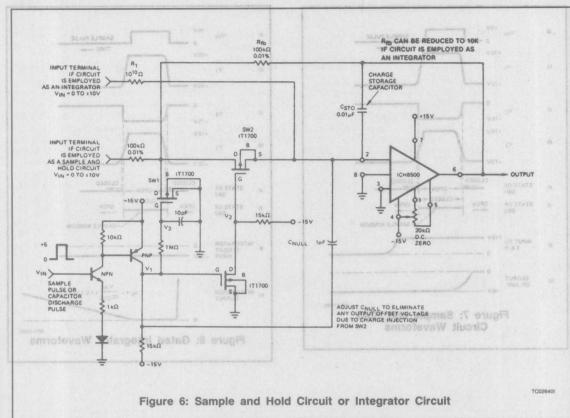
A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 4) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case the potential of the input is at virtual ground, or 0V. Therefore, the case of the device is grounded to intercept any stray leakage

currents that may otherwise exist between the  $\pm 15V$  input terminals and the inverting input summing junctions. Feedback capacitance\* should be kept to a minimum in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance  $C_{fb}$  times the feedback resistor  $R_{fb}$ . For instance, the time constant of the circuit in Figure 4 is 1 sec if  $C_{fb} = 1 p F$ . Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied.  $C_{fb}$  of less than 0.2 to 0.3pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 5.







The internal diodes CR1 and CR2 together with external resistor R1 protect the input stage of the amplifier from voltage transients. The two diodes contribute no error currents, since under normal operating conditions there is no voltage across them.

Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.

#### Sample and Hold Circuit

The basic principle of this circuit (Figure 6) is to rapidly charge a capacitor CSTO to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on CSTO. Since CSTO is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across CSTO should remain constant, causing the output of the amplifier to remain constant as well. However, the voltage across CSTO will decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of CSTO, leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existant (<0.01pA). Note that the voltages on the source, drain and gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a low drift sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA. The rate of change of the voltage across the  $0.01\mu F$  storage capacitor is then 10mV/s sec. In contrast, if an operational amplifier which exhibited an input bias current of 1nA were employed, the rate of change of the voltage across  $C_{STO}$  would be 0.1V/sec. An error build up such as this could not be tolerated in most applications.

Wave forms illustrating the operation of the sample and hold circuit are shown in Figure 7.

#### The Gated Integrator

The circuit in Figure 6 can double as an integrator. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of R1 and  $C_{STO}$ . Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of R1 (Up to  $10^{12}$  ohms) can be employed. This permits the use of small values of integrating capacitor ( $C_{STO}$ ) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 8.



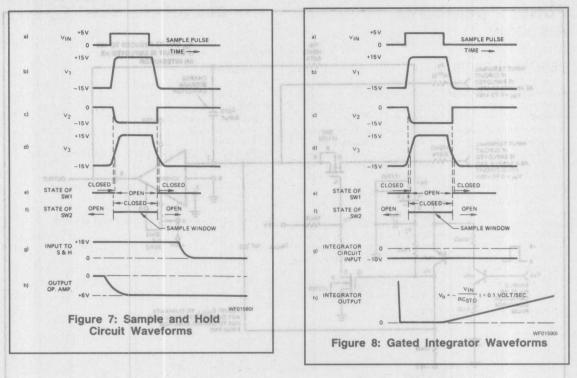


Figure 9: Sample and Hold Circuit or Integrator Circuit

The internal clodes CR1 and CR2 together with external salator R1 protect the input stage of the amplifler from oblige transients. The two clodes contribute no error urrents, since under normal operating conditions there is a voltage across them.

Recobers capacitance is the capacitance between the output and the inventing input reternal of the amplifier.

#### Sample and Hold Circuit

The basic principle of this circuit (Figure 6) is to rejuitly charge a capacitor Corro to a voltage equal to an input of segal. The input signal is then electrically disconnected from the capacitor with the charge still canaining on Corro Since Corro is in the negative feedback loop of the since Corro is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is contain to the amplifier to remain constant as well. However, curput of the amplifier to remain constant as well. However, the voltage across Corro will decay at a tate proportional to the current being injected or taken out of the ourrent comming node of the amplifier. This current can come took four sourcest last age resistance of Corro, leakage current out of the operations SW2, currents due to high bias current on the operational amplifier. If the ICH800A beias current on the operational amplifier is empoyed, this bias current is almost near existant if a OctaAN. Note that the voltages on the

source, drain and gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality espacitor is selected. The net result is a low drift sample and hold circuit.

As an example, suppose the leakage ourrent due to all sources flowing into the current summing node of the sources flowing into the current summing node of the sample and hold circuit is 100ph. The rate of voltage across the 0.01 µF storage capacitor is then 10mV/ sec. In contrast, if an operational amplifier which exhibited an input bias current of 1nA were employed, the rate of change of the voltage scross Garro would be 0.1V/sec. An error build up such as this could not be tolerated in most

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#### GENERAL DESCRIPTION

The ICH8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

There are three models available for up to +30V power supply operation: 2.7 amps @ 24 volt output levels, 2 amps @ 24V and 1 amp @ 24V. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors. For a device operating at lower voltages, see the ICH8515 data sheet.

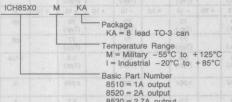
The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate for optimum heat transfer to the metal package. This substrate also provides electrical isolation between amplifiers and metal package.

The I.C. power driver chip has built-in regulators that provide the 741 with typically a ±13V supply.

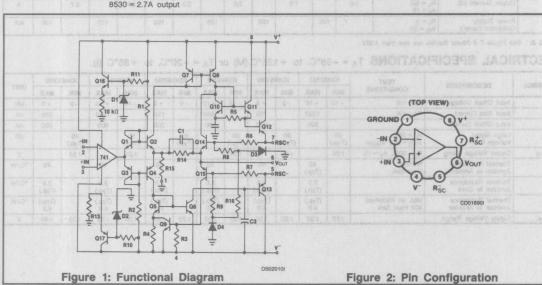
#### **FEATURES**

- Delivers Up to 2.7 Amps @ 24-28V DC (30V Supplies)
- Protected Against Inductive Kick Back With Internal Power Limiting
- Programmable Current Limiting (Short Circuit Protection)
- Package is Electrically Isolated (Allowing Easy
  Heat Sinking)
- Open Loop DC Gain > 100dB
- 20mA Typical Standy Quiescent Current
- Popular 8 Pin TO-3 Package
- Internal Frequency Compensation
- Can Drive Up to 0.1 Horsepower Motors

#### ORDERING INFORMATION



4



# 0688\0688 @INTERSIL

Power Operational

#### ABSOLUTE MAXIMUM RATINGS @ TA = 25°C

Supply Voltage	±32V
Power Dissipation, Safe Operating Are	a See Curves
Differential Input Voltage	±30V
Input Voltage	±15V (Note 1)
Peak Output CurrentSe	e Curves (Note 2)
Output Short Circuit Duration	
(to ground)	ontinuous (Note 2)

Operating Temperature Range M55°C → +125°C
120°C → +85°C
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10sec)300°C
Max Case Temperature150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltages of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltage of ±15V. For lower supply voltages, VINMAX = VSUPP, au tot additions a supply voltage of ±15V. For lower supply voltages of ±15V. For lower supply voltage

Note 2: Ratings apply as long as package dissipation is not exceeded. Device must be mounted on heat sink, see Figures 12 and 16.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS** TA = +25°C. V<sub>SUPPLY</sub> = ±30V (unless otherwise stated)

	roberns	TEST	ICH851	101	#ICH851	OM	ICH8	5201	ICHE	3520M	ICH6	5301	ICH8	530M	2.17.
SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ΔVos/ΔPd	Input Offset Voltage Change with Power Dissipation	Mtd on Wakefield 403 Heat Sink		4 (Typ.)		2 (Typ.)	um pa	4 (Typ.)	s no	2 (Typ.)	e mos	4 (Typ.)	ia sa milgo	2 (Typ.)	mV/Vm
Vos	Input Offset Voltage	R <sub>S</sub> < 10kΩ Pd < 1W	-6	+6	-3	+3	-6	+6	3	+3	-6	+6	-3	+3	mV
IBIAS	Input Bias Current	R <sub>S</sub> < 10kΩ P <sub>d</sub> < 1W		500		250	tors	500	nidia	250	girlo	500	TOWO	250	nA
los	Input Offset Current	R <sub>S</sub> < 10kΩ P <sub>d</sub> < 1W		200		100		200	dns A	100	Cally	200	W TAT	100	nA
AVOL	Large Signal Voltage Gain	R <sub>L</sub> = 20Ω V <sub>O</sub> > 2/3 V <sub>SUPP</sub>	100 (Typ.)		100 (Typ.)		100 (Typ.)		100 (Typ.)	MO	100 (Typ.)	HOR	100 (Typ.)	MIRE	dB
VCMR	Input Voltage Range	Typical	-10	+10	-10	+10	-10	+10	-10	+10	-10	+10	-10	+10	V
CMRR	Common Mode Rejction Ratio	$R_S = 10k\Omega$	70 (Typ.)		70 (Typ.)		70 (Typ.)		70 (Typ.)	Lot L	70 (Typ.)	nn9	70 (Typ.)		dB
PSRR	Power Supply Rejection Ratio	$R_S = 10k\Omega$	77 (Typ.)		77 (Typ.)		77 (Typ.)		77 (Typ.)	e Range	77 (Typ.)	ne T	77 (Typ.)		dB
SR	Slew Rate	$C_L = 3 \text{ pF}, A_V = 1$ $R_L = 10\Omega$ $V_O = 2/3 \text{ V}_{SUPP}$	0.5 (Typ.)		0.5 (Typ.)		0.5 (Typ.)	Sugar Cuest	0.5 (Typ.)	05 - V	0.5 (Typ.)		0.5 (Typ.)		V/µs
VOMAX	Output Voltage Swing	$R_L = 20\Omega$ $A_V = 10$	(R <sub>L</sub> = 30Ω) ± 26V		(R <sub>L</sub> = 30Ω ± 26V		±26V		±26V	luighuo humino	±25V	BB	± 25V		٧
IMAX	Output Current (3)	$A_{L} = 8\Omega$ $A_{V} = 10$	1.0		1.0		2.0	AND NAME OF	2.0	gluo Al	2.7	38	2.7		A
la	Power Supply Quiescent Current	$R_L = \chi$ $V_{IN} = 0V$		125		100		125		100		125		100	mA

NOTE 2: See Figure 7 if Power Suplies are less than ±30V.

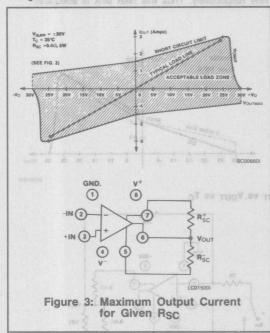
#### **ELECTRICAL SPECIFICATIONS** $T_A = -55^{\circ}C$ . to $+125^{\circ}C$ .(M) or $T_A = +20^{\circ}C$ . to $+85^{\circ}C$ (I).

averno.	DECORIDETON	TEST	ICH	85101	ICH	3510M	ICH	85201	ICH	3520M	ICHE	5301	ICH8	530M	
SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNIT										
Vos	Input Offset Voltage	Pd < 1W	-10	+10	-9	+9	-10	+ 10	-9	+9	-10	+10	-9	+9	MV
IBIAS	Input Bias Current	Pd < 1W		1500		750	1 35	1500		750		1500		750	nA
los	Input Offset Current	(Xamena	100	500	13.3	200		500		200	8/8/1	500		200	nA
AVOL	Large Signal Voltage Gain	$R_L = 20\Omega$ $\Delta V_O = 2/3 V_{SUPP}$	90 (Typ.)		90 (Typ.)		90 (Typ.)	事后	90 (Typ.)	7 00	90 (Typ.)		90 (Typ.)		dB
VOMAX	Output Voltage Swing	$R_L = 20\Omega$ , $A_V = 10$	±24		±24	T PRINT	±24	7	±24	10-9-4	±24	of she	±24		V
RθJA	Thermal Resistance Junction to Ambient	Without Heat Sink		40 (Typ.)	- tuch	40		40		40	(a)	40	0	40	°C/W
R <sub>θ</sub> JC	Thermal Resistance Junction to Case	Y		2.5 (Typ.)		2.5 (Typ.)	9	2.5 (Typ.)		2.5 (Typ.)		2.5 (Typ.)		2.5 (Typ.)	°C/W
R <sub>θ</sub> ЈΑ	Thermal Resistance Junction to Ambient	Mtd. on Wakefield 403 Heat Sink		(Typ.) 4.0		(Typ.) 4.0	Supr	(Typ.) 4.0	10	(Typ.) 4.0	Sta .	(Typ.) 4.0		(Typ.) 4.0	°C/W
VSUPP	Supply Voltage Range		±20	±30	±20	±30	±20	±30	±20	±30	±20	±30	±20	±30	V

Figure 1: Functional Diagram

#### How To Set The Externally Programmable, **Current Limiting Resistors:**

The maximum output current is set by the addition of two external resistors, RSC(+) and RSC(-). Due to the current limiting circuitry, maximum output current is available only when Vo is close to either power supply. As Vo moves away from VSUPPLY, the maximum output current decreases in proportion to output voltage. The curve on the next page shows maximum output current versus output



In general, for a given VO, ISC limit, and case temperature T<sub>C</sub>, R<sub>SC</sub> can be calculated from the equation below for V<sub>O</sub> positive, lour positive.

$$R_{SC} = \frac{(20.6V_{O})^* + 680 - 2.2(T_{C} - 25^{\circ}C)}{|_{SC(LIMIT)}}$$

\*For Vo negative, replace this term with 10.3 (Vo - 1.2) For example, for  $I_O = 1.5A @ V_O = 25V$  and  $T_C = 25^{\circ}C$ ,

$$R_{SC} = \frac{1195}{1500} = 0.797$$

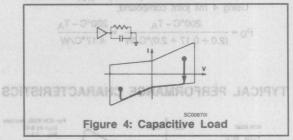
Therefore for this application,  $R_{SC} = 0.82\Omega$  (closest standard value)

When  $0.82\Omega$  is used, ISC @ VO = 0V will be reduced to about 1A. Except for small changes in the "±VO(max) Limit" area, the effects of changing RSC on the IOUT vs VOUT characteristics can be determined by merely changing the IOUT scale on Figure 3 to correspond to the new value. Changes in T<sub>C</sub> move the limit curve bodily up and down.

This internal current limiting circuitry however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 3.



Clearly, as Vo decreases, the lo requirement falls also, more steeply than the IO available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:



Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 24-28VDC motor/actuator, the RSC resistors must be calculated to get proper power delivered to the motor (up to a maximum of 2.7A) and VSUPP set at ±30V. For lower supply and/or output voltages, the maximum output current will follow graphs.

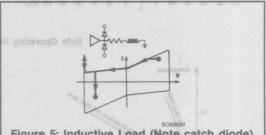


Figure 5: Inductive Load (Note catch diode)

#### NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_D = \frac{T_{J(MAX)} - T_A}{R_{AJC} + R_{ACL} + R_{AJA}}$$

where:

Maximum junction temperature

T<sub>A</sub> = Ambient temperature

 $R_{\theta JC}$  = Thermal resistance from transistor junction to case of package

RACH = Thermal resistance from case to heat sink

R<sub>BHA</sub> = Thermal resistance from heat sink to ambient air And since

T<sub>J</sub> = 200°C for silicon transistors

R<sub>θ,IC</sub> ≈ 2.0°C/W for a steel bottom TO-3 package with die attachment to beryllia substrate header

 $R_{\theta CH} = .045$ °C/W for 1 mil thickness of Wakefield type 120 thermal joint compound

0.09°C/W for 2 mil thickness of type 120

.13°C/W for 3 mil thickness of type 120

.17°C/W for 4 mil thickness for type 120

.21°C/W for 5 mil thickness of type 120

.24°C/W for 6 mil thickness of type 120

 $R_{\theta HA}$  = The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan).  $R_{\theta HA}\cong 2.0^{\circ}\text{C/W}$ . Using 4 mil joint compound,

$$P_D = \frac{200^{\circ}C - T_A}{(2.0 + 0.17 + 2.0)^{\circ}C/W} = \frac{200^{\circ}C - T_A}{4.17^{\circ}C/W}$$

or @ T<sub>A</sub> = 25°C,

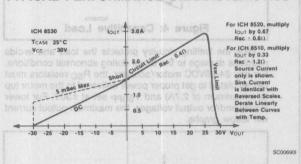
$$\frac{200^{\circ}\text{C} - 25^{\circ}\text{C}}{4.17^{\circ}\text{C/W}} = 42\text{W}$$

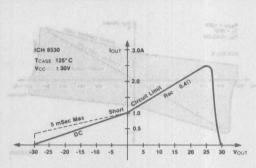
and @ TA = 125°C, - paR bns (+ pod R applies Ismels

$$\frac{200^{\circ}\text{C} - 125^{\circ}\text{C}}{4.17^{\circ}\text{C/W}} = 18\text{W}$$

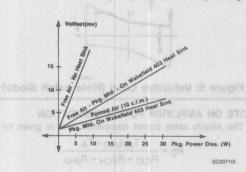
From Figure 6 the worst case steady state power dissipation for an IH8520 ( $R_{SC}=0.62\Omega$ ) is about 30W and 18W respectively. Thus this heat sink is adequate.

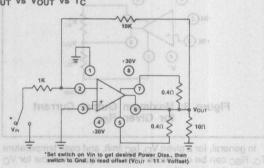
#### TYPICAL PERFORMANCE CHARACTERISTICS



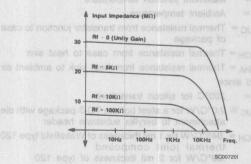


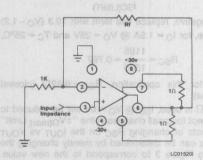
Safe Operating Area; IOUT vs VOUT vs TC



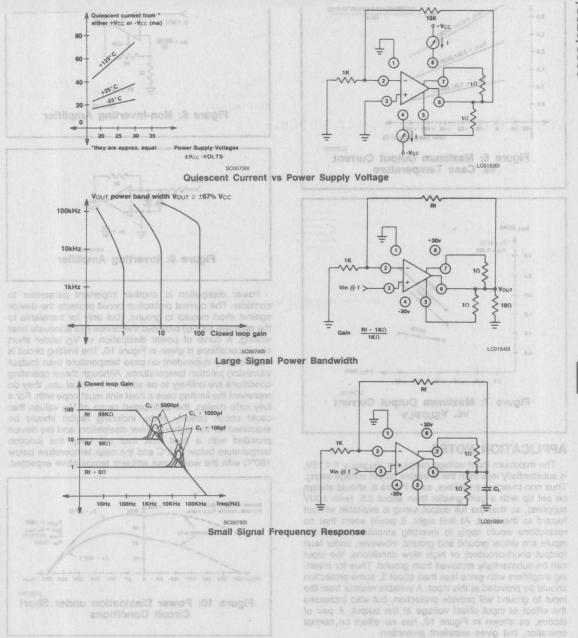


Input Offset Voltage vs Power Dissipation 35 - 058 + 10 V8 05

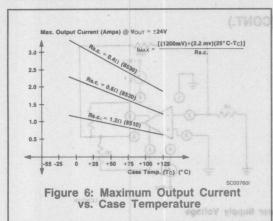


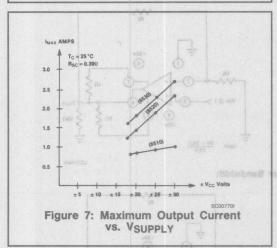


OSY early to seem that time is not input impedance vs Gain vs Frequency of ovince limit but even of in segment



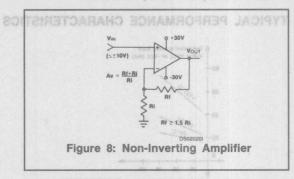


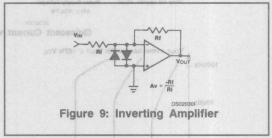




#### APPLICATION NOTES

The maximum input voltage range, for VSUPPLY < ±15V, is substantially less than the available output voltage swing. Thus non-inverting amplifiers, as in Figure 8, should always be set up with a gain greater than about 2.5. (with ±30V supplies), so that the full output swing is available without hazard to the input. At first sight, it would seem that no restrictions would apply to inverting amplifiers, since the inputs are virtual ground and ground. However, under fault (output short-circuited) or high slew conditions, the input can be substantially removed from ground. Thus for inverting amplifiers with gains less than about 5, some protection should be provided at this input. A suitable resistor from the input to ground will provide protection, but also increases the effect of input offset voltage at the output. A pair of diodes, as shown in Figure 10, has no effect on normal operation, but gives excellent protection.





Power dissipation is another important parameter to consider. The current protection circuit protects the device against short circuits to ground, (but only for transients to the opposite supply) provided the device has adequate heat sinking. A curve of power dissipation vs Vo under short circuit conditions is given in Figure 10. The limiting circuit is more closely dependent on case temperature than (output transistor) junction temperatures. Although these operating conditions are unlikely to be attained in actual use, they do represent the limiting case a heat sink must cope with. For a fully safe design, the anticipated range of Vo values that could occur, (steady state, including faults) should be examined for the highest power dissipation, and the device provided with a heat sink that will keep the junction temperature below 200°C and the case temperature below 150°C with the worst case ambient temperature expected.

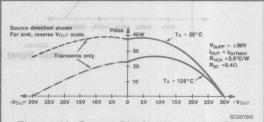
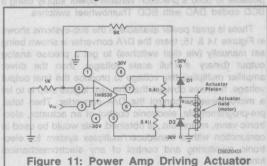


Figure 10: Power Dissipation under Short Circuit Conditions

#### TYPICAL APPLICATIONS

Actuator Driving Circuit (24 - 28 VDC rated)



The gain of the circuit is set to  $\pm 10$ , so a  $V_{IN} = \pm 2.4V$  will produce a  $\pm 24V$  output (and deliver up to 2.7 amps output current). To reverse the piston travel, invert  $V_{IN}$  to  $\pm 2.4V$  and  $V_{OUT}$  will go to  $\pm 2.4V$ . Diodes D1 and D2 absorb the inductive kick of the motor during transients (turn-on or turn-off); their breakdown should exceed 60V.

# Obtaining Up To 5 Amps Output Current Capability By Paralleling Amplifiers

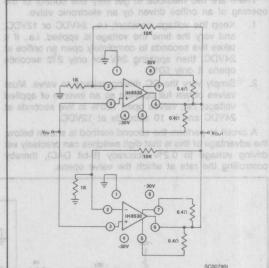
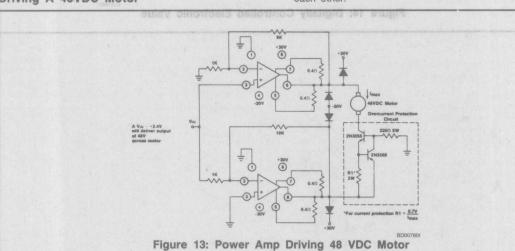


Figure 12: Paralleling Power Amps for Increased Current Capability

This paralleling procedure can be repeated to get any desired output current. However, care must be taken to provide sufficient load to avoid the amplifiers pulling against each other.

### **Driving A 48VDC Motor**



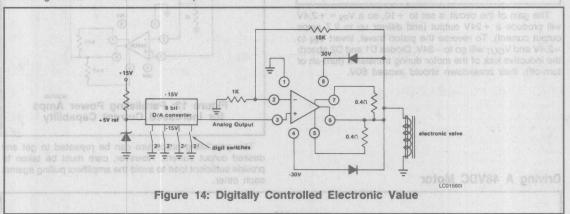
There are two methods to get very fine control of the opening of an orifice driven by an electronic valve.

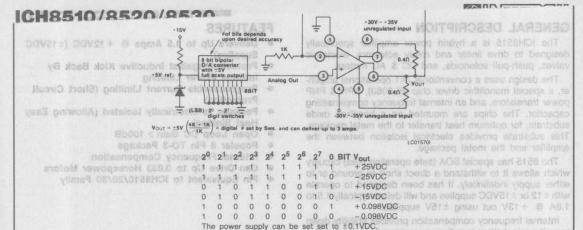
- Keep the voltage constant, i.e., 24VDC or 12VDC, and vary the time the voltage is applied, i.e., if it takes five seconds to completely open an orifice at 24VDC, then applying 24V for only 2½ seconds opens it only 50%.
- Simply vary the DC driving voltage to valve. Most valves obtain full opening as an inverse of applied voltage, i.e., valves open 100% in five seconds at 24VDC and in 10 seconds at 12VDC.

A circuit to perform the second method is shown below; the advantage of this is that digit switches can precisely set driving voltage to 0.2% accuracy (8-bit DAC), thereby controlling the rate at which the valve opens.

BCD coded DAC with BCD Thumbwheel switches.

There is great power available in the sub-systems shown in Figures 14 & 15; there the D/A converter is shown being set manually (via digit switches) to get a precise analog output (binary #x full scale voltage), then the driver amplifier multiplies this voltage to produce the final output voltage. It seems obvious that the next logical step is to let a microprocessor control the D/A converter. Then total, pre-programmable, electronic control of an actuator, electronic valve, motor, etc., is obtained. This would be used in conjunction with a transducer/multiplex system for electronic monitoring and control of any electromechanical function.





#### Figure 15: Digitally Programmable Power Supply

#### HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 (\$10.00 ea.) with a  $R_{\theta HA} = 1.3^{\circ}C/watt$ . A convenient mating connector is also available. Order part number 29-0306 (\$4.50 ea.).

Note: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

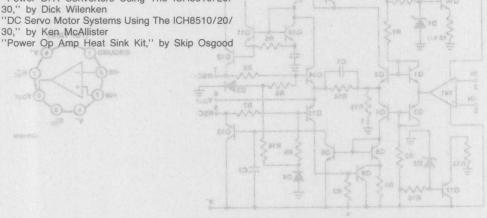
#### **APPLICATION NOTES**

ror runner Applications Assistance, See:

A021 "Power D/A Converters Using The ICH8510/20/ 30," by Dick Wilenken

"DC Servo Motor Systems Using The ICH8510/20/

A029 "Power Op Amp Heat Sink Kit," by Skip Osgood



4-15

## ICH8515

## **Power Operational Amplifier**



#### **GENERAL DESCRIPTION**

The ICH8515 is a hybrid power amplifier specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and an internal frequency compensating capacitor. The chips are mounted on a beryllium oxide substrate, for optimum heat transfer to the metal package. This substrate provides electrical isolation between the amplifier and the metal package.

The 8515 has special SOA (safe operating area) circuitry which allows it to withstand a direct short to ground or to either supply indefinitely. It has been designed to operate with ±12 or ±15VDC supplies and will deliver typically 1.5 to 1.8A @ +13V out using ±15V supplies.

Internal frequency compensation provides stability down to unity gain (either inverting or noninverting) even when using inductive loads.

#### **FEATURES**

- Delivers Up to 1.5 Amps @ +12VDC (±15VDC Supplies)
- Protected Against Inductive Kick Back By Internal Power Limiting
- Programmable Current Limiting (Short Circuit Protection)
- Package Is Electrically Isolated (Allowing Easy Heat Sinking)
- Open Loop DC Gain > 100dB
- Popular 8 Pin TO-3 Package
- Internal Frequency Compensation
- Can Drive Up to 0.033 Horsepower Motors
- Pin Equivalent to ICH8510/20/30 Family

#### ORDERING INFORMATION

PART NUMBER	OUTPUT CURRENT	TEMPERATURE	PACKAGE		
ICH8515MKA	1.5A	-55°C to +125°C	8-Lead TO-3		
ICH8515IKA	1.25A	-25°C to +85°C	8-Lead TO-3		

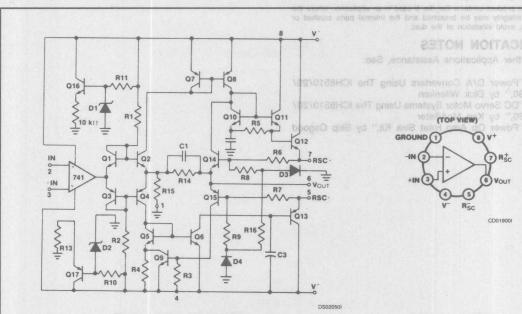
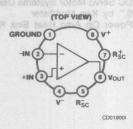


Figure 1: Functional Diagram



HEAT SINK IN Heat sinks are av

Figure 2: Pin Configuration (Outline dwg KA)

#### ABSOLUTE MAXIMUM RATINGS @ TA = 25°C

Supply Voltage		
Differential Input Voltage	P. OA BE.	±30V
Differential Input Voltage	±15V	(Note 1)
Peak Output CurrentSee	Curves	(Note 2)
Output Short Circuit Duration		
(to ground)Co	ntinuous	(Note 2)

Operating Temperature Range M.....-55°C to +125°C 

I.....-25°C to +85°C 

Storage Temperature Range .....-65°C to +150°C 

Lead Temperature (Soldering, 10sec) .....300°C 

Max Case Temperature ......150°C

Note 1: Rating applies to supply voltages of  $\pm 15V$ . For lower supply voltages,  $V_{INMAX} = V_{SUPPLY}$ .

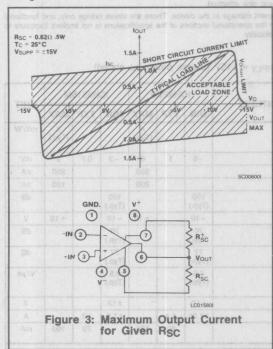
Note 2: Rating applies as long as package dissipation is not exceeded for heat sink attached.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# ELECTRICAL CHARACTERISTICS OPERATING CHARACTERISTICS T<sub>A</sub> = +25°C. V<sub>SUPPLY</sub> = ±15V (unless otherwise stated)

	Section 5 on 164 (appropriate Charles Incompany 178)	人。大	Sep. 100-10	CH851	51	10	H8515	M	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	mV/W nA nA dB V/µs A mA dB MA dB
ΔV <sub>OS</sub> /ΔPd	Input Offset Voltage Change with Power Dissipation	Mtd. on Wakefield 403 Heat Sink	77777	777	4 (Typ.)			2 (Typ.)	mV/V
Vos	Input Offset Voltage	$R_S \le 10k\Omega$ , $Pd < 1W$	-6	1	6	-3	0.7	3	mV
IBIAS	Input Bias Current	$R_S \le 10k\Omega$ , $Pd < 1W$		7	500			250	nA
los	Input Offset Current	$R_S \le 10k\Omega$ , $Pd < 1W$		131	200			100	nA
AVOL	Large Signal Voltage Gain	$R_L = 10\Omega$ , $V_O > 2/3 V_{SUPPLY}$	100 (Typ.)		· · · · · · · · · · · · · · · · · · ·	100 (Typ.)	OND		dB
VCMR	Input Voltage Range	Typical	-10		+10	-10	0	+10	٧
CMRR	Common Mode Rejection Ratio	$R_S = 10k\Omega$	70 (Typ.)		0_	70 (Typ.)	-0	(4)	dB
PSRR	Power Supply Rejection Ratio	$R_S = 10\Omega$	77 (Typ.)		-0	77 (Typ.)	10	47	dB
SR Tovs bas b	Slew Rate	$C_L = 30pF$ , $A_V = 1$ , $R_L = 10\Omega$ $V_O \ge 2/3 \ V_{SUPP}$	0.5 (Typ.)			0.5 (Typ.)			V/µs
$\Delta V_0$	Output Voltage Swing	$R_L = 10\Omega, A_V = 10$	±12		- 4	±12			٧
102Um 21078	Output Current Output Os Volom OC	$R_L = 5\Omega$ , $A_V = 10$	±1.25	1.4	emiser	±1.5	1.8	Strain Fil	А
la No 10 1 Va	Power Supply Quiescent Current	R <sub>L</sub> = ∞, V <sub>IN</sub> = 0V		80	125	0 10	70	100	mA
OPERATIN	G CHARACTERISTICS (continued	d) TA = -55°C to +125°C (N	I) or TA=	= -25°	C to -	+ 85°C	(1).		
Vos	Input Offset Voltage	Pd < 1W	-10	to sut	+10	-9	वाष्ट्र का पर	+9	mV
IBIAS	Input Bias Current	Pd < 1W	100000	120.00	1500	70	diane	750.	nA
los	Input Offset Current	Seria erili			500			200	nA
AVOL	Large Signal Voltage Gain	$R_L = 10\Omega$ , $\Delta V_O = 2/3 \ V_{SUPPLY}$	90 (Typ.)	/3.3	USO I	90 (Typ.)	(1015) 	ase	dB
$\Delta V_0$	Output Voltage Swing	$R_L = 10\Omega$ , $A_V = 10$	±10	0.01	History	±10	and one	- denomina	V
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	Without Heat Sink	T bas VS	= 01	40 (Typ.)	1=0	i not i	40 (Typ.)	°C/W
Rejc	Thermal Resistance Junction to Case	mA = AT	2810. = -	190	3.0 (Typ.)	(51)(	(20.4	3.0 (Typ.)	°C/W
Reja nodor	Thermal Resistance Junction to Ambient		ontol Ores	4.5 (Typ.)	9 00	teallas	4.5 (Typ.)	ani n	°C/W
VSUPPLY	Supply Voltage Range		±11		±17	±11		±17	V

The maximum output current is set by the addition of two external resistors.  $R_{SC(+)}$  and  $R_{SC(-)}$ . Because of the internal power limiting circuitry, the maximum output current is available only when  $V_O$  is close to either power supply. As  $V_O$  moves away from  $V_{SUPPLY}$ , the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.



In general, for a given  $V_O$ , IsC limit, and case temperature  $T_C$ , RSC can be calculated from the equation below for  $V_O$  positive,  $I_{OUT}$  positive.

$$R_{SC} = \frac{(20.6V_{O})^{*} + 680 - 2.2(T_{C} - 25^{\circ}C)}{I_{SC \text{ (limit)}} \text{ in mA}}$$

\*For Vo negative, replace this term with 10.3 (Vo - 1.2)

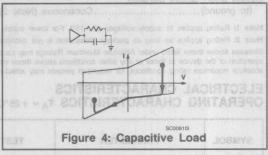
For example, for  $I_O = 1.5A$  @  $V_O = 12V$  and  $T_C = 25$ °C,

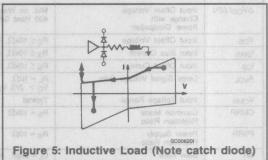
$$R_{SC} = \frac{(20.6)(12) + 680}{1500} = \frac{927.2}{1500} = .618\Omega$$

Therefore for this application,  ${\rm R}_{\rm SC}$  = .62  $\!\Omega$  (closest standard value).

When  $0.62\Omega$  is used, I<sub>SC</sub> @ V<sub>O</sub> = 0V will be reduced to about 1A. Except for small changes in the " $^{\pm}$ V<sub>O(max)</sub> Limit" area, the effects of changing R<sub>SC</sub> on the I<sub>OUT</sub> vs V<sub>OUT</sub> characteristics can be determined by merely changing the I<sub>OUT</sub> scale on Figure 3 to correspond to the new value. Changes in T<sub>C</sub> move the limit curve bodily up and down.

the static load line will be similar to that snown in Figure's. Clearly, as Vo decreases, the Io requirement falls also, more steeply than the Io available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:





Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 12VDC motor/actuator, the R<sub>SC</sub> resistors must be calculated to get proper power delivered to the motor (up to a maximum of 1.5 amps) and V<sub>SUPP</sub> set at ±15V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 3 and 13.

#### NOTE ON AMPLIFIER POWER DISSIPATION

The steady state power dissipation limit is given by

$$P_{D} = \frac{T_{J(MAX)} - T_{A}}{R_{\theta JC} + R_{\theta CH} + R_{\theta HA}}$$

where

T<sub>J</sub> = Maximum junction temperature

T<sub>A</sub> = Ambient temperature

 $R_{ heta JC}$  = Thermal resistance from transistor junction to case of package

 $R_{\theta CH}$  = Thermal resistance from case to heat sink

 $\ensuremath{\mathsf{R}}_{\ensuremath{\mathsf{H}}\ensuremath{\mathsf{A}}} = \ensuremath{\mathsf{Thermal}}$  resistance from heat sink to ambient air And since

T<sub>J</sub> = 150°C for silicon transistors

R<sub>θJC</sub> ≅ 2.0C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate header

.09°C/W for 2 mil thickness of type 120 .13°C/W for 3 mil thickness of type 120

.17°C/W for 4 mil thickness for type 120

.21°C/W for 5 mil thickness of type 120

.24°C/W for 6 mil thickness of type 120

 $R_{\theta HA}$  = The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan).  $R_{\theta HA} \cong 2.0$  °C/W. Using 4 mil joint compound,

$$P_D = \frac{150^{\circ}C - T_A}{2.0^{\circ} + 0.17^{\circ} + 2.0} = \frac{150^{\circ}C - T_A}{4.17^{\circ}C/W}$$

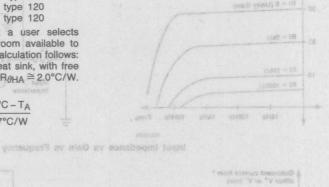
or @ TA = 25°C,

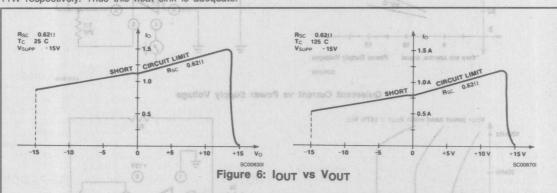
$$\frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{4.17^{\circ}\text{C/W}} = 30\text{W}$$

and @ TA = 125°C,

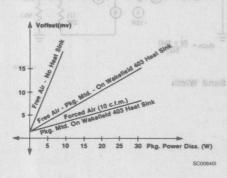
$$\frac{150^{\circ}\text{C} - 125^{\circ}\text{C}}{4.17^{\circ}\text{C/W}} = 6\text{W}$$

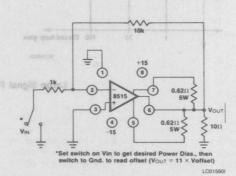
From Figure 6 the worst case steady state power dissipation for the IH8515 (R<sub>SC</sub> =  $0.62\Omega$ ) is about 15W and 11W respectively. Thus this heat sink is adequate.





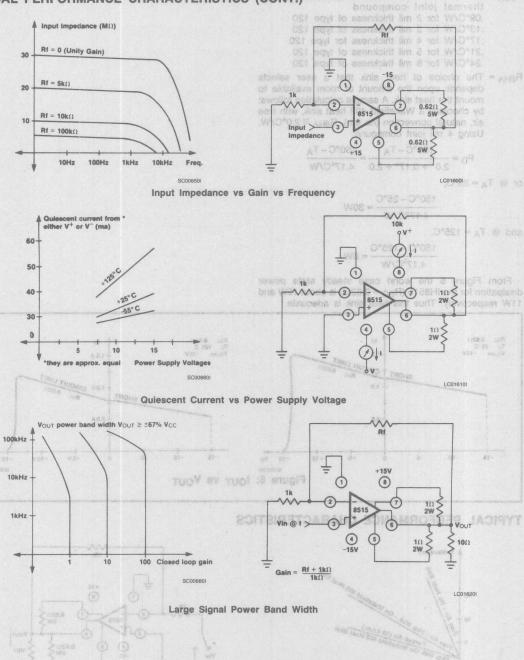
### TYPICAL PERFORMANCE CHARACTERISTICS



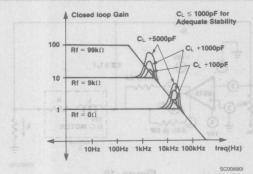


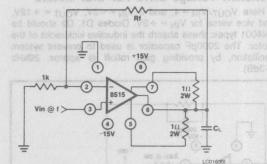
Input Offset Voltage vs Power Dissipation

### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)



#### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)





Small Signal Frequency Response

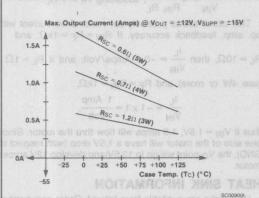


Figure 7: Maximum Output Current vs. Case Temperature

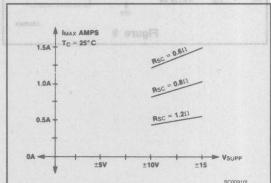
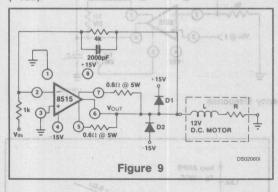
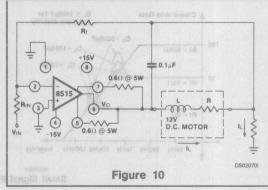


Figure 8: Maximum Output Current vs. V<sub>SUPPLY</sub>

#### Constant voltage Drive For D.C. Motors

Here  $V_{OUT}/V_{IN}=4$ , and if  $V_{IN}=-3V$ ,  $V_{OUT}=+12V$ , and vice versa for  $V_{IN}=+3V$ . Diodes D1, D2 should be 1N4001 types: these absorb the inductive kickbacks of the motor. The 2000pF capacitor is used to prevent system oscillation, by providing gain rolloff @ approx. 20kHz (-3dB).





$$\frac{I_L}{V_{IN}} = -\frac{R_f}{R_{IN}} \cdot \frac{1}{R_L}, \text{ assuming } R_f > > R_L.$$

This circuit allows precisely set motor drive current with op. amp. feedback accuracy. If  $R_{\rm IN}=R_{\rm F}=1{\rm k}\Omega$ , and

$$R_L=10\Omega,$$
 then  $\frac{I_L}{V_{IN}}=-0.1$  Amps/Volt, and if  $R_L=1\Omega$ 

(use 4W or more) and  $R_F = R_{IN} = 1k\Omega$ ,

$$\frac{I_L}{V_{IN}} = -1 \times 1 = \frac{1 \text{ Amp}}{\text{Volt}}.$$

thus if  $V_{IN}$  = 1.5V, 1.5 amps will flow thru the motor. Since one side of the motor will have a 1.5V drop (with respect to GND), the  $V_O$  point will go to 13.5V and develop 12V across motor.

#### HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 (\$10.00 ea.) with a  $R_{\theta HA} = 1.3$ °C/watt. A convenient mating connector is also available. Order part number 29-0306 (\$4.50 ea.).

NOTE: This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

# ICL7605/ICL7606 Commutating Auto-Zero (CAZ) Instrumentation Amplifier

#### GENERAL DESCRIPTION

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10Hz. This is made possible by the unique construction of this new Intersil device, which takes an entirely new design approach to low frequency amplifiers.

Unlike conventional amplifier designs, which employ three op-amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long-term drift phenomena and temperature effects, and a flying capacitor input.

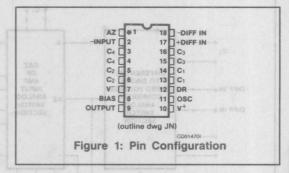
The ICL7605/ICL7606 consist of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

# **BINITERSIL**

#### **FEATURES**

- Exceptionally Low Input Offset Voltage 2μV
- Low Long Term Input Offset Voltage Drift 0.2μV/Year
- Low Input Offset Voltage Temperature Coefficient — 0.05μV/°C
- Wide Common Mode Input Voltage Range 0.3V Above Supply Rail
- High Common Mode Rejection Ratio 100 dB
- Operates at Supply Voltages As Low As ±2V
- Short Circuit Protection On Outputs for ±5V Operation
- Static-Protected Inputs No Special Handling Required
- Compensated (ICL7605) or Uncompensated (ICL7606) Versions



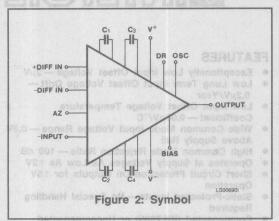
#### ORDERING INFORMATION

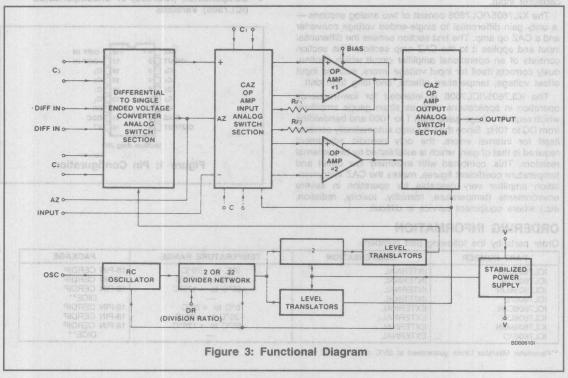
Order parts by the following part numbers:

PART NUMBER	COMPENSATION	TEMPERATURE RANGE	PACKAGE
ICL7605CJN	INTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7605IJN	INTERNAL	-25°C to +85°C	18-PIN CERDIP
ICL7605MJN	INTERNAL	-55°C to +125°C	18-PIN CERDIP
ICL7605/D	INTERNAL		DICE**
ICL7606CJN	EXTERNAL SAGTASAMA V	0°C to +70°C	18-PIN CERDIP
ICL7606IJN	EXTERNAL	-25°C to +85°C	18-PIN CERDIP
ICL7606MJN	EXTERNAL	-55°C to +125°C	18-PIN CERDIP
ICL7606/D	EXTERNAL		DICE**

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

ICL7605/ICL7606





#### ABSOLUTE MAXIMUM RATINGS

ICL7605/ICL7606	@INTERSIL
ABSOLUTE MAXIMUM RATINGS	ELECTRICAL CHARACTERISTICS (CONT.)
	Continuous Total Power Dissipation (Note 4)500mW  Operating Temperature Range:  ICL7605/ICL7606CJN
Differential Input Voltage (+DIFF IN to -DIFF IN) (Note 2)	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latch up. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.
- Note 2: No restrictions are placed on the differential input voltages on either the + DIFF IN or DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.
- Note 3: The outputs may be shorted to ground (GND) or to either supply (V + or V -). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 4: For operation above 25°C ambient temperature, derate 4mW/°C from 500mW above 25°C.

## ELECTRICAL CHARACTERISTICS

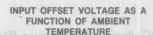
Test Conditions:  $V^+ = +5V$ ,  $V^- = -5V$ ,  $T_A = +25^{\circ}C$ , DR pin connected to  $V^+$  (f<sub>COM</sub> $\simeq$ 160Hz, f<sub>COM1</sub> $\simeq$ 80Hz),  $C_1 = C_2 = C_3 = C_4 = 1 \mu F$ . Test Circuit 1 unless otherwise specified.

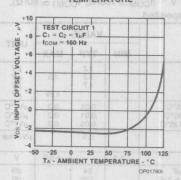
17 a.17 1651	100 of the line of		THE STATE OF THE S		VALUE	PEST CON	8- 1
SYMBOL	PARAMETER		ONDITIONS	MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage	$R_S \le 1k\Omega$ MIL version over temp.	Low Bias Setting Med Bias Setting High Bias Setting Med Bias Setting		±2 ±2 ±7	±5	μV μV μV
ΔV <sub>OS</sub> /ΔT	Average Input Offset Voltage Temperature Coefficient (Note 5)	Low or Med Bias Settings	-55°C > T <sub>A</sub> > +25°C +25°C > T <sub>A</sub> > +85°C +25°C > T <sub>A</sub> > +125°C		0.01 0.01 0.05	0.2 0.2 0.2	μV/°C μV/°C μV/°C
ΔV <sub>OS</sub> /Δt	Long Term Input Offset Voltage Stability	Low or Med Bias Settings			0.5		μV/Yea
CMVR	Common Mode Input Range	434 834 425 43 ADAT 100 V 66414 678	A CAN SER CONTROL	-5.3	May 1965	+5.3	V
CMRR	Common Mode Rejection Ratio	$C_{OSC} = 0$ , DR connected $C_{OSC} = 1 \mu F$ , DR connected $C_{OSC} = 1 \mu F$ , DR connected	to V <sup>+</sup> , C <sub>3</sub> = C <sub>4</sub> = $1\mu$ F and to GND, C <sub>3</sub> = C <sub>4</sub> = $1\mu$ F and to GND, C <sub>3</sub> = C <sub>4</sub> = $10\mu$ F	DAY (O)	94 100 104	o migu	dB dB dB
PSRR 1971	Power Supply Rejection Ratio	CERET VOLTAGE AND	O TURN A BA	POLTAGE	110	29-07-3	dB
-IBIAS	-INPUT Bias Current	Any bias setting, f <sub>C</sub> = 1601 (Includes charge injection		PUMBAO D= e0	0.15	1.5	nA
e <sub>n</sub> (p-p)	Equivalent Input Noise Voltage peak-to-peak	Band Width 0.1 to 10Hz	Low Bias Mode Med Bias Mode High Bias Mode		4.0 4.0 5.0	831	μV μV μV
ēn	Equivalent Input Noise voltage	Band Width 0.1 to 1.0Hz	All Bias Modes	See The	1.7	MIT	μV
Avol	Open Loop Voltage Gain	$R_L = 10k\Omega$	Low Bias Setting Med Bias Setting High Bias Setting	90 90 80	105 105 100	13044	dB dB dB
±VΟ	Maximum Output Voltage Swing	$\begin{aligned} R_L &= 1 M \Omega \\ R_L &= 100 k \Omega \\ R_L &= 10 k \Omega \end{aligned}$	Positive Swing Negative Swing	+4.4	±4.9 ±4.8	-4.5	V V V
GBW	Bandwidth of Input Voltage Translator	$C_3 = C_4 = 1 \mu F$	All Bias Modes	S ING.	10	HON L	Hz
fCOM.	Nominal Commutation Frequency	C <sub>OSC</sub> = 0	DR Connected to V <sup>+</sup> DR Connected to GND	· 基本一个	160 2560	01	Hz Hz
fCOM1	Nominal Input Converter Commutation Frequency	C <sub>OSC</sub> = 0	DR Connected to V <sup>+</sup> DR Connected to GND	and the second	80 1280	John Co.	Hz Hz
V <sub>BH</sub> V <sub>BM</sub> V <sub>BL</sub>	Bias Voltage required to set Quiescent Current	Low Bias Setting Med Bias Setting High Bias Setting		V + -0.3 V - + 1.4 V0.3	V <sup>+</sup> GND V <sup>-</sup>	V + + 0.3 V + - 1.4 V - + 0.3	V
IBIAS	Bias (Pin 8) Input Current				±30		pA

4) 500m/A	stal Power Dissipation (Note:		of *\	VALUE	by ylaqq	a leto	
SYMBOL	PARAMETER	DET gridding TEST CONDITIONS of (8-7V)	MIN	TYP	MAX	UNIT	
IDR + OF O	Division Ratio Input	$V^+ - 8.0 \le V_{DR} \le V^+ + 0.3 \text{ volt}$		±30	AIS TU	рА	
VDRH VDRL	DR Voltage required to set Oscillator division ratio	Internal oscillator division ratio 32 Internal oscillator division ratio 2	V + -0.3 V + -8	stoV :	V <sup>+</sup> + 0.3 V <sup>+</sup> - 1.4		
RAS	Effective Impedance of Voltage Translator Analog Switches	at (Note 3)Unitrified		30	tsO to	kΩ	
ISUPP	Supply Current	High Bias Setting Med Bias Setting Low Bias Setting	e another	03 1.7		mA mA mA	
v+_v-bas.b	Operating Supply Voltage Range	High Bias Setting Med or Low Bias Setting	10150		10	V	

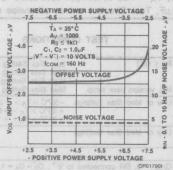
Note 5: For Design only, not 100% tested.

#### TYPICAL PERFORMANCE CHARACTERISTICS

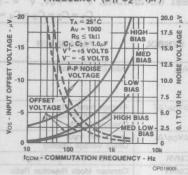




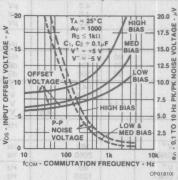
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A **FUNCTION OF SUPPLY VOLTAGES** 



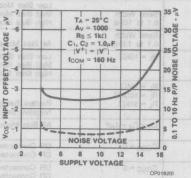
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A **FUNCTION OF COMMUTATION** FREQUENCY (C<sub>1</sub>, C<sub>2</sub> =  $1\mu$ F)



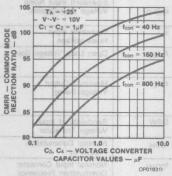
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A **FUNCTION OF COMMUTATION** FREQUENCY (C<sub>1</sub>, C<sub>2</sub> = 0.1  $\mu$ F)



INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V +-V-)

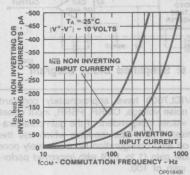


COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED **VOLTAGE CONVERTER CAPACITORS** 

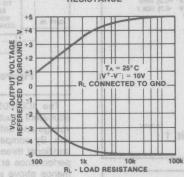


# CL7606

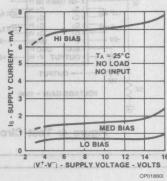
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



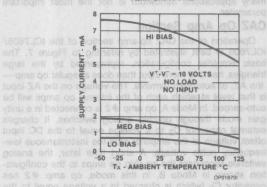
FUNCTION OF OUTPUT LOAD RESISTANCE



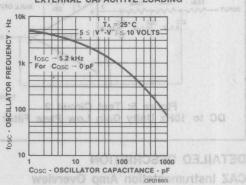
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



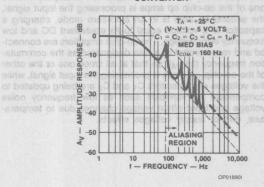
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



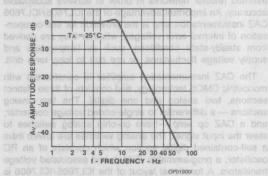
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

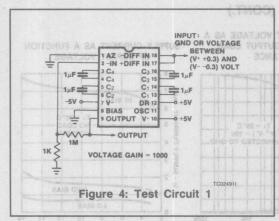


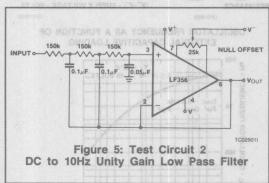
AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE state and to aspect CONVERTER the to sugar and



FREQUENCY RESPONSE OF THE 10Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).





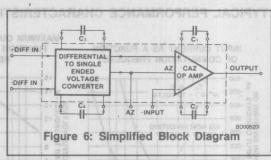


### **DETAILED DESCRIPTION**

### **CAZ Instrumentation Amp Overview**

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op-amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation of internal error voltages, whether they are derived from steady-state conditions, such as temperature and supply voltage fluctuations, or are due to long term drift.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 6.



The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20Hz maximum). However in many applications bandwidth is not the most important parameter.

#### CAZ Op Amp Section

Operation of the CAZ op-amp section of the ICL7605/ ICL7606 is best illustrated by referring to Figure 7. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor Co to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous lowfrequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (fcom), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C1 and C2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

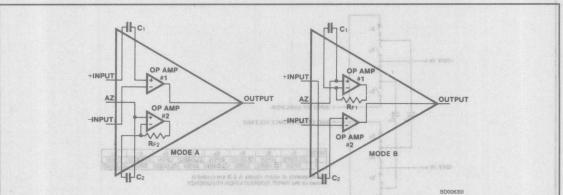


Figure 7: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

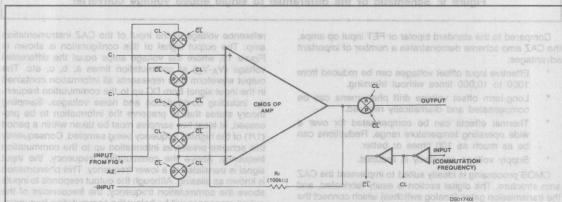


Figure 8: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

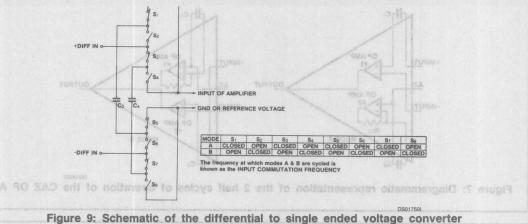


typical input offset voltages of itemy, and ultra-low leakage currents, typically fpA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 6. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and times switches are closen. Each analog switch sonsists of a P-channel translator in parallel with an M-channel translator.

DIFFERENTIAL-TO-SINGLE-ENDED UNITY

An coatized scrematic of the winting converter violate in above in Figure 9. The mode of operation is quite simple, amolying two capacitions and eight switches are arranged so that four are open and four are closed. The total course of the capacitors across the differential input, and the other from a ground or



Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

- Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
- Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
- Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
- Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. The CMOS structure provides the CAZ op-amp with open-loop gains of greater than 100dB, typical input offset voltages of ±5mV, and ultra-low leakage currents, typically 1pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 8. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

#### DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of the voltage converter block is shown in Figure 9. The mode of operation is guite simple. involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or

reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 10, where the voltage steps equal the differential voltage (VA-VB) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequencv. including commutation and noise voltages. Sampling theory states that to preserve the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency being sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is translated to a lower frequency. This phenomenon is known as aliasing. Although the output responds to inputs above the commutation frequency, the frequencies of the output responses will be below the commutation frequency.

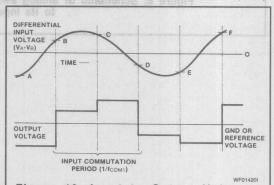
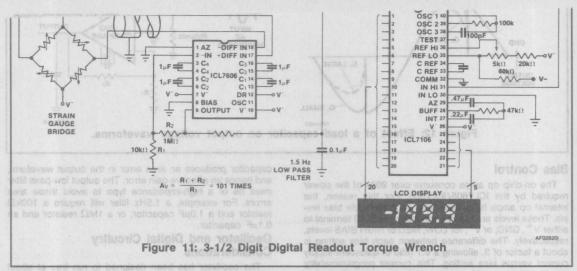


Figure 10: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.



The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have a finite ON impedances of  $30k\Omega$ , plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors  $C_3$  and  $C_4$  must be about  $1\mu F$  to preserve signal translation accuracies to 0.01%. The  $1\mu F$  capacitors, coupled with the  $30k\Omega$  equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is down approximately 3dB at 10Hz.

#### **APPLICATIONS**

# Using the ICL7605/ICL7606 to Build a Digital Readout Torque Wrench

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting it to a single-ended voltage referenced to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter which drives the LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL 7106

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of

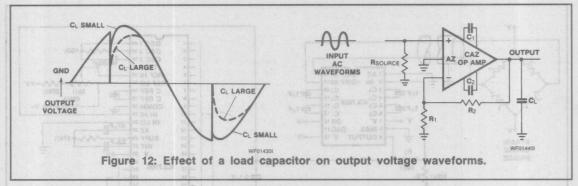
the A/D. In order to set the full-scale reading, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp must be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale, the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2mA. The accuracy is limited only by resistor ratios and the transducer.

# SOME HELPFUL HINTS Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Figure 4 and 5 (Test Circuits) provide a convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be a high-input impedance RC type — not simply a capacitor across the feedback resistor R2. Resistor and capacitor values of about 100k $\Omega$  and 1.0 $\mu$ F are necessary so that the output load impedance on the CAZ op-amp is greater than 100k $\Omega$ .



#### **Bias Control**

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606. For this reason, the internal op amps have externally- programmable bias levels. These levels are set by connecting the BIAS terminal to either V+, GND, or V-, for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of quiescent supply current versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

#### **Output Loading (Resistive)**

With a 10k $\Omega$  load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as  $2k\Omega$ .

However, with loads of less than  $50 k\Omega$ , the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly  $50 k\Omega$  each. Thus the open-loop gain is 20dB less with a  $2 k\Omega$  load than it would be with a  $20 k\Omega$  load. Therefore, for high gain configurations requiring high accuracy, an output load of  $100 k\Omega$  or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked. This is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

### Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 12. It can be seen that the effect of a large load

capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5Hz filter will require a  $100 k\Omega$  resistor and a  $1.0 \mu F$  capacitor, or a  $1 M\Omega$  resistor and an  $0.1 \mu F$  capacitor.

# Oscillator and Digital Circuitry Considerations

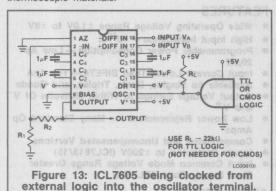
The oscillator has been designed to run free at about 5.2kHz when the OSC terminal is open circuit, If the full divider network is used, this will result in a nominal commutation frequency of approximately 160Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always, at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V +) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 13) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V + supply is +5V (±10%) and the logic driver also operates from a similar voltage supply. The reason for this requirement is that the logic section (including the oscillator) operates from an internal -5V supply, referenced to V + supply, which is not accessible externally.

#### Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the

same temperature, small thermoelectric voltages will be produced, generally about  $0.1\mu V/^{\circ}C$ . However, these voltages can be several tens of microvolts per  $^{\circ}C$  for certain thermocouple materials.



In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep the ICL7605/ICL7606 away from equipment which dissipates heat.

### **Component Selection**

The four capacitors (C<sub>1</sub> thru C<sub>4</sub>) should each be about  $1.0\mu F$ . These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene types are the best for C<sub>3</sub> and C<sub>4</sub>, although Mylar may be adequate for C<sub>1</sub> and C<sub>2</sub>.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at  $1.0 \mu F$  and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

#### **Commutation Voltage Transient Effects**

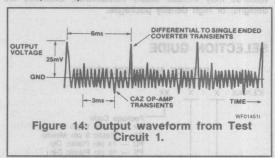
Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10Hz. The is due to the finite

switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest inband frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op-amps are typically in the 10pr range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors  $C_1$  and  $C_2$  must have values of at least  $10,000 \times 10 \, \text{pF}$ , or  $0.1 \, \mu \text{F}$  each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0pA at an ambient temperature of 25°C.

The output waveform in Figure 4 (with no input signal) is shown in Figure 14. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7mV are amplified by a factor of less than 1000.



### **Layout Considerations**

Care should be exercised in positioning components on the PC board particularly the capacitors  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$ , which must all be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

4

# GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1.0V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100µA, or 10µA, with no external components. This results in power consumption as low as 20 µW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of .01pA/,/Hz, and 1012Ω input impedance. These features optimize performance in very high source impedance applications.

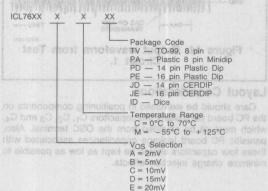
The inputs are internally protected and require no special handling procedures. Outputs are fully protected against short circuits to ground or to either supply. The state of the supply of the state of the

AC performance is excellent, with a slew rate of 1.6V/us. and unity gain bandwidth of 1MHz at IO = 1mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

#### SELECTION GUIDE

#### **DEVICE NOMENCLATURE**



#### FEATURES

- Wide Operating Voltage Range ±1.0V to ±8V
- High Input Impedance 1012 \O
- Programmable Power Consumption Low As 20 UW
- Input Current Lower Than BIFETs Tvp 1pA
- Available As Singles, Duals, Triples, and Quads
- Output Voltage Swings to Within Millivolts Of V" and V+
- Low Power Replacement for Many Standard Op Amps
- Compensated and Uncompensated Versions
- Inputs Protected to ±200V (ICL7613/15)
- Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)

### APPLICATIONS

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers and subsequent blove of another and
- Medical Instruments of beeplane ed bluode .
- High Impedance Buffers

#### SPECIAL FEATURE CODES

- INTERNALLY COMPENSATED EXTERNALLY COMPENSATED
- HIGH QUIESCENT CURRENT (1mA) = INPUT PROTECTED TO ±200V
- L = LOW QUIESCENT CURRENT (10µA)
  - M = MEDIUM QUIESCENT CURRENT (100 µA)
  - = OFFSET NULL CAPABILITY 0
  - PROGRAMMABLE QUIESCENT CURRENT
    - EXTENDED CMVR

ICL7611XCTV

ICL7611XMTV

ICL7612XCPA ICL7612XCTV

ICL7612XMTV

ICL7613XCPA ICL7613XCTV

ICL7613XMTV

	NUMBER OF	ASSIGNAN	1954	PA	CKAGE TYP	E AND SUFF	IX	30	WW.
BASIC PART	OP-AMPS IN PACKAGE, AND SPECIAL	8-LEAL	TO-99	8-PIN MINIDIP	8-PIN SOIC	PLASTIC DIP (1)	CERAMI	C DIP (1)	DICE
NUMBER	FEATURES (SEE ABOVE)	0°C to +70°C	-55°C to + 125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	-55°C to +125°C	DICE 2181 DI
ICL7611 ICL7612 ICL7613 ICL7614 ICL7615	SINGLE OP-AMP: C, O, P C, O, P, V C, I, O, P E, M, O E, I, M, O	ACTV BCTV DCTV	AMTV BMTV	ACPA BCPA DCPA	DCPA DCBA				D/D
ICL7621	DUAL OP-AMP: C, M	ACTV BCTV DCTV	AMTV BMTV	ACPA BCPA DCPA	, Nie				D/D
ICL7622	DUAL OP-AMP: C, M, O			edoegnoo T n	q»	ACPD BCPD DCPD	ACJD BCJD DCJD	AMJD BMJD	D/D
ICL7631 ICL7632	TRIPLE OP-AMP: C, P P(3)			we entitue)		CCPE ECPE	CCJE ECJE	CMJE	E/D
ICL7641 ICL7642	QUAD OP-AMP: C, H C, L	.1	1740 P	的	,ruo ),ui-	CCPD ECPD	CCJD ECJD	CMJD	E/D

NOTES: 1. Duals and quads are available in 14 pin DIP package, triples in 16 pin only.

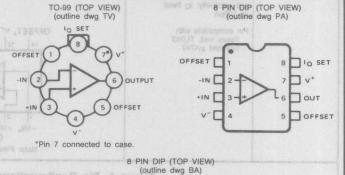
2. Ordering code must consist of basic part number and package suffix, e.g., ICL7611BCPA.

3. ICL7632 is not compensatable. Recommended for use in high gain circuits only. \*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

DEVICE DESCRIPTION PROPERTY TO-99 (TOP VIEW) (outline dwg TV)

offset null capability

and external IQ control



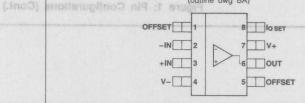
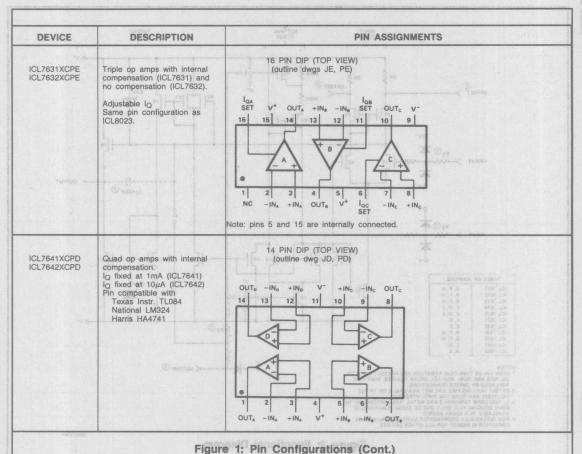
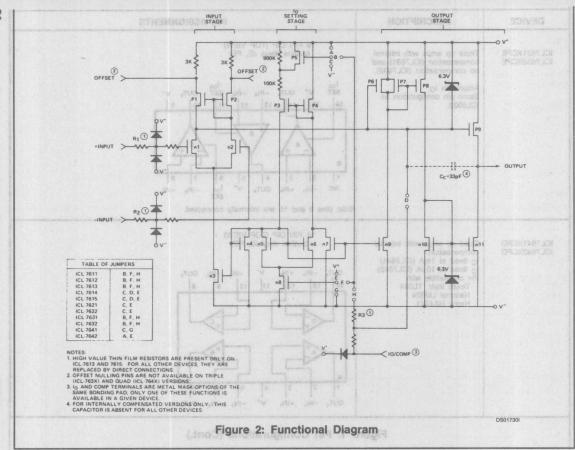


Figure 1: Pin Configurations

ICL76XX

	DESCR	III LION	ement transaction	MAG	PIN	ASSIGNME	NTS
ICL7614XCPA ICL7614XCTV ICL7614XMTV	Fixed IQ (100µ) compensation, a null capability	A), external and offset	8-91M	TO-99 (TOP (outline dwg	VIEW)	DARLI-8	8 PIN DIP (TOP VIEW) (outline dwg PA)
ICL7615XCPA ICL7615XCTV ICL7615XMTV	0°C to		01 010 0107.4	COMP		SOIC-8	
ONG .			OFFSET	7T>	7° ∨* 6 OUTP	VTOA VTOB OF VTOG	-IN 2 - 7 V+
			+IN (	30	5 OFFSET	ACTV BCTV DCTV	V- 4 5 OFFSET
GLM/ GLMS	ACJD RCJD	AGPD RGPD	*F	in 7 connected	d to case.		OUAL OF AMPL
ICL7621XCPA ICL7621XCTV ICL7621XMTV	Dual op amps compensation; I at 100 µA Pin compaptible Texas Inst. T Motorola MC Raytheon RC	with (L082 1458 44558	also agin o alsobro 3010	2	7 OUT <sub>8</sub>	Ne ni eidelleve id to telanor A .eldetsene mensug etim	gmod ton di Salt Jai la
	Annual Control of the		*F	in 8 connected			
ICL7622XCPD	Dual op amps			in 8 connected	14 PI	N DIP (TOP	
ICL7622XCPD  WEV SON (AF DWD	compensation a null capability; lat 100μA Pin compatible Texas Inst. T	nd offset Q fixed with L083		eniliuo) () 98-CV	14 PI (out)	line dwgs JD,	PD)  a V* OFFSET <sub>B</sub> 9 8
(WBIY SOT)	compensation a null capability; lat 100 µA  Pin compatible	nd offset Q fixed with 'L083 47	OP VIEW)	t) 98-OT enilipo)	14 PI (out)	line dwgs JD,	PD)  8 V* OFFSET  9 8
(TOP VIEW) dwg PA)	compensation a null capability; lat 100μA  Pin compatible Texas Inst. T Fairchild μΑ7.	nd offset Q fixed with 'L083 47	OF VIEW)	t) 98-OT enilipo)	14 PI (out)	line dwgs JD,	PD)  a V* OFFSET  9 8
(TOP VIEW) dwg PA)	compensation a null capability; li at 100 µA Pin compatible Texas Inst. T Fairchild µA7	ind offset Q fixed with L083 47	PO VIEW)	OFFS 14	14 PI (out)  ET <sub>A</sub> V* OU'  13 12  A  A  OFFSE	TA N/C OUT  11 10  4 5  V-  ETA OFFSE	PD)  a V* OFFSET  9 8  +INa -INa
OWG PA)	compensation a null capability; li at 100 µA  Pin compatible Texas Inst. T Fairchild µA7	ind offset Q fixed with L083 47	PRIVATE VICTOR VIEWS	OFFS 14	14 Pl (out)  ETA V* OU  13 12  A  A  Pl (out)  A  Pl (out	TA N/C OUT  11 10  4 5  V  ETA OFFSE d 13 are inte	PD)  a V* OFFSETa  9 8





۲.		

Input Voltag	je		V	0		3V	Continuous Power	Dissipation @25°C	Above 25°C derate as below:
Differential	Input V	oltage	2]±[(V <sup>-1</sup> 2] ICL761 ±[(V <sup>+</sup>	+0 3/15 +20	V to V <sup>+</sup> +200 $\cdot 3$ ) – (V <sup>-</sup> –0.3) Only	]V 	TO-99 8 Lead Minidip 14 Lead Plastic 14 Lead Cerdip	250mW 250mW 375mW 500mW	2mW/°C 2mW/°C 3mW/°C 4mW/°C
Duration of	Output	Short	Circuit <sup>[3]</sup>		Unlimite		16 Lead Plastic	375mW	3mW/°C
							16 Lead Cerdip Storage Temperate Operating Temperate	ure Range	4mW/°C -65°C to +150°C
		76 72 68		76 72 68	80 63 76 72		M Series C Series Lead Temperature		0°C to +70°C

#### Notes:

- 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- 2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
- 3. The outputs may be shorted to ground or to either supply, for V<sub>SUPP</sub> ≤ 10V. Care must be taken to insure that the dissipation rating is not exceeded.

# **ELECTRICAL CHARACTERISTICS (761X and 762X ONLY)**

(VSUPPLY = ±5.0V, TA = 25°C, unless otherwise specified.)

DVMDOL	TOO DADAM	001	TEST CONDITIONS	Mil ent.	76XX	A		76XXE	3	bones	HAUT		
SYMBOL	PARAM	EIER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage	e 10.0	$R_S \le 100k\Omega$ , $T_A = 25^{\circ}C$ $T_{MIN} \le T_A \le T_{MAX}$	WAY S	# = T	2 3			5 7	(reitig	mA 10	15 20	mV
ΔV <sub>OS</sub> /ΔT	Temperature Coeff	icient of Vos	$R_S \le 100k\Omega$		10			15			25		μV/°C
los	Input Offset Currer	nt	$T_A = 25^{\circ}C$ $\Delta T_A = C_{(2)}$ $\Delta T_A = M_{(2)}$	DI = 100	0.5	30 300 800		0.5	30 300 800	(6)	0.5	30 300 800	pA
IBIAS	Input Bias Current	31.0 3.1	$T_A = 25^{\circ}C$ $\Delta T_A = C$ $\Delta T_A = M$		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
VCMR	Common Mode Vo (Except ICL7612)	oltage Range	$I_Q = 10\mu A^{(1)}$ $I_Q = 100\mu A$ $I_Q = 1mA^{(1)}$	±4.4 ±4.2 ±3.7	Aug 003	= 0) = 0; = 0;	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7	a! es		V
VCMR	Extended Common		$I_Q = 10\mu A$	±5.3	double)	-07	±5.3		(8) <sub>101</sub>	±5.3	arional		
	Range (!CL7612 C	01	I <sub>Q</sub> = 100μA	+5.3	Augo:	= ot	+5.3 -5.1			+5.3			٧
50 (d 8 c	on many Brade (Brass)	0 P	I <sub>Q</sub> = 1mA	+5.3	Ann	01	+5.3			+5.3			
Vout	Output Voltage Sw		(1) $I_Q = 10\mu A$ , $R_L = 1M\Omega$ $T_A = 25^{\circ}C$ $\Delta T_A = C$ $\Delta T_A = M$	±4.9 ±4.8 ±4.7	ry Too (76)	10S	±4.9 ±4.8 ±4.7	er:	IARI	±4.9 ±4.8 ±4.7	JA	PIRT	LEC
	1/7612/7613 on 76XXB	PRINCIPLE PRINCI	$I_Q$ = 100 μA, $R_L$ = 100 kΩ $T_A$ = 25°C $\Delta T_A$ = C	±4.9 ±4.8	0 00		±4.9 ±4.8	A.	Acqui	±4.9 ±4.8	VO.	T Y	V
	LAM TYP MAL		$\Delta T_A = M$	±4.5			±4.5	MARI	P.	±4.5		JOS	WAS .
	2	\$ 8	(1) $I_Q = 1 \text{mA}$ , $R_L = 10 \text{k}\Omega$ $T_A = 25^{\circ}\text{C}$ $\Delta T_A = C$ $\Delta T_A = M$	±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0	opsic	W Jack	±4.5 ±4.3 ±4.0			

# ELECTRICAL CHARACTERISTICS (761X and 762X ONLY) (CONT.)

		Continuous Pow	/8/	76XX/	Α		76XXE	3 01	V si	UNIT		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Avol	Large Signal Voltage Gain	$V_{O} = \pm 4.0V, R_{L} = 1M\Omega$ $I_{Q} = 10\mu A^{(1)}, T_{A} = 25^{\circ}C$ $\Delta T_{A} = C$ $\Delta T_{A} = M$	86 80 74	104	0) (0 (2) - (1 (2) - (1)	80 75 68	104	[2] [2]	80 75 68	104		InmattiC InotettiC
W/°C W/°C to + 150°C	500mW 4a	$V_O = \pm 4.0V$ , $R_L = 100k\Omega$ $I_O = 100\mu A$ , $T_A = 25^{\circ}C$ $\Delta T_A = C$ $\Delta T_A = M$	86 80 74	102		80 75 68	102	PAIO 1	80 75 68	102	O io	dB
to +125°C to +70°C	- 85°C 9°C re (Soldering, 16sec)	$\begin{aligned} &V_O=\pm 4.0V, \ R_L=10k\Omega\\ &I_Q=1mA^{(1)}, \ T_A=25^{\circ}C\\ &\Delta T_A=C\\ &\Delta T_A=M \end{aligned}$	80 76 72	83		76 72 68	83		76 72 68	83		
GBW	Unity Gain Bandwidth end agrillar sends dis seed! To siveb	$I_Q = 10\mu A^{(1)}$ $I_Q = 100\mu A$ $I_Q = 1mA^{(1)}$	nay sa nose i	0.044 0.48 1.4	A mun	TERM C	0.044 0.48 1.4	tasiani ase or	rtt te e	0.044 0.48 1.4	wode :	MHz
RIN-	Input Resistance	E devido rehability.	lette V	1012	istraid, lat	Kanaba	1012	holikini	to prin	1012	sixem:	Ω
CMRR	Common Mode Rejection Ratio	$R_S \le 100 k\Omega$ , $I_Q = 10 \mu A^{(1)}$ $R_S \le 100 k\Omega$ , $I_Q = 100 \mu A$ $R_S \le 100 k\Omega$ , $I_Q = 1 m A^{(1)}$	76 76 66	96 91 87	11 Day	70 70 60	96 91 87	trup of	70 70 60	96 91 87	от едис	dBT.
PSRR	Power Supply Rejection Ratio	$R_S \le 100 k\Omega$ , $I_Q = 10 \mu A^{(1)}$ $R_S \le 100 k\Omega$ , $I_Q = 100 \mu A$ $R_S \le 100 k\Omega$ , $I_Q = 1 m A^{(1)}$	80 80 70	94 86 77	when	80 80 70	94 86 77	DALES DIES	80 80 70	94 86 77	MH.	dB
en	Input Referred Noise Voltage	$R_S = 100\Omega$ , $f = 1kHz$		100	-	-	100			100	1	nV/√Hz
in Mu	Input Referred Noise Current	$R_S = 100\Omega$ , $f = 1kHz$	IGMO	0.01	87		0.01	TRING	MAG	0.01	1	pA/√Hz
ISUPPLY	Supply Current (Per Amplifier)	No Signal, No Load IQ SET = +5V(1) IQ SET = 0V IQ SET = -5V(1)	× AT ,	0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5	V too	0.01 0.1 1.0	0.02 0.25 2.5	mA
V <sub>01</sub> /V <sub>02</sub>	Channel Separation	A <sub>VOL</sub> = 100		120	7.8	55,0	120	210/03/2012	9 9100	120		dB
SR (0)	Slew Rate <sup>(3)</sup>	A <sub>VOL</sub> = 1, C <sub>L</sub> = 100pF V <sub>IN</sub> = 8Vp-p		(g)D =	ATA ATA			Street	0 100			EOI
	9.7 09 0.7 00a 00a	$I_Q = 10\mu A^{(1)}, R_L = 1M\Omega$ $I_Q = 100\mu A, R_L = 100k\Omega$ $I_Q = 1mA^{(1)}, R_L = 10k\Omega$		0.016 0.16 1.6	ATA ATA		0.016 0.16 1.6	Ins	wa e	0.016 0.16 1.6		V/µs
t <sub>r</sub>	Rise Time <sup>(3)</sup>	$\begin{aligned} &V_{\text{IN}} = 50\text{mV}, \ C_{\text{L}} = 100\text{pF} \\ &I_{\text{Q}} = 10\mu\text{A}^{(1)}, \ R_{\text{L}} = 1\text{M}\Omega \\ &I_{\text{Q}} = 100\mu\text{A}, \ R_{\text{L}} = 100\text{k}\Omega \\ &I_{\text{Q}} = 1\text{mA}^{(1)}, \ R_{\text{L}} = 10\text{k}\Omega \end{aligned}$		20 2 0.9	= 01 = 01 = 01	89	20 2 0.9	ellev (S	Kade	20 2 0.9		μs
v	Overshoot Factor <sup>(3)</sup>	$\begin{aligned} &V_{IN} = 50 \text{mV}, \ C_L = 100 \text{pF} \\ &I_Q = 10 \mu \text{A}^1, \ R_L = 1 \text{M} \Omega \\ &I_Q = 100 \mu \text{A}, \ R_L = 100 \text{k} \Omega \\ &I_Q = 1 \text{mA}^1, \ R_L = 10 \text{k} \Omega \end{aligned}$		5 10 40	= 01 = 61	ogude	5 10 40	a Can	INSCIE	5 10 40		%

NOTES: 1. ICL7611, 7612, 7613 only.

# **ELECTRICAL CHARACTERISTICS (761X AND 762X ONLY)**

 $(V_{SUPPLY} = \pm 1.0V, I_Q = 10\mu A, T_A = 25^{\circ}C, unless otherwise specified. Specs apply to ICL7611/7612/7613 only.)$ 

CVMPOL	PARAMETER	SALE CONDITIONS	TA	76XX/	1				
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage	$R_S \le 100k\Omega$ , $T_A = 25^{\circ}C$ $T_{MIN} \le T_A \le T_{MAX}$	TA I		2 3			5 7	mV
ΔVos/ΔT	Temperature Coefficient of Vos	R <sub>S</sub> ≤ 100kΩ		10			15		μV/°C

<sup>2.</sup> C = Commercial Temperature Range: 0°C to +70°C

3. ICL7614/15; 39pF from pin 6 to pin.

M = Military Temperature Range: -55°C to +125°C

# ELECTRICAL CHARACTERISTICS (761X AND 762X ONLY) (CONT.)

(8	CANADO (a) BEXXET DEBENETED					76XXA	1				
SYMBOL	PARAMI			TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
los	Input Offset Current		24.9	$T_A = 25^{\circ}C$ $\Delta T_A = C$ $\Delta T_A = C$		0.5	30 300	ogistioV	0.5	30 300	pA
IBIAS	Input Bias Current		7,8±	$T_A = 25^{\circ}C$ $\Delta T_A = C_1$ $A_1000 = 0$		1.0	50 500		1.0	50 500	pA
VCMR	Common Mode Voltag (Except ICL7612)	ge Ran	ge	(3) TA = 26°C \( \Delta TA = C \) \( \Delta TA = SA \) \( \Delta TA = SA \)	±0.6			±0.6			٧
VCMR	Extended Common M Range (ICL7612 Only		oltage	(2) (0 = 1mA, R <sub>L</sub> = 10xΩ T <sub>A</sub> = 20°C -0.T <sub>A</sub> = C	+0.6 to -1.1			+ 0.6 to -1.1			٧
Vout	Output Voltage Swing	104	06	$R_L = 1M\Omega$ , $T_A = 25$ °C $\Delta T_A = C$		±0.98 ±0.96	spstio	/ tengii	±0.98 ±0.96		Viov
AVOL	Large Signal Voltage	Gain	88	$V_O = \pm 0.1 V$ , $R_L = 1 M \Omega$ $T_A = 25 ^{\circ} C$ $\Delta T_A = C$		90 80			90 80		dB
GBW	Unity Gain Bandwidth	9	68	0 + 472.		0.044			MHz		
RIN	Input Resistance			Voetanie je voetanie		1012			1012		
CMRR	Common Mode Rejec	tion Ra	atio	R <sub>S</sub> ≤ 100kΩ		80			80		
PSRR	Power Supply Rejection	on Rati	0 88	R <sub>S</sub> ≤ 100kΩ		80			80		dB
en	Input Referred Noise	Voltage	9	$R_S = 100\Omega$ , $f = 1kHz$		100	Hiberton	s8 nia	100		nV/√Hz
in	Input Referred Noise	Curren	t	$R_S = 100\Omega$ , $f = 1kHz$		0.01			0.01		pA/√Hz
ISUPPLY	Supply Current (Per Amplifier)		Stol	No Signal, No Load		6	15	nateles	6 I high	15	μΑ
SR	Slew Rate	-80 18 78	70 70 60	$A_{VOL} = 1, C_L = 100pF$ $V_{IN} = 0.2Vp-p$ $R_L = 1M\Omega$	Oil	0.016	s Rejet	tsaM n	0.016		V/µs
t <sub>res</sub>	Rise Time	98 88	08 08	$V_{IN} = 50$ mV, $C_L = 100$ pF $R_L = 1$ M $\Omega$		20	Reject	Supply	20		μs
To Ava	Overshoot Factor	001	01	$V_{IN} = 50$ mV, $C_L = 100$ pF $R_L = 1$ M $\Omega$		5	pusheld.	behisho	5		%

NOTE: C = Commercial Temperature Range (0°C to +70°C) M = Military Temperature Range (-55°C to +125°C).

### **ELECTRICAL CHARACTERISTICS (763X, 764X ONLY)**

(V<sub>SUPPLY</sub> = ±5.0V, T<sub>A</sub> = 25°C, unless otherwise specified.)

86	129 120	Avot = 100	70	6XXC	(6)	70	OVALOV		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage	$R_S \le 100k\Omega$ , $T_A = 25^{\circ}C$ $T_{MIN} \le T_A \le T_{MAX}$			10 15			20 25	mV
ΔV <sub>OS</sub> /ΔT	Temperature Coefficient of Vos	R <sub>S</sub> ≤ 100kΩ (Note 5)		20		(8)	30		
los	Input Offset Current	$T_A = 25^{\circ}C$ $\Delta T_A = C$ $\Delta T_A = M$		0.5	30 300 800		0.5	30 300 800	pA
IBIAS	Input Bias Current	T <sub>A</sub> = 25°C ΔT <sub>A</sub> = C ΔT <sub>A</sub> = M		1.0	50 500 4000		1.0	50 500 4000	pA
VCMR	Common Mode Voltage Range	$I_Q = 10\mu A^{(1)}$ $I_Q = 100\mu A^{(3)}$ $I_Q = 1mA^{(2)}$	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			٧

		9000						70	SXXC (	6)	7	6XXE	(6)	
SYME	BOL		PA	RAME	TER	MENS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNI
Vout	08	Output	Voltag	e Swing	6.0		(1) $I_Q = 10\mu A$ , $R_L = 1M\Omega$			Inshit	IsellO	sugni		
Ag				000			T <sub>A</sub> = 25°C	±4.9			±4.9		1	178
					-		$\Delta T_A = C$	±4.8	-	-	±4.8			-
		0.1					$\Delta T_A = M$	±4.7		mem	±4.7	Mont	Barrier B.	BAS
							$I_Q = 100\mu A$ , $R_L = 100k\Omega$							
		-					(3) $T_A = 25^{\circ}C$ $\Delta T_A = C$	±4.9 ±4.8	-		±4.9 ±4.8			V
							$\Delta T_A = M$	±4.5	go Rang	MOV BL	±4.5	moo ;		PMO
	-						(2) $I_Q = 1 \text{mA}, R_L = 10 \text{k}\Omega$		200	7	of bes			
							T <sub>A</sub> = 25°C	±4.5	oV ebol	a numa ano sk	±4.5	Sheep I		EMO
							$\Delta T_A = C$	±4.3			±4.3			
		RO O A			20.00		$\Delta T_A = M$	±4.0			±4.0			
AVOL	HAN	Large	Signal	Voltage	Gain		$V_0 = \pm 4.0 V$ , $R_L = 1 M \Omega^{(1)}$		100	Delinica VII	Taring C.			FUGA
							$I_Q = 10\mu A^{(1)}, T_A = 25^{\circ}C$	80	104		80	104		172/2
							$\Delta T_A = C$	75 68	niagi	enerioV	75 68	egra.		JOV
					09		ZIA - W	68		-0-0-0	68	1977	8 2	DOV
							$V_0 = \pm 4.0V$ , $R_L = 100k\Omega^{(3)}$	00	100		00	100		
							$I_Q = 100 \mu A, T_A = 25^{\circ} C$ $\Delta T_A = C$	80 75	102		80 75	102	12.14	1170
		sHM:					$\Delta T_A = M$	68		Holwbeam	68	Unity		dB
							$V_Q = \pm 4.0V$ , $R_L = 10k\Omega^{(2)}$			900	Regista	Sami-		UNIF
		08					IQ = 1mA <sup>(1)</sup> , T <sub>A</sub> = 25°C	80	98		80	98		
						-	$\Delta T_A = C$	75	ER FIOR	ajaR et	75	RH37		SHA
Sb		0.8	1		- 08		$\Delta T_A = M$ $\Delta MOOT \ge e^{AT}$	68	Hart no	InsieH.	68	- Popul		RAR
GBW		Unity	Gain Ba	andwidth			$I_Q = 10\mu A^{(1)}$		0.044	astold b	Referre	0.044		MHz
							$I_Q = 100 \mu A^{(3)}$		0.48	d Noise	Heterre	0.48		
-	37	- 0	-				$I_Q = 1 \text{mA}^{(2)}$	-	1.4	12	10111 to 1	1.4		
RIN		Input I	Resistar	nce				1012			10 <sup>12</sup>	1493	Ω	K JR4038
CMRR		Comm	on Mod	le Rejec	tion Ra	itio	$R_S \le 100 k\Omega$ , $I_Q = 10 \mu A^{(1)}$	70	96		70	96		FRE
							$R_S \le 100k\Omega$ , $I_Q = 100\mu$ A	70	91		70	91		dB
							$R_S \le 100 k\Omega$ , $I_Q = 1 mA^{(2)}$	60	87		60	87		
PSRR		Power	Supply	Rejecti	on Rati	0	$R_S \le 100k\Omega$ , $I_Q = 10\mu A^{(1)}$	80	94		80	94	100	15
							$R_S \le 100 k\Omega$ , $I_Q = 100 \mu A$	80	86		80	86		dB
- 2		1 8			a		$R_S \le 100k\Omega$ , $I_Q = 1mA^{(2)}$	70	77	3070	70	77		
en		Input	Referred	Noise	Voltage	)	$R_S = 100\Omega$ , $f = 1kHz$		100			100		nV/√
In		Input I	Referred	d Noise	Curren	-1 epn	$R_S = 100\Omega$ , $f = 1kHz$	tr + 7	0.01	aff. our	ensacronin	0.01	emis Dire	pA/V
ISUPPLY			Curren				No Signal, No Load		0.01	0.03		0.01	0.03	
		(Per A	mplifier)	)			$I_{Q} = 10 \mu A^{(1)}$	1 50	0.01	0.000	HAP	0.01	0.000	roal.
							$ Q = 10\mu A^{(1)}$ $ Q = 100\mu A$	simod	0.01	0.022	es = a	0.01	0.022	mA
							$I_{Q} = 1 \text{mA}^{(2)}$		1.0	2.5		1.0	2.5	111/4
V <sub>01</sub> /V <sub>02</sub>	(8)	Chann	el Sepa	ration	n oid	Ter	A <sub>VOL</sub> = 100		120			120		dB
SR	xate	Slew I	Rate <sup>(4)</sup>	N. 4150	977	MILIN	AvoL = 1, CL = 100pF		RM	MAR	49		JOE	MYS
			V CH LVE	AUTO NOTES		-	$V_{IN} = 8V_{P-P}$ $I_{Q} = 10\mu A^{(1)}, R_{L} = 1M\Omega$		0.046		resolution (	0.010		1//
							10 = 100 0A Pr = 100kO		0.016	egatio	/ tealt(	0.016		V/µ5
	100						$I_Q = 1 \text{mA}^{(1)}, R_L = 10 \text{k}\Omega^{(2)}$		1.6	-		1.6		
t <sub>r</sub>		Rise T	Time <sup>(4)</sup>		1.25	1	V <sub>IN</sub> = 50mV, C <sub>I</sub> = 100pF	2	24 10 II	storius)	or indicate to	duni,		TINSTING.
		0.5					$V_{IN} = 50 \text{mV}, C_L = 100 \text{pF}$ $I_Q = 10 \mu A^{(1)}, R_L = 1 \text{M}\Omega$	10570	20	Hymna	) isent	20	Mary Land	μs
	300						$I_{Q} = 100 \mu A, R_{L} = 100 k \Omega$		2	8 W. Y.		2		
	4			-	No.		$I_Q = 1 \text{mA}^{(2)}, R_L = 10 \text{k}\Omega$		0.9			0.9		
							0°85 - AT							
			2.4.2											
			7.03											

9	γ	4	۱	3	
	Ŀ	ń	i	i	

OVER DOL		ASP	PART CHESSIT SES THE	e 70	6XXC	(6)	76XXE (6)			UNIT
SYMBOL	PARAMETER	FIL	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
TOTAL CONTRACTOR	Overshoot Factor <sup>(4)</sup>		V <sub>IN</sub> = 50mV, C <sub>L</sub> = 100pF						10.283	
			$V_{IN} = 50 \text{mV}, C_L = 100 \text{pF}$ $I_Q = 10 \mu A^{(1)}, R_L = 1 \text{M}\Omega$	100	5			5		NEW COLUMN
No.	- 87.407 6 - "V	Far	$I_Q = 100 \mu A$ , $R_L = 100 k \Omega$		10			10	ou day E	%
		1	$I_Q = 1 \text{mA}^{(2)}, R_L = 10 \text{k}\Omega$		40		don't a	40	130 034 -	

NOTES: 1. Does not apply to 7641.

2. Does not apply to 7642.

3. ICL7631/32 only.
 4. Does not apply to 7632.

For Test Conditions:

C = Commercial Temperature Range: 0°C to +70°C

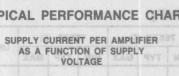
M = Military Temperature Range: -55°C to +125°C

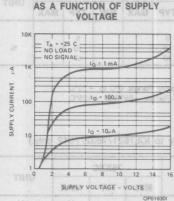
### **ELECTRICAL CHARACTERISTICS (763X AND 764X ONLY)**

(V<sub>SUPPLY</sub> =  $\pm 1.0V$ , I<sub>Q</sub> =  $10\mu$ A, T<sub>A</sub> =  $25^{\circ}$ C, unless otherwise specified. Specs apply to ICL7631/7632/7642 only.)

SYMBOL	PARAMETER SET	TEST CONDITIONS				
		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vos CITAR MOITOI	Input Offset Voltage	$R_S \le 100k\Omega$ , $T_A = 25^{\circ}C$ $T_{MIN} \le T_A \le T_{MAX}$	RATTABE	PRIO J	10 14(12) 3	Vm
ΔV <sub>OS</sub> /ΔT	Temperature Coefficient of Vos	$R_S \le 100k\Omega$	DELONG	20	HAN SEL	μV/°C
los	Input Offset Current	$T_A = 25^{\circ}C$ $\Delta T_A = C$		0.5	30 300	pA
IBIAS	Input Bias Current	$T_A = 25^{\circ}C$ $\Delta T_A = C$	Aust	1.0	50 500	pA unx
VCMR	Common Mode Voltage Range		±0.6	Chief - Appets		V
Vout	Output Voltage Swing	$R_L = 1M\Omega$ , $T_A = 25^{\circ}C$ $\Delta T_A = C$		±0.98 ±0.96		V
AVOL	Large Signal Voltage Gain	$V_O = \pm 0.1V$ , $R_L = 1M\Omega$ $T_A = 25^{\circ}C$ $\Delta T_A = C$	27,60	90 80	0 85 1	dB
GBW	Unity Gain Bandwidth	V - VOMBOSDR	0.044	BUTARSAN	TRUE SERS	MHz
RIN	Input Resistance	DESIGN TOWN STANDINGS	1012	mini no	M ADDISON	Ω
CMRR A TOW T	Common Mode Rejection Ratio	R <sub>S</sub> ≤ 100kΩ A	MA-SER	80	EUNOTA	A BA dB
PSRR	Power Supply Rejection Ratio	DMSUOSRY	80	RUTARE	PEMBL	dB
e <sub>n</sub>	Input Referred Noise Voltage	$R_S = 100\Omega$ , $f = 1$ kHz		100		nV/√Hz
in	Input Referred Noise Current	$R_S = 100\Omega$ , $f = 1kHz$	Apr. + Mills	0.01	Aunit v pl.	pA/√Hz
ISUPPLY	Supply Current (Per Amplifier)	No Signal, No Load		6	15 Autor and	μА
V <sub>01/V</sub> 02	Channel Separation	Avol = 100		120		dB
SR	Slew Rate	$A_{VOL} = 1$ , $C_L = 100pF$ $V_{IN} = 0.2Vp-p$ $R_L = 1M\Omega$		0.016	A101 = 01	V/µs
tr	Rise Time	$V_{IN} = 50$ mV, $C_L = 100$ pF $R_L = 1$ M $\Omega$	1	20		μs
1001 101 2000	Overshoot Factor	$V_{IN} = 50$ mV, $C_L = 100$ pF $R_L = 1$ M $\Omega$	un et	5	68- 0	%

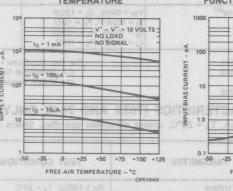
NOTE: C = Commercial Temperature Range (0°C to +70°C)



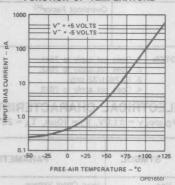


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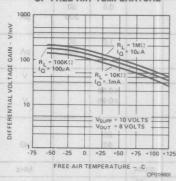
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR **TEMPERATURE** 



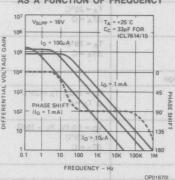
INPUT BIAS CURRENT AS A **FUNCTION OF TEMPERATURE** 



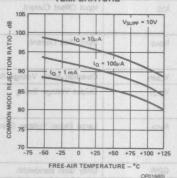
LARGE SIGNAL DIFFERENTIAL **VOLTAGE GAIN AS A FUNCTION** OF FREE-AIR TEMPERATURE



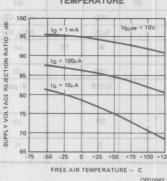
LARGE SIGNAL DIFFERENTIAL **VOLTAGE GAIN AND PHASE SHIFT** AS A FUNCTION OF FREQUENCY



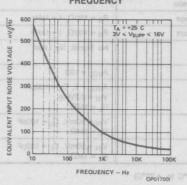
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



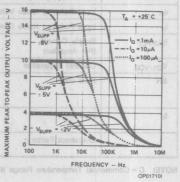
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR **TEMPERATURE** 



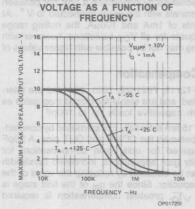
EQUIVALENT INPUT NOISE **VOLTAGE AS A FUNCTION OF** FREQUENCY



PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

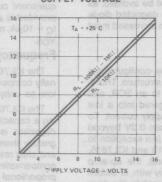


# TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

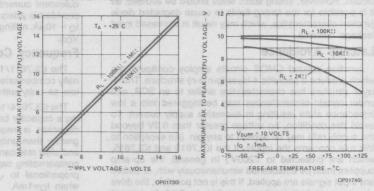


MAXIMUM PEAK-TO-PEAK OUTPUT

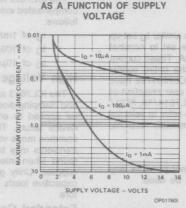
MAXIMUM PEAK-TO-PEAK OUTPUT **VOLTAGE AS A FUNCTION OF** SUPPLY VOLTAGE



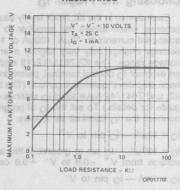
MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



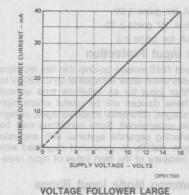
MAXIMUM OUTPUT/SOURCE



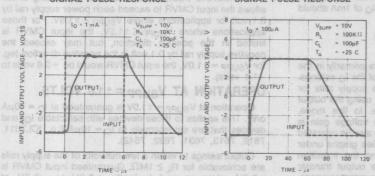
MAXIMUM OUTPUT SINK CURRENT MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



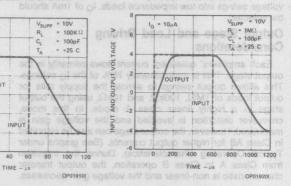
CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



10 = 1 mA NOT NO Au Co DANO! INPUT

SIGNAL PULSE RESPONSE

to VV.0- cr Ve 0+ Viscolly oposson muminim, Va.0± common success where greater common values greater common values greater common values of vo.r± = squev

0 2 4 6 8

10

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

#### Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. (An exception to this rule concerns the inputs of the ICL7613 and ICL7615, which are protected to ±200V.) In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

### Choosing the Proper IQ

Each device in the ICL76XX family has a similar I $_Q$  set-up scheme, which allows the amplifier to be set to nominal quiescent currents to  $10\mu A$ ,  $100\mu A$  or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12/13 and ICL7631/32 have an external I $_Q$  control terminal, permitting user selection of each amplifiers' quiescent current. (The ICL7614/15, 7621/22, and 7641/42 have fixed I $_Q$  settings — refer to selector guide for details.) To set the I $_Q$  of programmable versions, connect the I $_Q$  terminal as follows:

 $I_Q = 10\mu A - I_Q$  pin to V<sup>+</sup>

 $I_Q=100\mu A$  —  $I_Q$  pin to ground. If this is not possible, any voltage from V  $^+$  -0.8 to V  $^-$  +0.8 can be used.

IQ = 1mA - IQ pin to V

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads,  $I_Q$  of 1mA should be selected.

# Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the  $I_Q$  settings. This allows output swings to almost the supply rails for output loads of  $1M\Omega$ ,  $100k\Omega$ , and  $10k\Omega$ , using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the  $I_Q$  settings if corresponding loads of  $10k\Omega$ ,  $100k\Omega$ , and  $1M\Omega$  are used.

nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V $^+$ . At quiescent currents of 1mA and 100 $\mu\text{A}$ , the nulling range provided is adequate for all VOS selections; however with  $I_Q=10\,\mu\text{A}$ , nulling may not be possible with higher values of VOS.

#### Frequency Compensation

The ICL7611/12/13, 7621/22, 7631, 7641/42 are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF

The ICL7614/15 are externally compensated by connecting a capacitor between the COMP and OUT pins. A 39pF capacitor is required for unity gain compensation; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor. Since the  $g_m$  of the first stage is proportional to  $\sqrt{I_Q}$ , greatest compensation is required when  $I_Q\!=\!1\text{mA}$ .

The ICL7632 is not compensated internally, nor can it be compensated externally. The device is stable when used as follows:

I<sub>Q</sub> of 1mA for gains  $\ge 20$ I<sub>Q</sub> of 100 $\mu$ A for gains  $\ge 10$ I<sub>Q</sub> of 10 $\mu$ A for gains  $\ge 5$ 

#### **High Voltage Input Protection**

The ICL7613 and 7615 include on-chip thin film resistors and clamping diodes which allow voltages of up to ±200V to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages, or high transients may be experienced. Such conditions may be found when interfacing separate systems with separate supplies. Unity gain stability is somewhat degraded with capacitive loads because of the high value of input resistors.

# **Extended Common Mode Input Range**

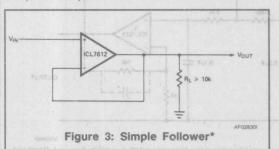
The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where  $V_{SUPP} \ge \pm 1.5V$ . For those applications where  $V_{SUPP} \le \pm 1.5V$ , the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for  $V_{SUPP} = \pm 1.0V$ , the input CMVR would be  $\pm 0.6$  volts to  $\pm 1.1$  volts).

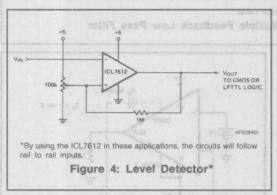
# OPERATION AT VSUPP = ±1.0 VOLTS

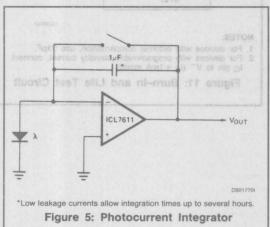
Operation at V<sub>SUPP</sub> =  $\pm 1.0V$  is guaranteed at I<sub>Q</sub> =  $10\mu$ A only. This applies to those devices with selectable I<sub>Q</sub>, and devices that are set internally to I<sub>Q</sub> =  $10\mu$ A (i.e., ICL7611, 7612, 7613, 7631, 7632, 7642).

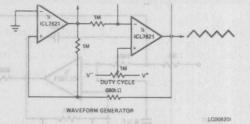
Output swings to within a few millivolts of the supply rails are achievable for  $R_L \geq 1 M \Omega$ . Guaranteed input CMVR is  $\pm 0.6 V$  minimum and typically + 0.9 V to -0.7 V at  $V_{SUPP} = \pm 1.0 V$ . For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction,









Since the output range swings exactly from rail to rail, frequently and duty cycle are virtually independent of power supply variations.

Figure 6: Precise Triangle/Square Wave Generator

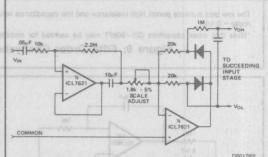
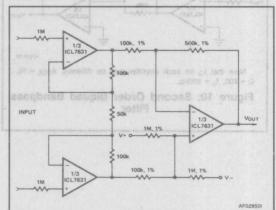


Figure 7: Averaging AC to DC Converter for A/D Converters Such as ICL7106, 7107, 7109, 7116, 7117

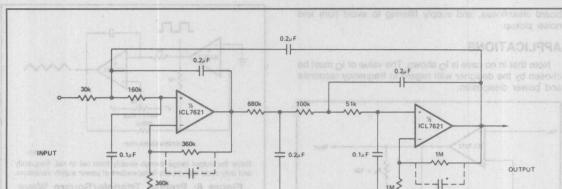


Note that A<sub>VOL</sub> = 25; single Ni-cad battery operation, input current (from sensors connected to patient) limited to  $<5\mu\text{A}$  under fault conditions.

Figure 8: Medical Instrument Preamp

4

CL76XX



The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f<sub>c</sub> = 10Hz, A<sub>VCL</sub> = 4, Passband ripple = 0.1dB

\*Note that small capacitors (25-50pF) may be needed for stability in some cases.

Figure 9: Fifth Order Chebyshev Multiple Feedback Low Pass Filter

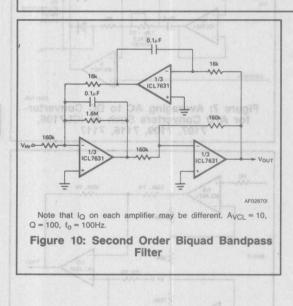
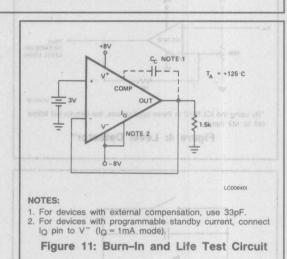


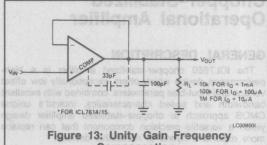
Figure 8: Medical Instrument Preamp



AF02860I

4-48

Extremely Low Chopping Spikes at Input and Output



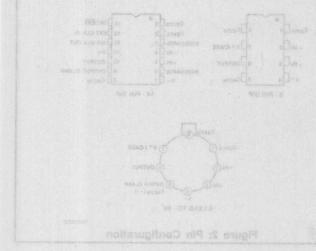
Compensation The Hand of ord Tallers of a specific single process of the specific single proc

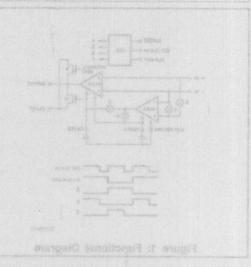
The clock oscillator and all the other control credity is ancely self-contained, nowever the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the 102.7869 is internally concentrated for unity-cain coexisted.

#### ORDERING INFORMATION

TEMPERATURE	
-65°C to + (25°C	

PACKAGE	TEMPERATURE	TRAS
	0°05 + 00°0	
8-PIN TO-89		
	-25°C to + 65°C	
8-PH CERCIP		CL79698UA-1





# ICL7650

# Chopper-Stabilized Operational Amplifier

#### GENERAL DESCRIPTION

The ICL7650 chopper-stabilized amplifier is a highperformance device which offers exceptionally low offset voltage and input-bias parameters, combined with excellent bandwidth and speed characteristics. Intersil's unique CMOS approach to chopper-stabilized amplifier design yields a versatile precision component that can replace more expensive hybrid or monolithic devices.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650 is internally compensated for unity-gain operation.

#### ORDERING INFORMATION

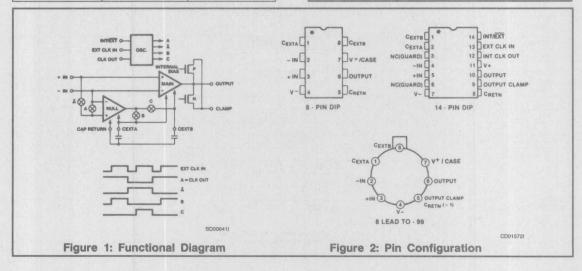
PART	TEMPERATURE RANGE	PACKAGE
ICL7650CPA-1	0°C to +70°C	8-PIN Plastic
ICL7650BCPA-1	0°C to +70°C	8-PIN Plastic
ICL7650CPD	0°C to +70°C	14-PIN Plastic
ICL7650BCPD	0°C to +70°C	14-PIN Plastic
ICL7650CTV-1	0°C to +70°C	8-PIN TO-99
ICL7650BCTV-1	0°C to +70°C	8-PIN TO-99
ICL7650IJA-1 ·	-25°C to +85°C	8-PIN CERDIP
ICL7650BIJA-1	-25°C to +85°C	8-PIN CERDIP

GE)		WE	RS	
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#### **FEATURES**

- Extremely Low Input Offset Voltage 2μV
- Low Long-Term and Temperature Drifts of Input Offset Voltage
- Low DC Input Bias Current 10pA (20pA 7650B)
- Extremely High Gain, CMRR and PSRR Min 120dB
- High Slew Rate 2.5V/μs
- Wide Bandwidth 2MHz
- Unity-Gain Compensated
- Very Low Intermodulation Effects (Open Loop Phase Shift < 10°C @ Chopper Frequency)</li>
- Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use
- Extremely Low Chopping Spikes at Input and Output

PART	TEMPERATURE RANGE	PACKAGE
ICL7650IJD	-25°C to +85°C	14-PIN CERDIP
ICL7650BIJD	-25°C to +85°C	14-PIN CERDIP
ICL7650ITV-1	-25°C to +85°C	8-PIN TO-99
ICL7650BITV-1	-25°C to +85°C	8-PIN TO-99
ICL7650MJD	-55°C to +125°C	14-PIN CERDIP
ICL7650BMJD	-55°C to +125°C	14-PIN CERDIP
ICL7650MTV-1	-55°C to +125°C	8-PIN TO-99
ICL7650BMTV-1	-55°C to +125°C	8-PIN TO-99



#### ABSOLUTE MAXIMUM RATINGS

Total Supply Vo	Itage (V + to V-)	18 Volts Cont.	Total Power Dissipn (TA	= 25°C)
Input Voltage	( $V^+ + 0.3$ ) to ( $V^ 0.3$ )	3) Volts	CERDIP Package	500mW
Voltage on oscil	lator control pinsV+	to V	Plastic Package	375mW
except EXT CLC	OCK IN: $(V^+ + 0.3)$ to $(V^+ - 6.1)$	0) Volts	TO-99	250mW
Duration of Out	out short circuitlr	ndefinite Stora	ige Temp. Range	65°C to 150°C
Current into any	pin	10mA Oper	ating Temp. Range	See Note 1
	g (Note 4)		Temperature (Soldering, 1	0sec)300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

Test Conditions:  $V^+ = +5V$ ,  $V^- = -5V$ ,  $T_A = +25$ °C, (unless otherwise specified)

21 61	1 9 4 8 4 B		L	IMITS 765	0	arL	IMITS 7650	В	LINUT
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage	T <sub>A</sub> = +25°C -25°C < T <sub>A</sub> < +85°C -55°C < T <sub>A</sub> < +125°C	LISSIA av TU	±2 ±5	±5 ±50	DELTAN	#2 V-TU±5  30 OV VJ99U3	±10.0 ±75	MAMO PV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temp. Coefficient of Input Offset Voltage	-25°C < T <sub>A</sub> < +85°C		0.1	6		0.1		μV/°C
$\frac{\Delta V_{OS}}{\Delta t}$	Change in Input Offset Voltage With Time			100			100		nV/mont
IBIAS	Input Bias Current (doubles every 10°C) Polarity is + or - (Note 5)	T <sub>A</sub> = +25°C '0°C < T <sub>A</sub> < +70°C -25°C < T <sub>A</sub> < +85°C	EUMOR EUMOR Mr = y	±1.5 ±35 ±100	±10		±1.5 ±35 ±100	±20	pA
los	Input Offset Current (Note 5)	T <sub>A</sub> = 25°C		5.0			5.0		pA
RIN	Input Resistance			1012			1012		Ω
AVOL	Large Signal Voltage Gain	$R_L = 10k\Omega$	1x10 <sup>6</sup>	5x10 <sup>6</sup>	1	1x10 <sup>6</sup>	5x10 <sup>6</sup>		V/V
Vout	Output Voltage Swing (Note 3)	$R_L = 10k\Omega$ $R_L = 100k\Omega$	±4.7	±4.85 ±4.95	-	±4.7	±4.85 ±4.95	3411111	VO
CMVR	Common Mode Voltage Range	ISAVIOSE	-5.0	-5.2 to +2.0	1.5	-5.0	-5.2 to +2.0	1.5	٧
CMRR	Common Mode Rejection Ratio	CMVR = -5V  to  +1.5	110	120	30	110	30 A 120	38440	dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	120	130		120	130	3, 748	dB
e <sub>n</sub>	Input Noise Voltage	$R_S = 100\Omega$ f = 0 to 10Hz	1	2	-		2	- name	μV <sub>p-p</sub>
İn	Input Noise Current	f = 10Hz		0.01	-		0.01		pA/√H
GBW	Unity Gain Bandwidth			2.0			2.0		MHz
SR	Slew Rate	$C_L = 50pF$ , $R_L = 10k\Omega$	4.41	2.5	0 19	-	2.5		V/µs
t <sub>r</sub>	Rise Time	A SHELLMAN		0.2		999800	0.2	110000000	μs
	Overshoot	A BUILDING	1 111	20	18 B	181132	20	442000	%
V+ to V-	Operating Supply Range	A PULL THE	4.5		16	4.5		16	V
ISUPP	Supply Current	no load	1 11	2.0	3.5		2.0	3.5	mA
fch	Internal Chopping Frequency	pins 12-14 open (DIP)	120	200	375	120	200	375	Hz
	Clamp ON Current (note 2)	$R_L = 100k\Omega$	25	70	150	25	70	150	μΑ
8 5	Clamp OFF Current (note 2)	-4.0V < V <sub>OUT</sub> < +4.0V	ASS.	Charles of the Con-	- 81	81	Sr 10r	0 8	pA

NOTES: 1. Operating temperature range for M series parts is -55°C to +125°C, for I series is -25°C to +85°C, for C series is 0°C to +70°C

2. See OUTPUT CLAMP under detailed description.

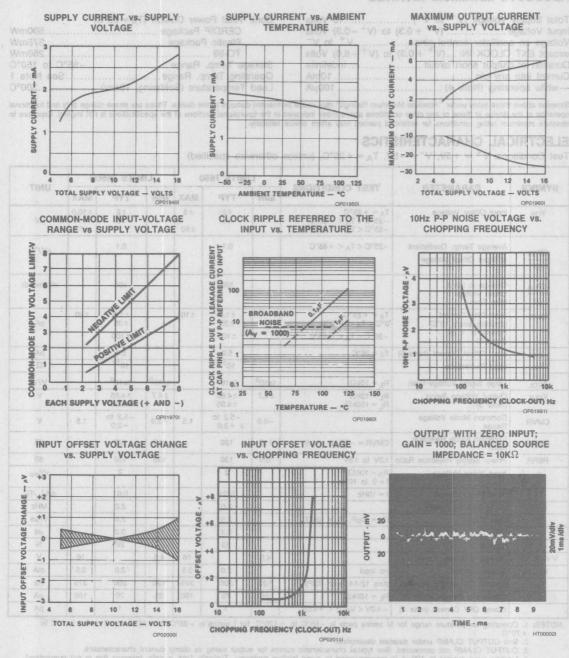
3. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.

4. Limiting input current to  $100\mu$ A is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed. 5.  $los = 2 \bullet l_{BIAS}$ 

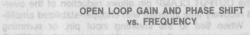
CL7650

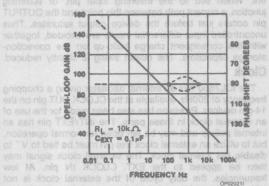
# **WINTERSIL**

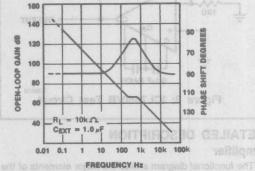
### TYPICAL PERFORMANCE CHARACTERISTICS



# TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)



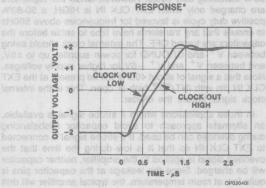




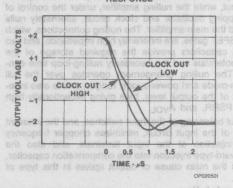
OPEN LOOP GAIN AND PHASE SHIFT

vs. FREQUENCY

VOLTAGE FOLLOWER LARGE SIGNAL PULSE

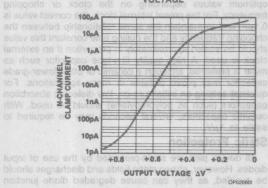


VOLTAGE FOLLOWER LARGE SIGNAL PULSE
RESPONSE\*

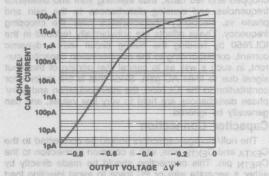


\* THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

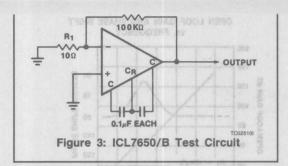
N-CHANNEL CLAMP CURRENT vs. OUTPUT VOLTAGE



P-CHANNEL CLAMP CURRENT vs. OUTPUT VOLTAGE



OP02070I



# DETAILED DESCRIPTION Amplifier

The functional diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and AyOL.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

#### Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/ phase disturbances are held to very low values, and can generally be ignored.

# **Capacitor Connection**

The null/storage capacitors should be connected to the CEXTA and CEXTB pins, with a common connection to the CRETN pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to CRETN.

load recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650 has an internal oscillator giving a chopping frequency of 200Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V<sup>-</sup> to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies, the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50-80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the

capacitors are turned OFF. The external clock should swing

between V+ and GROUND for power supplies up to ±6V,

and between V+ and V+ -6V for higher supply voltages.

Note that a signal of about 400Hz will be present at the EXT

CLK IN pin with INT/EXT high or open. This is the internal

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than  $10\mu V/\text{sec}$ , and relatively long measurements can be made with little change in offset.

# BRIEF APPLICATION NOTES Component Selection

clock signal before the divider.

The two required capacitors,  $C_{\text{EXTA}}$  and  $C_{\text{EXTB}}$ , have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is  $0.1\mu\text{F}$ , and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorbtion capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to  $1\mu\text{V}$ .

#### Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

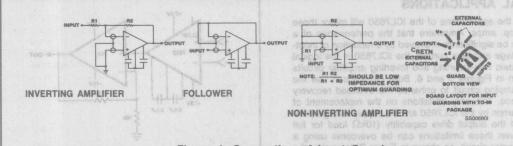


Figure 4: Connection of Input Guards

#### Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

#### Output Stage/Load Driving

The output circuit is a high-impedance type (approximately  $18k\Omega$ ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a  $1k\Omega$  load than with a  $10k\Omega$  load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a  $1k\Omega$  load. However, for wideband applications, the best frequency response will be achieved with a load resistor of  $10k\Omega$  or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than  $10^\circ$  in the transition region where the main amplifier takes over from the null amplifier.

#### Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 µV/°C, but up to tens of  $\mu V/^{\circ}C$  for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

#### Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

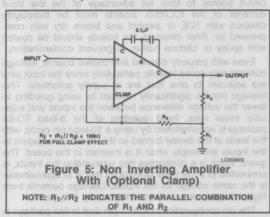
#### Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V $^+$ , by two capacitors from those pins to V $^-$ , will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V $^-$  is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101,  $\mu$ A748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650.

#### TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op, amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of inputoffset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650 are the supply voltage (±8V max.) and the output drive capability (10k $\Omega$  load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.



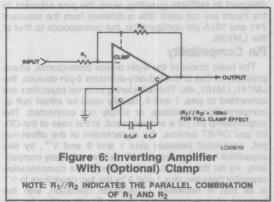
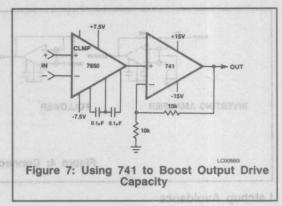
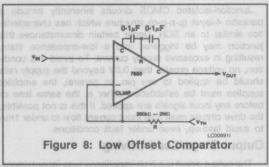
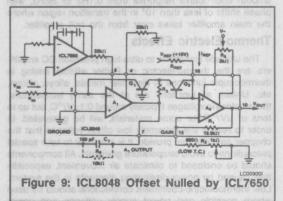


Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current  $\approx V_{IN}/R$  without disturbing other portions of the system.





Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Figure 8. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.



FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

#### GENERAL DESCRIPTION

The ICL7652 chopper-stabilized amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature, It is similar to INTERSIL's ICL7650 but offers improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are reduced slightly.

INTERSIL's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

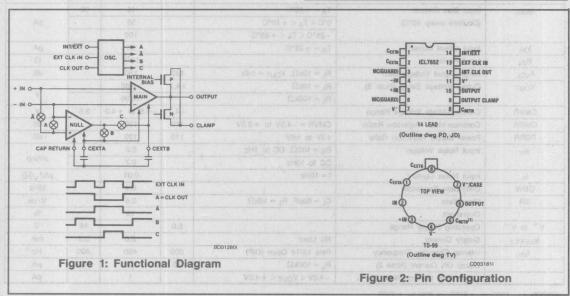
The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652 is internally compensated for unity-gain operation.

# FEATURES PARTIES PROPERTY PROP

- Extremely Low Input Offset Voltage 10µV Over Temperature Range
- Ultra Low Long-Term and Temperature Drifts of Input Offset Voltage (150nV/Month, 100nV/°C)
- Low DC Input Bias Current 15pA
- Extremely High Gain, CMRR and PSRR Min 110dB
- Low Input Noise Voltage 0.2µVp-p (DC 1Hz)
- Internally Compensated for Unity-Gain Operation
- Very Low Intermodulation Effects (Open-Loop Phase Shift < 2°@ Chopper Frequency)
- Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use
- Extremely Low Chopping Spikes at Input and Output

### ORDERING INFORMATION

PART	TEMP. RANGE	PACKAGE
ICL7652CPD	0°C to +70°C	14-pin plastic
ICL7652IJD	-25°C to +85°C	14-pin CERDIP
ICL7652CTV	0°C to +70°C	8-pin TO-99
ICL7652ITV	-25°C to +85°C	8-pin TO-99



4-57



### **ABSOLUTE MAXIMUM RATINGS**

Total Supply Voltage (V + to V-)	18V
Input Voltage (V + 0.3) to (V-	-0.3)V
Voltage on Oscillator Control PinsV+	to V
Duration of Output Short Circuit	definite
Current into Any Pin	.10mA
- while operating (Note 4)	100μΑ

Extremely High Gain, CMRR and PSRR -- Min

Continuous Total Power Dissipation (T	$A = 25^{\circ}C$
CERDIP Package	500mW
CERDIP Package	375mW
TO-99	250mW
Storage Temperature Range	55°C to 150°C
Operating Temperature Range	
ICL7652CXX	0°C to +70°C
ICL7652IXX	25°C to +85°C
Lead Temperature (Soldering, 10sec) .	300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

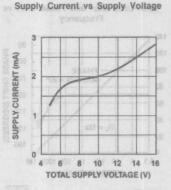
# ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = +5V, V- = -5V, T<sub>A</sub> = +25°C, Test Circuit (unless otherwise specified)

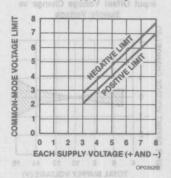
	emely Low Chapping Spikes	es two external a External ting polepilats on		opinien, oui		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage	T <sub>A</sub> = +25°C	torile	±2	±5	Jania . ed
PACKAGE	IRY TENR. RANGE	Over Operating Temperature Range (Note 1)			enistric	hVφlock o-liea yier
ΔV <sub>OS</sub> ΔT	Average Temperature Coefficient of Input Offset Voltage	Operating Temperature Range (Note 1)	the ICL tion.	notions ni	lication for un	μV/°C
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage vs Time	COI		150		nV/mont
IBIAS	Input Bias Current	T <sub>A</sub> = +25°C		15	30	Alexander Victoria
	(Doubles every 10°C)	0°C < T <sub>A</sub> < +70°C		35	*	pA
		-25°C < T <sub>A</sub> < +85°C		100		
los	Input Offset Current	T <sub>A</sub> = +25°C		25	-0 ISI	pA
RIN	Input Resistance			1012	Les cons	Ω
AVOL	Large Signal Voltage Gain	$R_L = 10k\Omega$ , $V_{OUT} = \pm 4V$	120	150	100	dB
Vout	Output Voltage Swing (Note 3)	$R_L = 10k\Omega$	±4.7	±4.85		V
	et travello de la concentra	$R_L = 100k\Omega$		±4.95		V
CMVR	Common-Mode Voltage Range		-4.3	-4.8 to +4.0	3.5	V
CMRR	Common-Mode Rejection Radio	CMVR = -4.3V  to  +3.5V	110	130	1000	dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	110	130	13	dB
en	Input Noise Voltage	$R_S = 100\Omega$ , DC to 1Hz	.0.7	0.2	ons o or	Inutatina
	[ac] and	DC to 10Hz		0.7		μVp-p
in	Input Noise Current	f = 10Hz		0.01		pA/√H
GBW	Unity-Gain Bandwidth	Designation of the second	RERJOT	0.4	2 6	MHz
SR	Slew Rate	$C_L = 50 pF$ , $R_L = 10 k\Omega$	190 xun	0.5	and the second	V/µs
	Overshoot			15	Recognition	%
V <sup>+</sup> to V <sup>-</sup>	Operating Supply Range		5.0	S. Constitution of the	16	V
ISUPPLY	Supply Current	No Load		2.0	3.5	mA
fch	Internal Chopping Frequency	Pins 12-14 Open (DIP)	200	400	600	Hz
Lts	Clamp ON Current (Note 2)	$R_L = 100k\Omega$	25	100	150	μΑ
noise	Clamp OFF Current (Note 2)	-4.0V < V <sub>OUT</sub> < +4.0V		1		рА

NOTES: 1. -25°C to +85°C, or 0°C to +70°C.
2. See OUTPUT CLAMP under detailed description.
3. OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs clamp current characteristics.
4. Limiting input current to 100μA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.

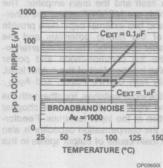
# TYPICAL PERFORMANCE CHARACTERISTICS TAIST DARAMS TO MANAGERS JAOIS



Common-Mode Input Voltage Range vs Supply Voltage



Clock Ripple Referred to the Input vs Temperature



noguation
ious enapper-stabilized amplifiers have suffered
solutation effects between the chapter frequency

Supply Current vs Ambient

Input Offset Voltage vs Chopping
Frequency



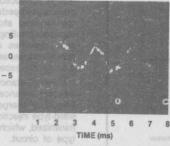
% parameter is EXT CLK in duty cycle

OP038301

Broadband Noise Balanced Source

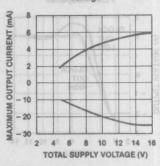
Impedance =  $1k\Omega$  Gain = 1000

 $C_{EXT} = 0.1 \mu F$ 



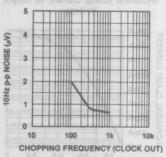
OP03660

Maximum Output Current vs Supply Voltage



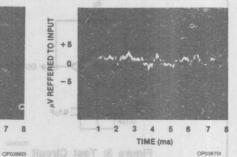
OP03610

10Hz P-P Noise Voltage Voltage vs Chopping Frequency



OP03640

Broadband Noise Balanced Source Impedance =  $1k\Omega$  Gain = 1000  $C_{EXT} = 1.0 \mu F$ 



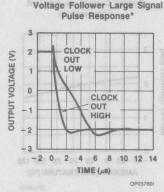
probiny. The main amplifier is connected continuously on the input to the output. The nulling amplifier, under the

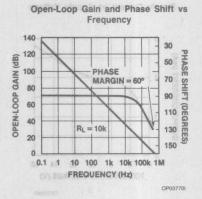
REFERRED TO INPUT

# **BINTERSIL**

# TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

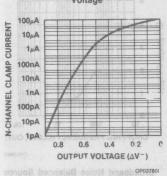
Voltage Follower Large Signal Pulse Response\* CLOCK OUTPUT VOLTAGE (V) OUT LOW CLOCK 0 OUT HIGH -2 -2 0 2 4 6 8 10 12 14 TIME (µs) OP037501



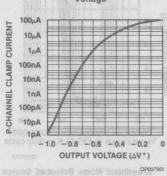


\*The two different responses correspond to the two phases of the clock.

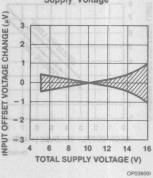
N-Channel Clamp Current vs Output Voltage



P-Channel Clamp Current vs Output Voltage



Input Offset Voltage Change vs Supply Voltage



R<sub>2</sub>
1MΩ
1kΩ
1kΩ
1kΩ
10L7652 c OUTPUT

0.1μF

TO028401

control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high-impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A<sub>VOL</sub>. Careful balancing of the input switches, together with the

Careful balancing of the input switches, together with the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals. Feedforward-type injection into the compensation capacitor is also minimized, which is the main cause of output spikes in this type of circuit.

# DETAILED DESCRIPTION

The Functional Diagram (Figure 1) shows the major elements of the ICL7652. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output. The nulling amplifier, under the

#### Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping

frequency. These effects are substantially reduced in the ICL7652 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7652, the intermodulation and gain/ phase disturbances are held to very low values, and can generally be ignored.

# Capacitor Connection owled TV bas 8 bas 1 and

The null-storage capacitors should be connected to the CEXTA and CEXTB pins, with a common connection to the CRETN pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to CRETN. that of the LM108 device, owing to th

#### Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled differential input voltages are avoided, together with the consequent charge build-up on the correctionstorage capacitors. The output swing is slightly reduced.

#### Clock

The ICL7652 has an internal oscillator, giving a chopping frequency of 400Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%-80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V+ and V-. The logic threshold will be at about 2.5V below V+. Note also that a signal of about 800Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10 µV/sec, and relatively long measurements can be made with little change in offset.

# BRIEF APPLICATION NOTES

### Component Selection

The required capacitors, CEXTA and CEXTB, are normally in the range of  $0.1\mu F$  to  $1.0\mu F$ . A  $1.0\mu F$  capacitor should be used in broad bandwidth circuits if minimum clock ripple noise is desired. For limited bandwidth applications where clock ripple is filtered out, using a 0.1 µF capacitor results in slightly lower offset voltage. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other

lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV. an expensive against and sevol

#### Static Protection probable from the

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics which may result in increased input-leakage

# Latchup Avoidance and eff as some ones ent vi

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be trigerred into a low-impedance state, resulting in excessive supply current. To avoid this condition no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

#### Output Stage/Load Driving

The output circuit is a high-impedance type (approximately  $18k\Omega$ ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a  $1k\Omega$  load than with a  $10k\Omega$  load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a  $1k\Omega$  load. However, for wideband applications, the best frequency response will be achieved with a load resistor of  $10k\Omega$  or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

#### Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermo-couple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around 0.1 µV/°C, but up to tens of  $\mu V/^{\circ}C$  for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

#### Guarding

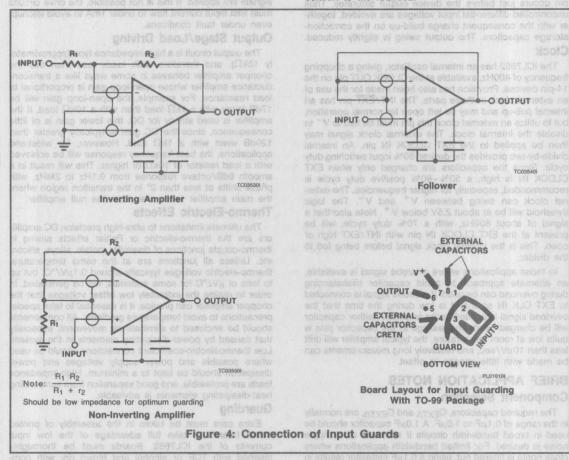
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7652. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 lead TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

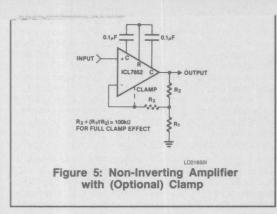
The pin configuration of the 14-pin dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

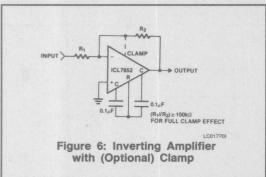
possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, which are usually used for offset-null or compensation capacitors. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V $^+$ , by two capacitors from those pins to V $^-$ , will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to V $^-$  is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101,  $\mu$ A748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7652.









Clearly the applications of the ICL7652 will mirror those of other op-amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7652 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op-amps by the ICL7652 are the supply voltage (±8V max) and the output drive capability (10k $\Omega$  load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7652. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

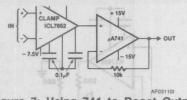
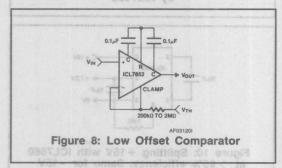


Figure 7: Using 741 to Boost Output Drive Capability

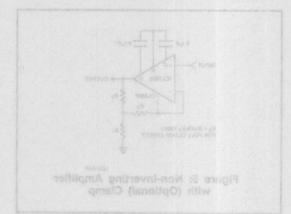
Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper-stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current  $\approx V_{IN}/R$  without disturbing other portions of the system.



It is possible to use the ICL7652 to offset-null such high slew rate and bandwidth amplifiers as the HA2500 and HA2600 series, as shown in Figure 9. The same basic idea can be used with low-noise bipolar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced. More details on these and other ideas are explained in application note A053.

Mixing the ICL7652 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit "backwards". A suitable connection is shown in Figure 10.







Clearly the approactions of the ICL7652 will minor those of other op-amps. Thus, anywhere that the performance of a credit can be significantly improved by a reduction of input, offset voltage and bias current. The ICL7652 is the logical choice. Basic non-inventing and inverting amplifier our deciring any streeting amplifier that the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7652 are the supply voltage (±8V other op amps by the ICL7652 are the supply voltage (±8V awing). Even these limitations can be overcome using a sample boostar directl, as shown in Figure 7 to enable the device) to be combined with the input capabilities of the device, so loop gain stability, when the leadback network is added, should be stability, when the leadback network is added, should be



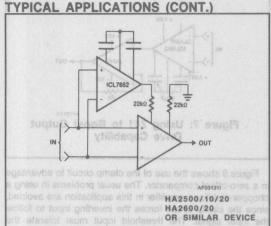
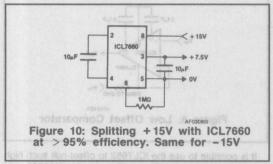


Figure 9: HA2500 or HA2600 Offset-Nulled by ICL7652



For further applications assistance, see A053 and R017

gan be used with low-noise bipotar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced, More details on these and other ideas are explained in application note A053.

Milbring the IGL7652 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the IGL7660 voltage converter circuit "backwards". A suitable connection is shown in Figure 10.

### GENERAL DESCRIPTION

The Intersil ICL8007 is a low input current JFET input operational amplifier. The ICL8007A is selected for 4 pA max input current.

The devices are designed for use in very high input impedance applications. Because of their high slew rate, high common mode voltage range and absence of 'latch-up', they are ideal for use as a voltage follower.

The Intersil 8007 and 8007A are short circuit protected. They require no external components for frequency compensation because the internal 6 dB/roll-off insures stability in closed loop applications. A unique bootstrap circuit insures unusually good common mode rejection for a JFET input op-amp and prevents large input currents as seen in some amplifiers at high common mode voltage.

#### ORDERING INFORMATION

PART	TEMPERATURE RANGE	PACKAGE
ICL8007CTY ICL8007ACTV	0°C to +70°C	8 LEAD TO-99
ICL8007MTY ICL8007AMTV	-55°C to +125°C	METAL CAN
ICL8007/D	1 - 6	DICE**

\*\*Parameter Min/Max Limits quaranteed at 25°C only for DICE orders.

#### **FEATURES**

- Of Ultra Low Input Current spalled high fadnesell C
- High Slew Rate 6V/µs .. (\$ etc//) egation augal
- Wide Input Common Mode Voltage
- 1MHz Band Width
- Excellent Stability
- Ideal for Unity Gain Applications

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range65°C to	+150°C

Operating Temperature Range	
8007M, 8007AM	-55°C to +125°C
8007C, 8007AC	
Lead Temperature (Soldering, 10sec)	300°C
Output Short-Circuit Duration (Note 3)	

#### NOTES:

- Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.

   For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

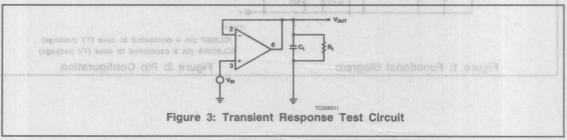
   Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- 4. For Design only, not 100% tested.

### ELECTRICAL CHARACTERISTICS (VS = ±15V unless otherwise specified)

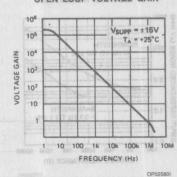
				8007C	07C 80		8007AM & 8007AC				
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
The following specifications	s apply for $T_A = 25^{\circ}C$ :			ago.	Nov. et	nom n	orome urc a s	night o	de an	eililgen Saaudi	s em
Input Offset Voltage	R <sub>S</sub> ≤ 100kΩ		10	20		20	50	22 2 2 2	15	30	mV
Input Offset Current			0.5	EXOAS		0.5	TARBY	May .	0.2	TRAS	рА
Input Bias Current (either input)			2.0	20		3.0	50		0.5	4.0	pA
Input Resistance			106	ASU B		10 <sup>6</sup>	470	0°C 10	106	YTON	МΩ
Input Capacitance		No in	2.0	E-01		2.0		Men II	2.0	CTANE	pF
Large Signal Voltage Gain	$R_L \ge 2k\Omega$ , $V_{OUT} = \pm 10V$	50,000			20,000			20,000		DIM ASS	V/V
Output Resistance			75	Sain		75			75	FILE	Ω
Output Short-Circuit Current			25	-		25			25	DA-18810.81	mA
Supply Current			3.4	5.2	Alux C	3.4	6.0	emb anny	3.4	6.0	mA
Power Consumption			102	156		102	180		102	180	mW
Slew Rate			6.0			6.0		2.5	6.0		V/µs
Unity Gain Bandwidth			1.0			1.0			1.0		MHz
Risetime	$C_L \le 100 pF$ , $R_L = 2k\Omega$		300			300	2000	1	300		ns
Overshoot	$C_L \le 100 pF, R_L = 2k\Omega$		10	17-2112	so we	10	in		10		%

The following specifications apply for  $0^{\circ}\text{C} \le T_{A} \le +70^{\circ}\text{C}$  (8007C and 8007AC), and  $+55^{\circ}\text{C} \le T_{A} \le +125^{\circ}\text{C}$ (8007M and 8007AM):

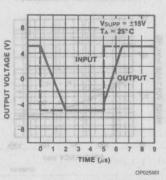
Input Voltage Range	100	±10	±12	580	±10	±12	10	±10	±12	O CONTRACT	V
Common Mode Rejection Ratio	TURNO De -	70	90		70	90		86	95	Uffers .	dB
Supply Voltage Rejection Ratio			70	300		70	600		70	200	μV/V
Large Signal Voltage Gain		25,000		REXPT	15,000			15,000			V/V
Output Voltage Swing	$R_L \ge 10k\Omega$ $R_L \ge 2k\Omega$	±12 ±10	±14 ±13	205.4	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Bias Current (either input)	T <sub>A</sub> = + 125°C T <sub>A</sub> = + 70°C		2.0			50	.>-	James &	1.0		nA pA
Average Temperature Coefficient of Input Offset Voltage	(Note 4)		1	75	0 }		75	5	5-10	50	μV/°C



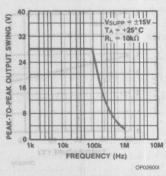
#### TYPICAL PERFORMANCE CHARACTERISTICS TO A RAND 

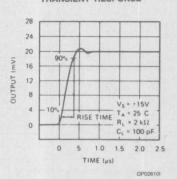
#### VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



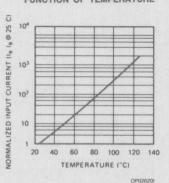
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



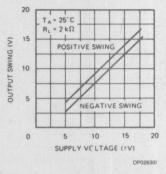
TRANSIENT RESPONSE



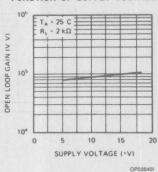
INPUT BIAS CURRENT AS A **FUNCTION OF TEMPERATURE** 



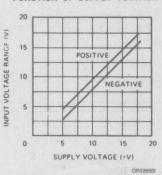
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



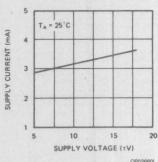
OPEN LOOP VOLTAGE GAIN AS A **FUNCTION OF SUPPLY VOLTAGE** 



INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

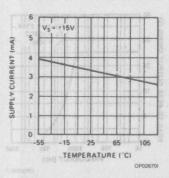


QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

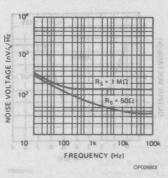


### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

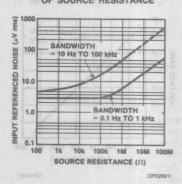
QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



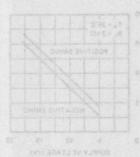
INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

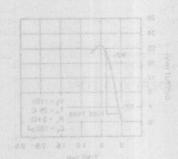


WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE

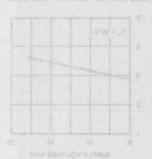


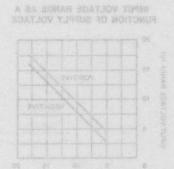
For additional information, see Application Note A005.













## ICL8021/ICL8022/ ICL8023

## Low Power Bipolar Operational Amplifier

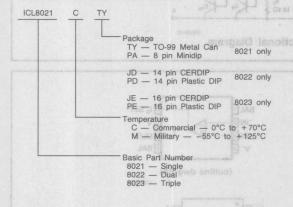
#### GENERAL DESCRIPTION

The Intersil ICL8021 series are low power operational amplifiers specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 series can be tailored to a particular application by adjusting an external resistor, R<sub>SET</sub>, which controls the quiescent current. This is advantageous because I<sub>Q</sub> can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

Other features of the 8021 series include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-forpin compatibility with the 741.

The Intersil 8022 (8023) consists of two (three) low power operational amplifiers in a single 14(16)-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R<sub>SET</sub>, which controls the quiescent current of that amplifier.

#### **ORDERING INFORMATION**



	MERSIL
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#### **FEATURES**

- V<sub>OS</sub> = 3mV Max (Adjustable to Zero)
- ±1.5V to ±18V Power Supply Operation
- Power Consumption 20μW @ ±1V
- Input Bias Current 30nA Max
   Internal Compensation
- Pin-For-Pin Compatible With 741
- Short Circuit Protected

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8021/D ICL8021CJA ICL8021CBA ICL8021CPA ICL8021CTY ICL8021MJA ICL8021MJD ICL8021MTY	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C -55°C to +125°C -55°C to +125°C -55°C to +125°C	DICE** 8 Lead CERDIP 8 Lead S.O.I.C 6 Lead MINIDIP 8 Lead Metal Can 8 Lead CERDIP 14 Lead CERDIP 8 Lead Metal Can
ICL8022/D ICL8022CJD ICL8022CPD ICL8022MJD	0°C to 70°C 0°C to 70°C -55°C to +125°C	DICE 14 Lead CERDIP 14 Lead MINIDIP 14 Lead CERDIP
ICL8023/D ICL8023CJE ICL8023CPE ICL8023MJE	0°C to 70°C 0°C to 70°C -55°C to +125°C	DICE 16 Lead CERDIP 16 Lead MINIDIP 16 Lead CERDIP

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

## ICL8021/ICL8022/ICL8023



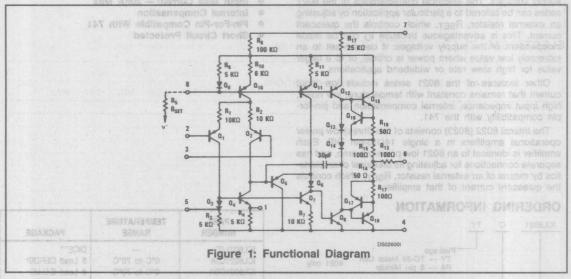
#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	±18V
Differential Input Voltage (Note 1)	
Common Mode Input Voltage (Note 1)	±15V
Output Short Circuit Duration	ndefinite
Power Dissipation (Note 2)	.300mW
	.300mW

Operating Tomporature Bange	
Operating Temperature Range 8021M	INCULTATION LA
8021C	0°C to +70°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10sec	e)+300°C

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.



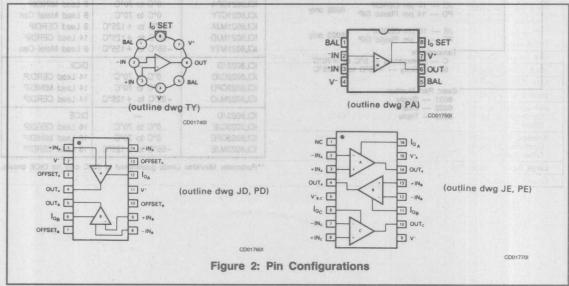


Figure 3: Voltage Offset Null Circuit

THE PERSON NAMED IN COLUMN TWO IS NOT THE PERSON NAMED IN COLUMN TO THE PERSON NAMED IN COLUMN T		Annual Service	5384		C2442.5 C244C0			
CHARACTERISTICS	TEST CONDITIONS		8021M			8021C		UNIT
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	ONI
The following specifications apply for TA:	= 25°C:		The street			TO HELE		
Input Offset Voltage	R <sub>S</sub> ≤ 100kΩ	TOWN I	2	3		2	6	mV
Input Offset Current	RISTICS*	STOA	.5	7.5	AMS	.7	10	nA
Input Bias Current	se specified.)	ivnertio	5	20	OL VE	1 7 V	30	nA
Input Resistance	Kerlense Allense et al.	3	10		3	10		МΩ
Input Voltage Range	V <sub>SUPPLY</sub> = ±15V	±12	±13	39 70	±12	±13	DRIVE.	٧
Common Mode Rejection Ratio	R <sub>S</sub> ≤ 10kΩ	70	80	THE	70	80	60	dB
Supply Voltage Rejection Ratio	$R_S \le 10k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2	ponent O	kΩ
NAME OF THE PARTY	R <sub>L</sub> ≥ 20kΩ, V <sub>SUPPLY</sub> = ±15V	±12	±14		±12	±14		V
Output Voltage Swing	$R_L \ge 10k\Omega$ , $V_{SUPPLY} = \pm 15V$	±11	±13		±11	±13	andrea:	٧
Output Short-Circuit Current	I was been a superior of the superior	4	±13	ALLES MA		±13		mA
Power Consumption	V <sub>OUT</sub> = 0	1 9	360	480	A SH	360	600	μW
Slew Rate (Unity Gain)	Au GC e of	J 101 3	0.16		Jan 1	0.16	0	V/µs
Unity Gain Bandwidth	$R_L = 20k\Omega$ , $V_{IN} = 20mV$		270			270	-	kHz
Transient Response (Unity Gain)	$R_L = 20k\Omega$ , $V_{IN} = 20mV$	1 0 0					- James	60
Risetime		1 5	1.3			1.3		μs
Overshoot			10			10		%
The following specifications apply for 0°C	$\leq$ T <sub>A</sub> $\leq$ +70°C (8021C) and -55°C	$C \leq T_A \leq$	+ 125°C	(8021M)	1		land ;	
Input Offset Voltage	D- < 1010	100°	2.0	4.0	. 901	2.0	7.5	mV
Input Offset Current	R <sub>S</sub> ≤ 10kΩ   BAUYARBAMST		1.0	(44) 3)	CURRE	1.5	0 15	nA
Input Bias Current	RISTESPACE		10	32		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	R <sub>S</sub> ≤ 10kΩ	119	5	THEOS	arup e	5 5 7	WEJE	μV/°(
Average Temperature Coefficient of Input Offset Current	CT TO THE TOTAL OF		1.7	BREEK		0.8		pA/°
Large Signal Voltage Gain	$R_L = 10k\Omega$	50	200		50	200	7-12	V/m\
Output Voltage Swing	$R_1 \ge 10k\Omega$	±10	±13	TO LET	±10	±13		V

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## ICL8021/ICL8022/ICL8023

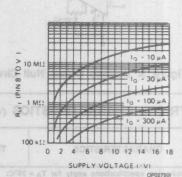
## **BINTERSIL**

#### QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 to V<sup>-</sup>)

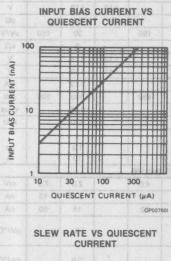
Vs	10μΑ	30μΑ	100μΑ	300μΑ
±1.5	1.5ΜΩ	470kΩ	150kΩ	-
±3	3.3MΩ	1.1ΜΩ	330kΩ	100kΩ
±6	7.5MΩ	2.7ΜΩ	750kΩ	220kΩ
±9	13ΜΩ	4ΜΩ	1.3ΜΩ	350kΩ
±12	18ΜΩ	5.6ΜΩ	1.5ΜΩ	510kΩ
±15	22ΜΩ	7.5ΜΩ	2.2ΜΩ	620kΩ

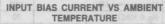


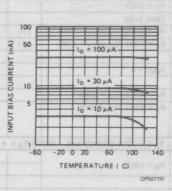


#### TYPICAL PERFORMANCE CHARACTERISTICS\*

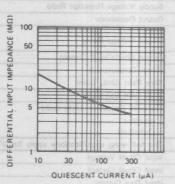
 $(T_A = +25$ °C,  $V_S = \pm 6V$ ,  $I_Q = 30\mu A$  unless otherwise specified.)

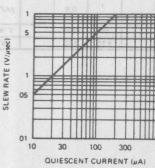




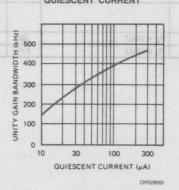


DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT

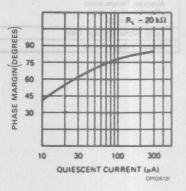




FREQUENCY RESPONSE VS
QUIESCENT CURRENT

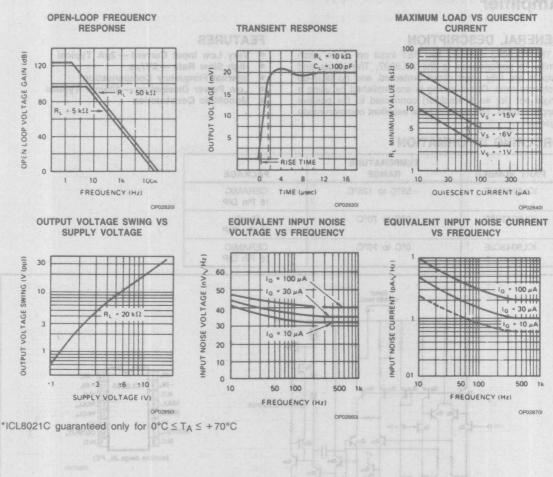


PHASE MARGIN VS QUIESCENT CURRENT



## ICL8021/ICL8022/ICL8023

### TYPICAL PERFORMANCE CHARACTERISTICS\* (CONT.)



# ICL8043 **Dual JFET Input Operational**



#### **GENERAL DESCRIPTION**

The ICL8043 contains two FET input op amps, each similar in performance to the ICL8007. The inputs and outputs are fully short circuit protected, and no latch-up problems exist. Offset nulling is accomplished by using a single pot (for each amplifier) connected to the positive supply voltage. The devices have excellent common mode rejection.

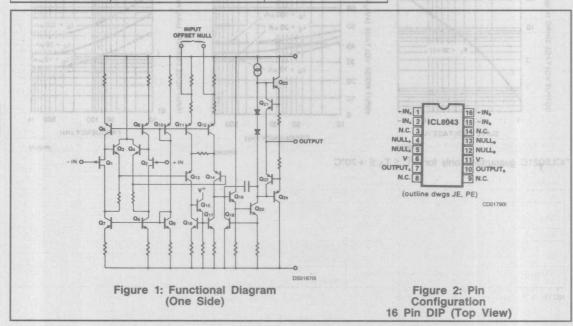
#### **FEATURES**

- Very Low Input Current 2pA Typical

- High Slew Rate 6V/µs
  Internal Frequency Compensation
  Low Power Dissipation 135mW Typical
- Monolithic Construction

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8043MJE	-55°C to 125°C	CERAMIC 16 Pin DIP
ICL8043CPE		Plastic 16 Pin DIP
ICL8043CJE	0°C to 70°C	CERAMIC 16 Pin DIP



**BINTERSIL** 

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage±18V	Operating Temperature Range
Internal Power Dissipation (Note 1)500mW	8043M55°C to +125°C
Differential Input Voltage±30V	8043C 0°C to +70°C
Input Voltage (Note 2)±15V	Lead Temperature (Soldering, 10sec)300°C
Voltage between Offset Null and V + ±0.5V	Output Short-Circuit Duration
Storage Temperature Range -65°C to +150°C	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. Rating applies for case temperatures to 125°C; derate linearly at 9mW/°C for ambient temperatures above +95°C.

2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

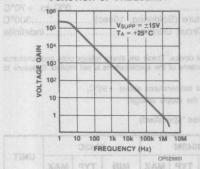
#### **ELECTRICAL CHARACTERISTICS** (V<sub>SUPPLY</sub> = ±15V unless otherwise specified)

(but	par	- NHT YORBUDBAA	1	3043M	(19)	TOKELOS	3043C		199
SYMBOL CHARAC	CHARACTERISTIC	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
The following sp	ecifications apply for T <sub>A</sub> = 25°C:	BRUTAR PROOF TO			324	T 05550	Mattern	LETT	
Vos	Input Offset Voltage	R <sub>S</sub> < 100kΩ		10	20		20	50	mV
los	Input Offset Current		107 6	0.5			0.5		рА
IIN	Input Current (either input)			2.0	20		3.0	50	pA
RIN	Input Resistance		The state of	106		Or Dealers Con Long	106	100	мΩ
CIN	Input Capacitance		1 1	2.0			2.0	THE STREET	pF
Av	Large Signal Voltage Gain	$R_L > 2k\Omega$ , $V_{out} = \pm 10V$	50,000			20,000	-	12	V/V
Ro	Output Resistance		7	75			75	0	Ω
Isc	Output Short-Circuit Current	STATE SALES NAMED IN	fi.	25	3/2 7 99	199 30	25	25 10	mA
ISUPPLY	Supply Current (Total)		GI 2	4.5	6	AV 154	4.5	6.8	mA
PDISS	Power Consumption		1	135	180	.0	135	204	mW
SR one are	Slew Rate	957 707 76 95 98 0		6.0	0.0	1.0.1	6.0		V/µs
GBW BOAT	Unity Gain Bandwidth	(O") SRUTARBAWSY		1.0		(#40) (#80E) T	1.0		MHz
CURRENT AS A	Transient Response (Unity Gain) Risetime Overshoot	$C_L < 100pF$ , $R_L = 2k\Omega$	MI B-FA	300	A MIAE	LTAGE	300	PEN LO	ns %
The following sp	ecifications apply for 0°C < T <sub>A</sub> < +	70°C (8043C), -55°C < TA <	+ 125°C	(8043M)	-				1 100
ΔVIN	Input Voltage Range		±10	±12	frat.	±10	±12	177	V
CMRR	Common Mode Rejection Ratio		70	90		70	90	38-1	dB
PSRR	Supply Voltage Rejection Ratio		70 9	70	300		70.	600	μV/V
Ay	Large Signal Voltage Gain	TAX I I I I	25,000			15,000			V/V
		$R_L > 10k\Omega$	±12	±14	STATE OF THE PARTY	±12	±14	101	V
ΔVο	Output Voltage Swing	$R_L > 2k\Omega$	±10	±13		±10	±13		V
Vos	Input Offset Voltage		- 9	15	30		30	60	mV
		T <sub>A</sub> = +125°C		2.0	15				o nA
IIN	Input Current (either input)	T <sub>A</sub> = +70°C					50	175	рА
ΔVOS/ΔT	Average Temperature Coefficient of Input Offset Voltage	(Note 3)		75	調士	OFE STRONG VIE	75	10	μV/°(

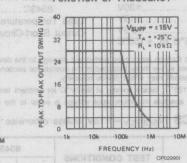
NOTE: 3. For Design only, not 100% tested.

### TYPICAL PERFORMANCE CHARACTERISTICS SOMITAR MUMIXAM STUJORBA

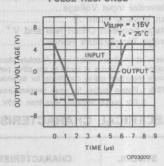
OPEN LOOP VOLTAGE GAIN AS A OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



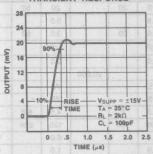
FUNCTION OF FREQUENCY PULSE RESPONSE



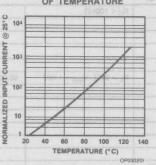
VOLTAGE FOLLOWER LARGE-SIGNAL



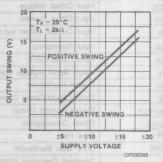
TRANSIENT RESPONSE



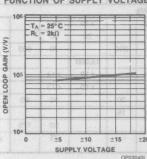
INPUT CURRENT AS A FUNCTION OF TEMPERATURE



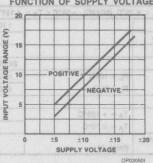
OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



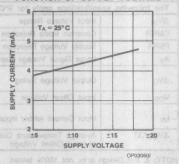
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE RANGE AS A **FUNCTION OF SUPPLY VOLTAGE** 

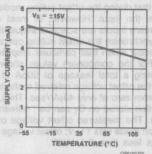


QUIESCENT SUPPLY CURRENT AS A **FUNCTION OF SUPPLY VOLTAGE** 

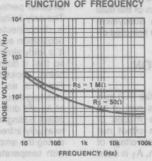


### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

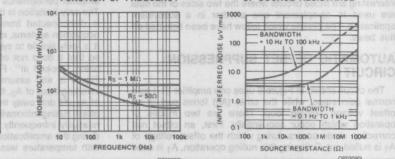
TOTAL QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A **FUNCTION OF FREQUENCY** 



WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



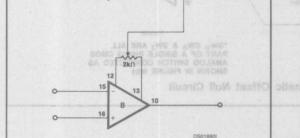


Figure 3: Offset Voltage Null Circuit

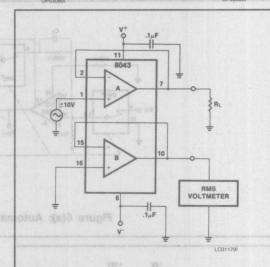


Figure 4: Channel Separation Test Circuit

#### CHANNEL SEPARATION

Channel separation or crosstalk is measured using the circuit of Figure 4. One amplifier is driven so that its output swings ±10V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Figure 5.

Channel Separation = 20 log 
$$\left(\frac{V_{OUT}(A)}{V_{IN}(B)}\right)$$

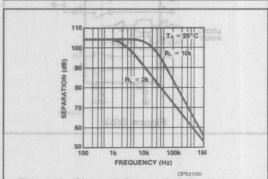


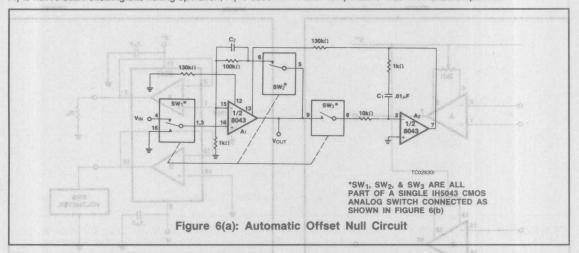
Figure 5: Channel Separation Performance

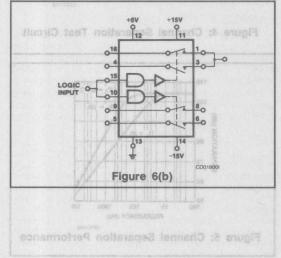
There are those which use the two-in-one package concept simply to save circuit-board space and cost, but more interesting are those circuits where the two sides of the dual are used to complement one another in a subsystem application. The circuits which follow have been selected on this basis.

## AUTOMATIC OFFSET SUPPRESSION CIRCUIT

The circuit shown in Figure 6 uses one amplifier  $(A_1)$  as a normal gain stage, while the other  $(A_2)$  forms part of an offset voltage zeroing loop. There are two modes of operation which occur sequentially. First, an offset null correction mode occurs during which the offset voltage of  $A_1$  is nulled out. Following this nulling operation,  $A_1$  is used

The advantage of this circuit is that it allows chopper amplifier performance to be achieved at one-tenth the cost. The only limitation is that during the offset nulling mode,  $A_1$  is disconnected from the input. However, in most data acquisition systems, many inputs are scanned sequentially. It is fairly simple to synchronize the offset nulling operation so that it does not occur when that particular amplifier is being "looked at". For the component values shown in Figure 3, and assuming a total leakage of 50pA at the inverting input of  $A_2$ , the offset voltage referred to the input of  $A_1$  will drift away from zero at only  $40\mu\text{V/sec}$ . Thus, the offset nulling information stored on  $C_1$  can be "refreshed" relatively infrequently. The measured offset voltage of  $A_1$  during the amplification mode was  $11\mu\text{V}$ ; offset voltage drift with temperature was less than  $0.1\mu\text{V}/^{\circ}\text{C}$ .

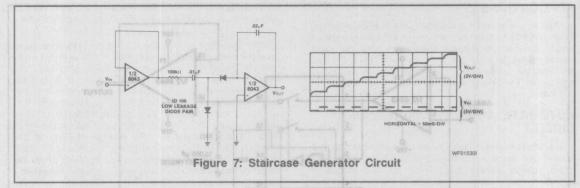


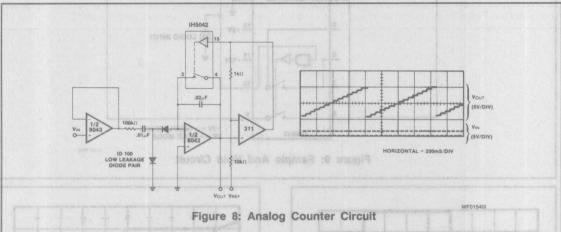


CHANNEL SEPARATION

Channel separation or crosstelk is measured using the circuit of Figure 4. One amplifier is diven so that its output swings ±10V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Figure 5.

thancel Separation = 20 log (Volv (B)





#### STAIRCASE GENERATOR

The circuit shown in Figure 7 is a high input impedance version of the so-called "diode pump" or staircase generator. Note that charge transfer takes place at the negative-going edge of the input-signal.

The most common application for staircase generators is in low cost counters. By resetting the capacitor when the output reaches a predetermined level, the circuit may be made to count reliably up to a maximum of about 10. A straightforward circuit using a LM311 for the level detector, and a CMOS analog gate to discharge the capacitor, is shown in Figure 8. An important property of this type of counter is the ease with which the count can be changed; it is only necessary to change the voltage at which the comparator trips. A low cost A-D converter can also be designed using the same principle since the digital count between reset periods is directly proportional to the analog voltage used as a reference for the comparator.

A considerable amount of hysteresis is used in the comparator shown in Figure 8. This ensures that the capacitor is completely discharged during the reset period. In a more sophisticated circuit, a dual comparator "window detector" could be used, the lower trip point set close to

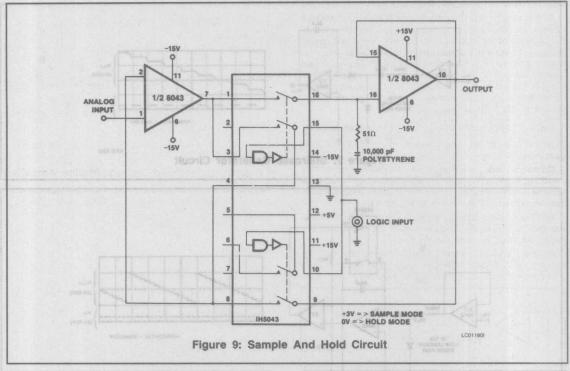
ground to assure complete discharge. The upper trip point could then be adjusted independently to determine the pulse count.

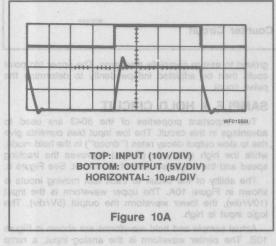
#### SAMPLE & HOLD CIRCUIT

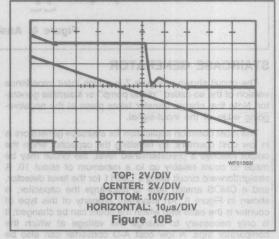
Two important properties of the 8043 are used to advantage in this circuit. The low input bias currents give rise to slow output decay rates ("droop") in the hold mode, while the high slew rate  $(6V/\mu s)$  improves the tracking speed and the response time of the circuit. See Figure 6.

The ability of the circuit to track fast moving inputs is shown in Figure 10A. The upper waveform is the input (10V/div), the lower waveform the output (5V/div). The logic input is high.

Actual sample and hold waveforms are shown in Figure 10B. The center waveform is the analog input, a ramp moving at about 67V/ms, the lower waveform is the logic input to the sample & hold; a logic "1" initiates the sample mode. The upper waveform is the output, displaced by about 1 scope division (2V) from the input to avoid superimposing traces. The hold mode, during which the output remains constant, is clearly visible. At the beginning of a sample period, the output takes about 8 µs to catch up with the input, after which it tracks until the next hold period.







#### **INSTRUMENTATION AMPLIFIER**

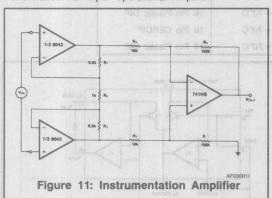
A dual JFET-input operational amplifier is an attractive component around which to build an instrumentation amplifier because of the high input resistance. The circuit shown in Figure 11 uses the popular triple op-amp approach. The output amplifier is a High Speed 741 (741 HS, slew rate guaranteed  $\geq 0.7 V/\mu s)$  so that the high slew rate of the 8043 is utilized to the full extent. Input resistance of the circuit (either input, regardless of gain configuration) is in excess of  $10^{12}$  ohms.

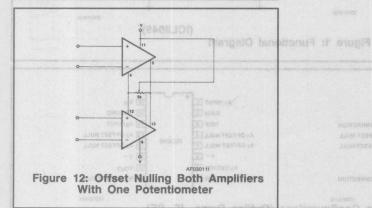
For the component values shown, the overall amplifier gain is 200 (front end gain =  $\frac{2R_1 + R_2}{R_2}$ , back end gain, =  $R_6/R_4$ ).

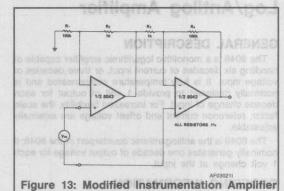
Common mode rejection is largely determined by the matching between  $R_4$  and  $R_5$ , and  $R_6$  and  $R_7$ . In applications where offset nulling is required, a single potentiometer can be connected as shown in Figure 12.

Another popular circuit is given in Figure 13. In this case the gain is  $1+R_1/R_2$ , and the CMRR determined by the match between  $R_1$  and  $R_4$ ,  $R_2$  and  $R_3$ .

For more information on FET input operational amplifiers, see Intersil Application Bulletin A005 "The 8007: A High Performance FET-input Operational Amplifier."







4

#### **GENERAL DESCRIPTION**

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

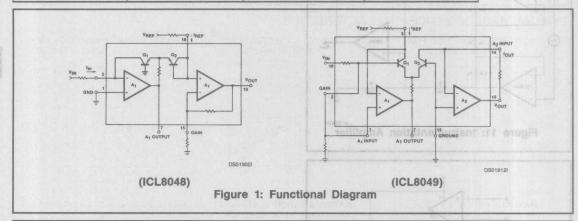
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

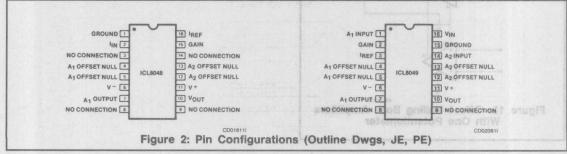
#### FEATURES mustard me bland of distribution benefits the normal

- 1/2% Full Scale Accuracy
- Temperature Compensated for 0°C to +70°C Operation
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual JFET-Input Op-Amps

#### ORDERING INFORMATION

PART NUMBER	ERROR (25°C)	TEMPERATURE RANGE	PACKAGE
ICL8048BCJE	30mV	0°C to +70°C	16 Pin CERDIP
ICL8048BCPE	30mV	0°C to +70°C	16 Pin Plastic DIP
ICL8048CCJE	60mV	0°C to +70°C	16 Pin CERDIP
ICL8048CCPE	60mV	0°C to +70°C	16 Pin Plastic DIP
ICL8049BCJE	10mV	0°C to +70°C	16 Pin CERDIP
ICL8049BCPE	10mV	0°C to +70°C	16 Pin Plastic DIP
ICL8049CCJE	25mV	0°C to +70°C	16 Pin CERDIP
ICL8049CCPE	25mV	0°C to +70°C	16 Pin Plastic DIP





## ICL8048/ICL8049

#### **ABSOLUTE MAXIMUM RATINGS (ICL8048)**

Supply Voltage	±18V
I <sub>IN</sub> (Input Current)	
IRFF (Reference Current)	
Voltage between Offset Null and V+	±0.5V
Power Dissipation	750mW

Operating Temperature Range 0°C to +70°C
Output Short Circuit DurationIndefinite
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10sec)300°C

**ELECTRICAL CHARACTERISTICS (ICL8048)**  $V_S = \pm 15V$ ,  $T_A = 25$ °C,  $I_{REF} = 1$ mA, scale factor adjusted for 1V/decade unless otherwise specified.

	Administration of the second	8048BC			8048CC			(en) mojordi
PARAMETER AND THE PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Dynamic Range I <sub>IN</sub> (1nA - 1mA) V <sub>IN</sub> (10mV - 10V)	R <sub>IN</sub> = 10kΩ	120 60	DHIO 2	seimo ,	120 60	and a	00) 80	dB dB
Error, % of Full Scale	T <sub>A</sub> = 25°C, I <sub>IN</sub> = 1nA to 1mA	O Tea	.20	0.5	. 19:	.25	1.0	%
Error, % of Full Scale	$T_A = 0$ °C to +70°C, $I_{IN} = 1$ nA to 1mA	Venor	.60	1.25		.80	2.5	%
Error, Absolute Value	T <sub>A</sub> = 25°C, I <sub>IN</sub> = 1nA to 1mA	Vis on	12	30		14	60	mV
Error, Absolute Value	$T_A = 0$ °C to $+70$ °C $I_{IN} = 1$ nA to 1mA	+ 0/ 0/	36	75		50	150	dA mV
Temperature Coefficient of Vour	I <sub>IN</sub> = 1nA to 1mA	V	0.8		Incomple	0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5	777		2.5		mV/V
Offset Voltage (A <sub>1</sub> & A <sub>2</sub> )	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for I <sub>IN</sub> = 100μA	Professor	250			250	A) spall	μV(RMS)
(SMRW) es	$R_L = 10k\Omega$	±12	±14		±12	±14	sainti	V

#### TYPICAL PERFORMANCE CHARACTERISTICS

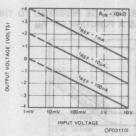
 $R_L = 2k\Omega$ 

## TRANSFER FUNCTION FOR CURRENT INPUTS

Output Voltage Swing

Power Consumption

Supply Current



TRANSFER FUNCTION FOR VOLTAGE INPUTS

±10

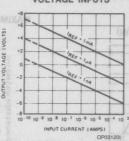
±13

150

5

200

6.7



SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT

±13

150

5

200

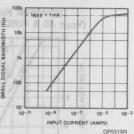
6.7

V

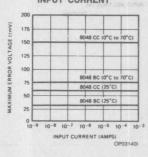
mW

mA

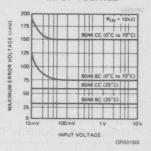
±10



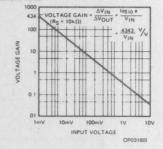
MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT



MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR  $R_{S}=10 \mathrm{k} \Omega$ 



## ICL8048/ICL8049



#### **ABSOLUTE MAXIMUM RATINGS (ICL8049)**

Supply Voltage	±18V
VIN (Input Voltage)	±15V
IREF (Reference Current)	2mA
Voltage between Offset Null and V+	±0.5V
Power Dissipation	750mW

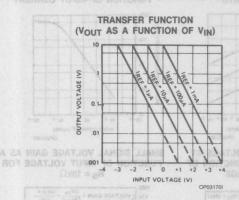
Operating Temperature Range0°C	to +70°C
Output Short Circuit Duration	. Indefinite
Storage Temperature Range65°C to	+150°C
Lead Temperature (Soldering, 10sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

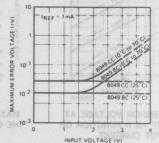
**ELECTRICAL CHARACTERISTICS (ICL8049)**  $V_S = \pm 15V$ ,  $T_A = 25$ °C,  $I_{REF} = 1$ mA, scale factor adjusted for 1 decade (out) per volt (in), unless otherwise specified.

50 00	68		8049BC	) FI		8049C	701 - N	mail) say
PARAMETER 3.0	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Dynamic Range (V <sub>OUT</sub> )	V <sub>OUT</sub> = 10mV to 10V	60	ADT W	MI I	60			dB
Error, Absolute Value	$T_A = 25$ °C, $OV \le V_{IN} \le 3V$	CIT F MI	3	10		.5	25	mV
Error, Absolute Value	$T_A = 0$ °C to +70°C, $0V \le V_{IN} \le 3V$	Ant	20	75		30	150	mV
Temperature Coefficient, Referred to VIN	V <sub>IN</sub> = 3V	Part C	0.38		100	0.55	A CHINESE	mV/°C
Power Supply Rejection Ratio	Referred to Input, for V <sub>N</sub> = 0V	BUILDING	2.0	88		2.0	F <sub>1</sub> A) ag	μ\/\
Offset Voltage (A <sub>1</sub> & A <sub>2</sub> )	Before Nulling	et Wil You	15	25		15	50	mV
Wideband Noise	Referred to Input, for VIN = 0V		26	原		26	ige Swin	μV(RMS)
999 150 200 mW	$R_L = 10k\Omega$	±12	±14		±12	±14	nodgmu	V
Output Voltage Swing	$R_L = 2k\Omega$	±10	±13		±10	±13	Ins	mo V
Power Consumption			150	200		150	200	mW
Supply Current	60118	Mall	5	6.7	JELAG	5	6.7	mA

#### TYPICAL PERFORMANCE CHARACTERISTICS



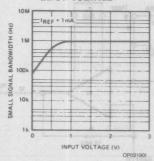






### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE



#### **ICL8048 DETAILED DESCRIPTION**

The ICL8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S[e \ qV_{BE}/kT_{-1}] \tag{1}$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S e^{qV_{BE}/kT}$$
 (2)

(R) + (R) From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the VBF difference ( $\Delta V_{BF}$ ) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10} \left[ \frac{I_{C1}}{I_{C2}} \right]$$
 (3)

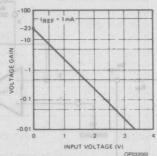
Referring to Figure 3, it is clear that the potential at the collector of Q2 is equal to the A VBE between Q1 and Q2. The output voltage is  $\Delta$  V<sub>BF</sub> multiplied by the gain of A<sub>2</sub>:

$$V_{OUT} = -2.303 \left( \frac{R_1 + R_2}{R_2} \right) \left( \frac{kT}{q} \right) \log_{10} \left[ \frac{I_{IN}}{I_{REF}} \right]$$
 (4)

The expression 2.303 x Thas a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio (R<sub>1</sub> + R<sub>2</sub>)/R<sub>2</sub> is chosen to be 16.9 For this scale factor to hold constant as a function of temperature, the (R<sub>1</sub> + R<sub>2</sub>)/R<sub>2</sub> term must have a 1/T characteristic to compensate for kT/q.

In the ICL8048 this is achieved by making R<sub>1</sub> a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R2 is external and should be a low T.C. type; it should have a nominal value of  $1k\Omega$  to provide 1 volt/ decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R1.

#### SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE



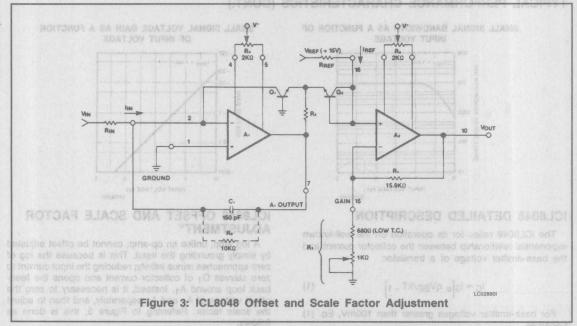
#### ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT'

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q1 of collector current and opens the feedback loop around A1. Instead, it is necessary to zero the offset voltage of A1 and A2 separately, and then to adjust the scale factor. Referring to Figure 3, this is done as follows:

- Temporarily connect a 10kΩ resistor (R<sub>0</sub>) between pins 2 and 7. With no input voltage, adjust R4 until the output of A1 (pin 7) is zero. Remove R0. Note that for a current input, this adjustment is not necessary since the offset voltage of A1 does not cause any error for current-source inputs.
- Set I<sub>IN</sub> = I<sub>REF</sub> = 1mA. Adjust R<sub>5</sub> such that the output of A2 (pin 10) is zero.
- 3) Set  $I_{IN} = 1\mu A$ ,  $I_{REF} = 1 \text{ mA}$ . Adjust  $R_2$  for  $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting  $I_{IN} = 1 \mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100 µA to 1mA, it would be better to set  $I_{IN} = 100\mu$ A in Step #3. Similarly, adjustment for other scale factors would require different I<sub>IN</sub> and V<sub>OUT</sub> values.

\*See A053 for an automatic offset nulling circuit.



#### ICL8049 DETAILED DESCRIPTION

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific  $\triangle V_{BE}$  between  $Q_1$  and  $Q_2$  (Figure 4). This  $V_{BE}$  difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C_1}}{I_{C_2}} = \exp\left[\frac{q\triangle V_{BE}}{kT}\right]$$

When numerical values for q/kT are put into this equation, it is found that a  $\triangle V_{BE}$  of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R1 and R2. In order that scale factors other than one decade per volt may be selected, R2 is external to the chip. It should have a value of  $1k\Omega_{\rm c}$  adjustable  $\pm 20\%$ , for one decade per volt. R1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right]$$
 (6)

Substituting Vout = Iout x Rout gives:

$$V_{OUT} = R_{OUT} I_{REF} \exp \left[ \frac{-R_2}{(R_1 + R_2)} x \frac{qV_{IN}}{kT} \right]$$
 (7)

For voltage references equation 7 becomes

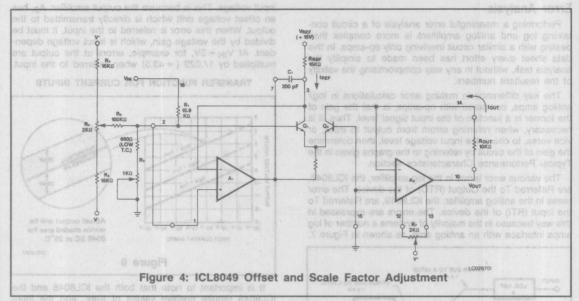
$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp \left[ \frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right]$$
(8)

## ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT\*

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A2. This is accomplished by reverse biasing the base-emitter of Q2. A2 then operates as a unity gain buffer with a grounded input. The second step forces  $V_{IN}=0$ ; the output is adjusted for  $V_{OUT}=10V$ . This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 4, the exact procedure for 1 decade/volt is as follows:

- Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q<sub>2</sub>. Adjust R<sub>7</sub> for V<sub>OUT</sub> = 0V. Disconnect the input from +15V.
- Connect the input to Ground. Adjust R<sub>4</sub> for V<sub>OUT</sub> = 10V. Disconnect the input from Ground.
- Connect the input to a precise 2V supply and adjust R<sub>2</sub> for V<sub>OUT</sub> = 100mV.

The procedure outlined above optimizes the performance over a 3-decade range at the output (i.e.,  $V_{OUT}$  from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for  $V_{OUT} = 1V$ . For other scale factors and/or starting points, different values for  $R_2$  and  $R_{REF}$  will be needed, but the same basic procedure applies. \*See A053 for an automatic offset nulling circuit.



#### APPLICATIONS INFORMATION ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048 and ICL8049, are primarily directed towards setting up 1 volt ( $\Delta V_{OUT}$ ) per decade ( $\Delta I_{IN}$  or  $\Delta V_{IN}$ ) for the log amp, or one decade ( $\Delta V_{OUT}$ ) per volt  $(\Delta V_{IN})$  for the antilog amp.

This corresponds to K = 1 in the respective transfer functions: huong lauthy out a ton at (gapt) nig consister

Log Amp: 
$$V_{OUT} = -K \log_{10} \left[ \frac{I_{IN}}{I_{REF}} \right]$$
 (9)  
Antilog Amp:  $V_{OUT} = R_{OUT} I_{REF} = 10 \frac{-V_{IN}}{K}$  (10)

Antilog Amp: 
$$V_{OUT} = R_{OUT} I_{REF} 10 \frac{-V_{IN}}{\kappa}$$
 (10)

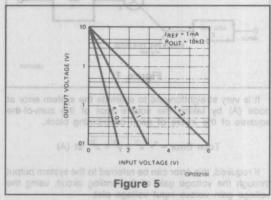
By adjusting R2 (Figure 3 and Figure 4) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Figure 5 for the log amp, and Figure 6 for the antilog amp. The nominal value of R2 required to give a specific value of K can be determined from equation 11. It should be remembered that R1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R2 by ±20%.

$$R_2 = \frac{941}{(K - .059)} \Omega$$
 (11)

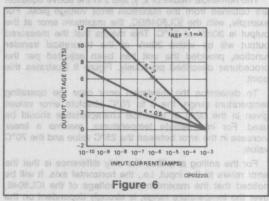
#### Frequency Compensation address of the second

Although the op-amps in both the ICL8048 and the ICL8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150 pF should be connected between Pins 2 and 7 (Figure 3). In the 8049, 200 pF between Pins 3 and 7 is recommended (Figure 4).

#### EFFECT OF VARYING "K" ON THE LOG AMPLIFIER



EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER



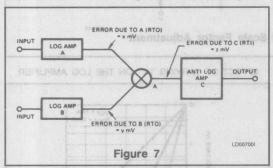
## ICL8048/ICL8049

#### **Error Analysis**

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Characteristics section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the ICL8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 7.



It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

Total Error = 
$$\sqrt{x^2 + y^2 + z^2}$$
 at (A)

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 8 illustrates this point.

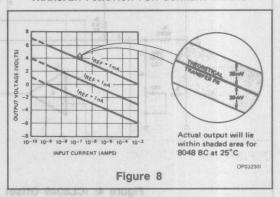
To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i.e., the horizontal axis. It will be noticed that the maximum error voltage of the ICL8049, over the temperature range, is strongly dependent on the



input voltage. This is because the output amplifier,  $A_2$ , has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At  $V_{\rm IN} = 3V$ , for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

#### TRANSFER FUNCTION FOR CURRENT INPUTS



It is important to note that both the ICL8048 and the ICL8049 require positive values of I<sub>REF</sub>, and the input (ICL8048) or output (ICL8049) currents (or voltages) respectively must also be positive. Application of negative I<sub>IRF</sub> to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

#### SETTING UP THE REFERENCE CURRENT

In both the ICL8048 and the ICL8049 the input current reference pin (IREF) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 3). This does not constitute an appreciable error provided  $V_{\rm REF}$  is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the ICL8049, a fraction of the input voltage appears on Pin 3 (Figure 4), placing a similar restraint on the value of  $V_{\rm REF}$ .

Alternatively, IREF can be provided from a true current source. One method of implementing such a current source is shown in Figure 9.

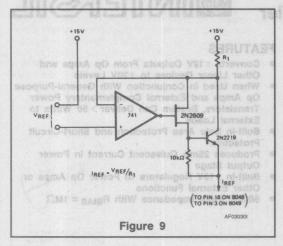
#### LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the IREF input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -Klog_{10} \left[ \frac{I_{IN}}{I_{BEF}} \right]$$
 (9)

Clearly it is possible to perform division using just one ICL8048, followed by an ICL8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the  $I_{REF}$  input not being a true virtual ground (discussed in the previous section), the circuit of Figure 9 is again recommended if the  $I_{REF}$  input is to be modulated.



#### **DEFINITION OF TERMS**

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

DYNAMIC RANGE The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the ICL8049 the dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048) or (ICL8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the ICL8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

Error, % of Full Scale =  $\frac{100 \text{ x Error, absolute value}}{\text{FullScale Output Voltage}}$ 

TEMPERATURE COEFFICIENT OF V<sub>OUT</sub> OR V<sub>IN</sub> For the ICL8048 the temperature coefficient refers to the drift with temperature of V<sub>OUT</sub> for a constant input current.

For the ICL8049 it is the temperature drift of the input voltage required to hold a constant value of  $V_{\mbox{OUT}}$ .

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (VOUT for the ICL8048, VIN for the ICL8049) to the change in the supply voltage, assuming that the log axis is held constant.

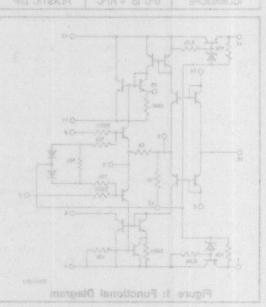
WIDEBAND NOISE For the ICL8048, this is the noise occurring at the output under the specified conditions, In the case of the ICL8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

#### **APPLICATION NOTES**

For further applications assistance, see

A007 "The ICL8048/8049 Monolithic Log-Antilog Amplifiers", by Ray Hendry



#### GENERAL DESCRIPTION

The ICL8063 is a unique monolithic power transistor driver and amplifier that allows construction of minimum chip power amplifier systems. It includes built in safe operating area circuitry, short circuit protection and voltage regulators, and is primarily intended for driving complementary output stages.

Designed to operate with all varieties of operational amplifiers and other functions, two external power transistors, and 8 to 10 passive components, the ICL8063 is ideal for use in such applications as linear and rotary actuator drivers, stepper motor drivers, servo motor drivers, power supplies, power DACs and electronically controlled orifices.

The ICL8063 takes the output levels (typically  $\pm 11V$ ) from an op amp and boosts them to  $\pm 30V$  to drive power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 supply up to 100mA to the base leads of the external power transistors.

The amplifier-driver contains internal positive and negative regulators, to power an op amp or other device; thus, only ±30V supplies are needed for a complete power amp.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL8063MJE	-55°C to +125°C	CERDIP
ICL8063CJE	0°C to +70°C	CERDIP
ICL8063CPE	0°C to +70°C	PLASTIC DIP

#### **FEATURES**

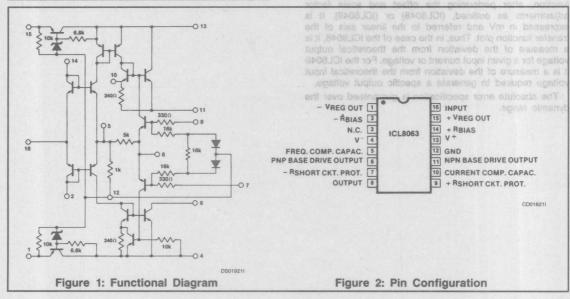
- Converts ±12V Outputs From Op Amps and Other Linear Devices to ±30V Levels
- When Used in Conjunction With General-Purpose Op Amps and External Complementary Power Transistors, System Can Deliver > 50 Watts to External Loads
- Built-in Safe Area Protection and Short-Circuit Protection
- Produces 25mA Quiescent Current in Power Output Stage
- Built-in ±13V Regulators to Power Op Amps or Other External Functions
- 500k $\Omega$  Input Impedance With RBIAS = 1M $\Omega$

DEFINITION OF TERMS

in the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is

DYNAMIC RANGE The dynamic range of the IOL8048 infers to the range of input voltages or durants over which the device is gueranteed to operate. For the IOL8049 line dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer.



#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	.±35V
Power Dissipation5	00mW
Input Voltage (Note 1)	.±30V
Regulator Output Currents	10mA

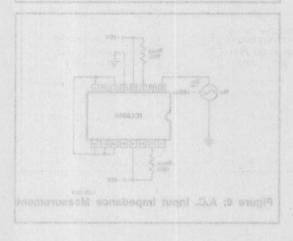
Operating Temperature Range	
ICL8063MJE	55°C to +125°C
ICL8063CPE	0°C to +70°C
ICL8063CJE	
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10sec)	

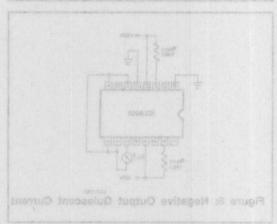
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS (TA = 25°C; VSUPPLY = ±30V)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS						
			ICL8063M		ICL8063C			UNIT	
			- 55°C	+ 25°C	+ 125°C	0°C	+ 25°C	+ 70°C	
Vos	Max. Offset Voltage	See Figure 3	150	50	50		75		mV
ГОН	Min. Positive Drive Current	See Figure 4	50	50	50		40		mA
urement pol	Max. Positive Output Quiescent Current	See Figure 5	500	250	250	W tos	300	BATCH LA	μΑ
loL	Min. Negative Drive Current	See Figure 4	25	25	25		20		mA
laL	Max. Negative Output Quiescent Current	See Figure 6	500	250	250		300		μА
VREG	Regulator Output Voltages Range	a l	±13.7 ±1.2V	±13.7 ±1.0V	±13.7 ±1.5V	±13.7 ±1.0V	±13.7 ±1.0V	±13.7 ±1.0 V	٧
IREG	Regulator Output Current	(See Note 2)	10	10			10		mA
Z <sub>IN</sub>	A.C. Input Impedance	See Figure 8		400 (Typ)	是道	unne	400 (Typ)		kΩ
VSUPPLY	Power Supply Range		±5 to ±35V				V		
la	Power Supply Quiescent Currents		10	6	6	E-92821-01	7		mA
Av	Range of Voltage Gain	See Figure 9 V <sub>IN</sub> = 8Vp-p	6±2	6±2	6±2	an pa	6±2		V/V
Vout(MIN)	Minimum Output Swing	See Figure 9; Increase VIN until VOUT flattens	±27	±27	±27		±27		٧
IBIAS	Input Bias Current	See Figure 10	100	. 100	100	g- 6Bay-	100	BY NO	μΑ

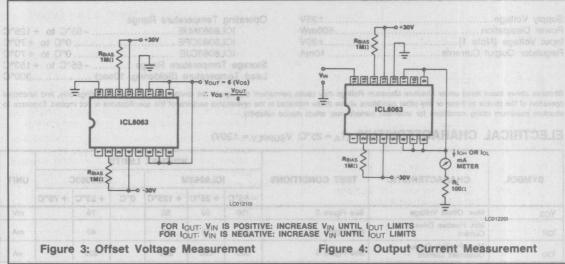
 For supply voltages less than ±30V the absolute maximum input voltage is equal to the supply voltage.
 Care should be taken to ensure that maximum power dissipation is not exceeded. NOTES:





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#### **TEST CIRCUITS**



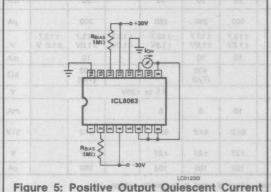
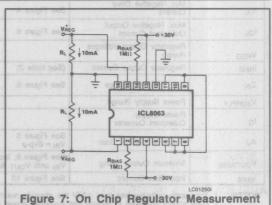
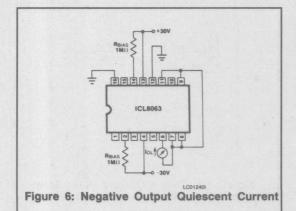
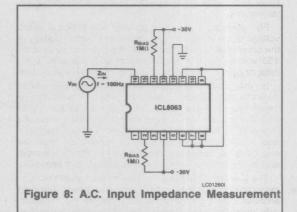


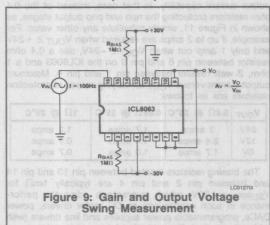
Figure 5: Positive Output Quiescent Current

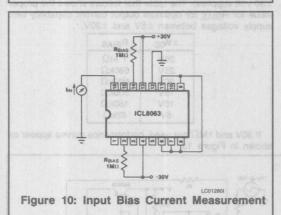






#### TEST CIRCUITS (CONT.)





#### APPLICATIONS INFORMATION

One problem faced almost every day by circuit designers is how to interface the low voltage, low current outputs of linear and digital devices to that of power transistors and darlingtons.

For example, a low level op amp has a typical output voltage range of  $\pm 6$  to  $\pm 12V$ , and output current usually on the order of about 5 milliamperes. A power transistor with a  $\pm 35$  volt supply, a collector current of 5 amperes, and a beta, or gain of 100 needs at least 50 milliamperes of drive.

In the past, connecting two transistors with widely dissimilar requirements meant that a rather ornate discrete circuit had to be built to convert the weak output signals from the first into levels large enough to drive the second. However, in addition to converting voltage and current, it was also necessary to include a number of protection circuits to guard against damage from shorts, for example, and all this design work was both tedious and expensive.

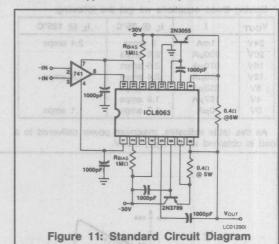
The ICL8063 provides a solution to these problems. It's a monolithic power transistor driver and power transistor amplifier circuit on the same chip, has all the necessary safe operating area circuitry and short circuit protection,

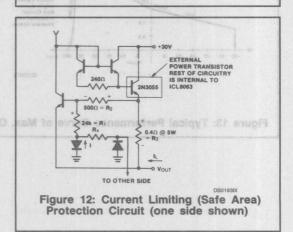
and has on-chip  $\pm 13V$  voltage regulators to eliminate the need for extra external power supplies.

# Using the ICL8063 to make a complete Power Amplifier

As Figure 11 shows, using the ICL8063 allows the circuit designer to build a power amplifier block capable of delivering ±2 amperes at ±25 volts (50 watts) to any load, with only three additional discrete devices and 8 passive components. Moreover, the circuit draws only about ±30 milliamperes of quiescent current from either of the ±30V power supplies. A similar design using discrete components would require anywhere from 50 to 100 components.

Slew rate is about the same as that of a 741 op amp, approximately  $1V/\mu s$ . Input current, voltage offset, CMRR and PSRR are also the same. Use of 1,000 picofarad compensation capacitors (three in this configuration) allows good stability down to unity gain non-inverting (the worst case). This circuit will drive a 1000pF  $C_L$  to Gnd, or in other words, the circuit can drive 30 feet of RG-58 coaxial cable for line driver applications with no problems.





1

As Figure 12 indicates, setting up a current limiting (safe area) protection circuit is straightforward. The 0.4 ohm, 5 watt resistors set the maximum current one can get out of the output. The equation this SOA circuit follows is: for VouT positive,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2} (V_{OUT} + I_L R_3 - 0.7V)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2} (V_{OUT})$$

for VouT negative,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4} (V_{OUT} + I_2 R_3 + 0.7)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4} \text{ (Vout)}$$

Solving these equations we get the following:

Vout	1 200	IL @ 25°C	IL @ 125°C
24V	1mA	3 amps	2.4 amps
20V	830µA	2.8 amps	
16V	670µA	2.6 amps	
12V	500μΑ	2.4 amps	1.8 amps
8V	333µA	2.1 amps	
4V	167μΑ	1.9 amps	
OV	0μΑ	1.7 amps	1.1 amps

As this table indicates, maximum power delivered to a load is obtained when  $V_{OUT} \ge 24V$ .

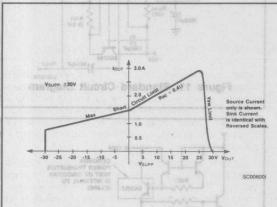
Often design requirements necessitate an unsymmetrical output current capability. In that case, instead of the 0.4 ohm resistors protecting the npn and pnp output stages, as shown in Figure 11, simply substitute any other value. For example, if up to 3 amps are required when  $V_{OUT} \ge +24V$  and only 1 amp out when  $V_{OUT} \ge -24V$ , use a 0.4 ohm resistor between pin 8 and pin 9 on the ICL8063 and a 1 ohm, 2 watt resistor between pin 7 and pin 8. Maximum output current versus  $V_{OUT}$  for varying values of protection resistors are as follows:

Vout	0.4Ω @ 25°C	0.68Ω @ 25°C	1Ω @ 25°C
24V	3 amps	1.7 amps	1.2 amps
12V	2.4 amps	1.4 amps	0.9 amps
OV	1.7 amps	1.0 amps	0.7 amps

The biasing resistors located between pin 13 and pin 14 and between pin 2 and pin 4 are typically  $1 m \Omega$  for  $V_{SUPPLY} = \pm 30 V$ , which guarantees adequate performance in such applications as DC motor drivers, power DACs, programmable power supplies and line drivers (with  $\pm 30$  volt supplies). The table that follows shows the proper value for  $R_{BIAS}$  for optimum output current capability with supply voltages between  $\pm 5 V$  and  $\pm 30 V$ .

±Vcc	RBIAS		
30V	1 ΜΩ		
25V	680kΩ		
20V	500kΩ		
15V	300kΩ		
10V	150kΩ		
5V	62kΩ		

If 30V and 1M $\Omega$  are used, performance curves appear as shown in Figure 13.



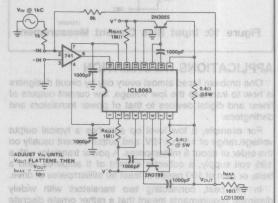
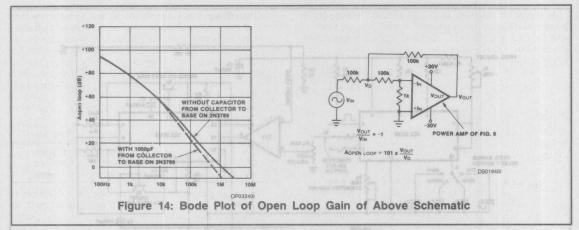
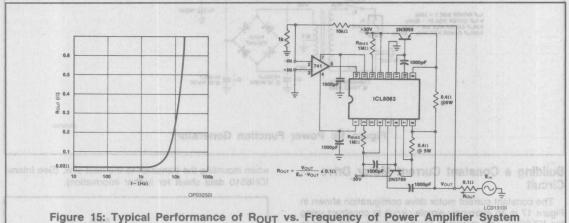


Figure 13: Typical Performance Curve of Max. Output Current Vs.  $V_{SUPP}$  For Fixed  $R_{BIAS} = 1M\Omega$ 







When buying external power transistors, careful attention should be paid to beta values. For 2N3055 and 2N3789 transistors used in this circuit, beta should be no more than 150 max at I<sub>C</sub> = 20mA and V<sub>CE</sub> = 30V. This beta value sets the quiescent current at less than 30mA when not delivering power to a load.

The design in Figure 11 will tolerate a short circuit to ground indefinitely, provided adequate heat sinking is used.

However if  $V_{OUT}$  is shunted to  $\pm 30V$  the output transistors (2N3055 and 2N3789) will be destroyed, but since the safe operating area for these devices is 4 amps at 30 volts, the problem does not occur for  $V_{SUPP} = \pm 15V$ .

A typical bode plot of the power amplifier system openloop frequency-response is shown in Figure 14. Referring to Figure 8, the schematic for this bode plot is shown in Figure 14.

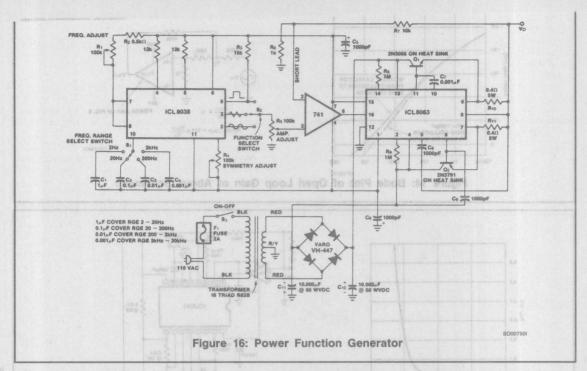
#### **Designing A Simple Function Generator**

Using a variation of the fundamental power amplifier building block described in the previous section, the

ICL8063 can be used in the design of a simple, low cost function generator (Figure 16). It will supply sine waves, triangular waves and square waves from 2 hertz to 20 kilohertz. This complete test instrument can be plugged into a standard 110VAC line for power.  $V_{OUT}$  will be up to  $\pm 25V$  (50V p-p) across loads as small as 10 ohms (about 2.5 amps maximum output current).

Capacitor working voltages should be greater than 50V DC and all resistors should be 1/2W, unless otherwise indicated. The interconnecting leads from the 741 pins 2 and 3 to their respective resistors should be kept short, less than 2 inches if possible; longer leads may result in oscillation.

Full output swing is possible to about 5kHz; after that the output begins to taper off due to the slew rate of the 741, until at 20kHz the output swing will be about  $20V_{pp}$  ( $\pm 10V$ ). This problem can be remedied by simply using an op amp with a higher slew rate, such as the LF356.



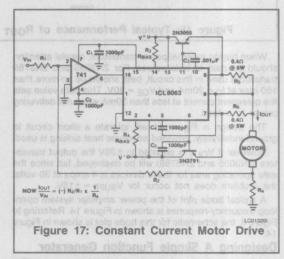
## Circuit

The constant current motor drive configuration shown in Figure 17 is an extremely simple circuit to construct using the ICL8063. This minimum device circuit can be used to drive DC motors where there is some likelihood of stalling or lock up; if the motor locks, the current drive remains constant and the system does not destroy itself. Using this approach two 6V batteries are sufficient for good performance. A 10 volt input will produce one amp of output current to drive the motor, and if the motor is stalled, lour remains at 1 amp. as flame as absol agonos (g-g VOE

For example, suppose it is necessary to drive a 24V DC motor with 1 amp of drive current. First make VSUPPLY at least 6 volts more than the motor being driven (in this case 30 volts). Next select RBIAS according to VSUPPLY from the data sheet, which indicates  $R_{BIAS} = 1M\Omega$ . Then choose R<sub>1</sub>, R<sub>2</sub>, and R<sub>a</sub> for optimum sensitivity. That means making  $R_a = 1\Omega$  to minimize the voltage drop across  $R_a$  (the drop will be 1 amp x 1 ohm or 1 volt). If 1 amp/volt sensitivity is desirable let  $R_2 = R_1 = 10k\Omega$  to minimize feedback current error. Then a ±1V input voltage will produce a ±1 amp current through the motor. The state of states in the

Capacitors should be at least 50 volts working voltage and all resistors 1/2W, except for those valued at 0.4 ohms. Power across  $R_a = I \times V = 1$  amp x 1 volt = 1 watt, so at least a 2 watt value should be used. Use large heat sinks for the 2N3055 and 2N3791 power transistors. A Delta NC-641 or the equivalent is appropriate. Use a thermal compound

Building a Constant Current Motor Drive when mounting the transistor to the heat sink. (See Intersil ICH8510 data sheet for further information).



#### Building A Low Cost 50 Watt per Channel **Audio Amplifier**

For about \$20 per channel, it is possible to build a high fidelity amplifier using the ICL8063 to drive 8 ohm speakers. A channel is defined here as all amplification between turntable or tape output and power output. (Figure 18)

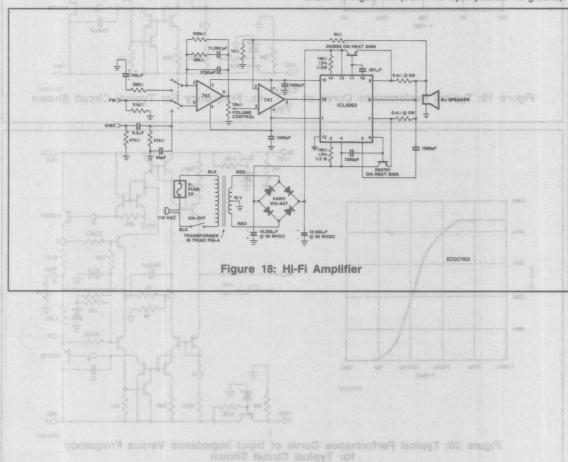
The input 741 stage is a preamplifier with R.I.A.A. equalization for records. Following the first 741 stage is a  $10 k\Omega$  control pot, whose wiper arm feeds into the power amplifier stage consisting of a second 741, the ICL8063 and the power transistors. To achieve good listening results, selection of proper resistance values in the power amplifier stage is important. Best listening is to be found at a gain value of 6 [(5k\Omega + 1k\Omega/1k\Omega = 6)]. 3 is a practical minimum, since the first stage 741 preamp puts out only  $\pm 10$  volt maximum signals, and if maximum power is necessary this value must be multiplied by 3 to get  $\pm 30$  volt levels at the output of the power amp stage.

Each channel delivers about 56 volts p-p across an 8 ohm speaker and this converts to 50 watts RMS power. This is derived as follows:

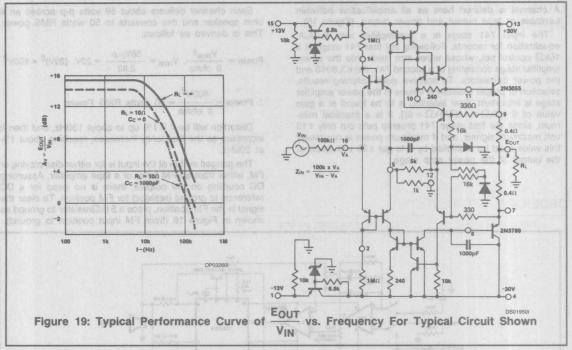
Power = 
$$\frac{V_{rms}^2}{8 \text{ ohms}}$$
,  $V_{rms} = \frac{56V_{P-P}}{2.82} = 20V$ ,  $(20V)^2 = 400V^2$   
 $\therefore \text{ Power} = \frac{400V^2}{8 \text{ ohms}} = 50 \text{ watts RMS Power.}$ 

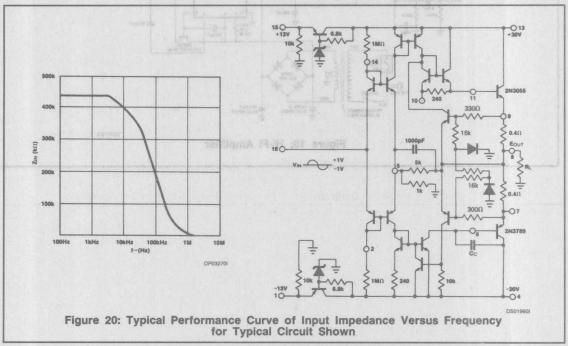
Distortion will be < 0.1% up to about 100Hz, and then it increases as the frequency increases, reaching about 1% at 20kHz.

The ganged switch at the input is for either disc playing or FM, either from an FM tuner or a tape amplifier. Assuming DC coupling on the outputs, there is no need for a DC reference to ground (resistor) for FM position. To clear the signal in the FM position, place a  $51k\Omega$ resistor to ground as shown in Figure 18 (from FM input position to ground).



ICL8063





Note: Intersil offers a hybrid power amplifier similar to that shown in Figure 11. See ICH8510/8520/8530 data sheet for details.

## LH2108/LH2308 **Dual Super-Beta Operational Amplifier**



# GENERAL DESCRIPTION

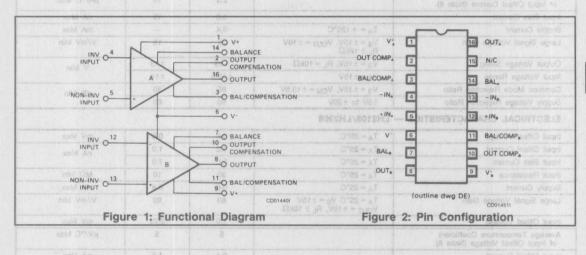
The LH2108A/LH2308A and LH2108/LH2308 series of dual operational amplifiers consist of two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, and reduced insertion cost.

- Power Diseignation (Note 1) (September 2) (S ● Low Offset Current — 50pA ( etal) = patio V hand
- Low Offset Voltage 0.7mV
- Low Offset Voltage LH2108A: 0.3mV
- LH2108: 0.7mV

   Wide Input Voltage Range ±15V
- Wide Operating Supply Range ±3V to ±20V

#### ORDERING INFORMATION

PART NUMBER	Ot	TEMPERATURE RANGE	- 7	PACKAGE	e23 e
LH2108D	8.0	-55°C to +125°C	AT		
LH2108AD	25	-55°C to +125°C V3 = aV 0°33	w AT	16-PIN	
LH2308D	Ot	0°C to +70°C	UDA	CERAMIC	
LH2308AD	700	0°C to +70°C			



## LH2108/LH2308



#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	±20V
Power Dissipation (Note 1)	
Differential Input Current (Note 2)	
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	ontinuous

Operating Temperature Range
LH2108A/LH210855°C to +125°C
LH2308A/LH2408 0°C to +70°C
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10sec)300°C

# ELECTRICAL CHARACTERISTICS (See Note 4) (LH2108/LH2308)

			LIN	MITS		
PARAMETER		TEST CONDITIONS LH21		LH2308	UNIT	
Input Offset Voltage T <sub>A</sub> = 25°C			2.0	7.5	mV Max	
Input Offset Current		T <sub>A</sub> = 25°C	0.2	1.0	nA Max	
Input Bias Current	dependent of the	T <sub>A</sub> = 25°C	2.0	7.0	THE STATE OF THE S	
Input Resistance (Note 5)	MAKEN	T <sub>A</sub> = 25°C	30	10	MΩ Min	
Supply Current		T <sub>A</sub> = 25°C	0.6-	0.8	mA Max 0013M	
Large Signal Voltage Gain	16-218	$T_A = 25$ °C $V_S = \pm 15V$ $V_{OUT} = \pm 10V$ , $R_L \ge 10kΩ$	07 0 50	25	V/mV Min	
Input Offset Voltage	MARISO	Office Control	3.0	10	mV Max	
Average Temperature Coefficient of Input Offset Voltage (Note 6)		70°C	01 0 15	30	μV/°C Max	
Input Offset Current			0.4	1.5	nA Max	
Average Temperature Coefficient of Input Offset Current (Note 6)			2.5	10	pA/°C Max	
Input Bias Current	ACTION CONTRACTOR		3.0	10	nA Max	
Supply Current		T <sub>A</sub> = +125°C	0.4		mA Max	
Large Signal Voltage Gain		$V_S = \pm 15V$ , $V_{OUT} = \pm 10V$ $R_L \ge 10k\Omega$	W 25	15	V/mV Min	
Output Voltage Swing	5.00	$V_S = \pm 15V$ , $R_L = 10k\Omega$	±13	±13	V Min	
Input Voltage Range	751	V <sub>S</sub> = ±15V	±13.5	±14		
Common Mode Rejection Ratio	and the same	$V_S = \pm 15V, V_{CM} = \pm 13.5V$	85	80	dB Min	
Supply Voltage Rejection Ratio	part -	±5V to ±20V	80	80	TURBIT.	
ELECTRICAL CHARACTERI	STICS -	LH2108/LH2308				
Input Offset Voltage	[3]	V T <sub>A</sub> = 25°C	0.5	0.5	mV Max	
Input Offset Current	Total Control	TA = 25°C	0.2	1.0	nA Max	
Input Bias Current	lan.	T <sub>A</sub> = 25°C	2.0	7.0		
Input Resistance		T <sub>A</sub> = 25°C	30	10	MΩ Min	
Supply Current		T <sub>A</sub> = 25°C	0.6	0.8	mA Max	
Large Signal Voltage Gain	aneuar	$T_A = 25^{\circ}C \ V_S = \pm 15V$ $V_{OUT} = \pm 10V, \ R_L \ge 10k\Omega$	80	80	V/mV Min	
Input Offset Voltage	DITT CS	Amata III	1.0	0.73	mV Max	
Average Temperature Coefficient of Input Offset Voltage (Note 6)			5	5	μV/°C Max	
Input Offset Current		M. E. S.	0.4	1.5	nA Max	
Average Temperature Coefficient of Input Offset Current (Note 6)			2.5	10	pA/°C Max	
Input Bias Current			3.0	10	nA Max	
Supply Current		$T_A = +125^{\circ}C$	0.4		mA Max	
Large Signal Voltage Gain		$V_S = \pm 15V$ , $V_{OUT} = \pm 10V$ $R_L \ge 10k\Omega$	40	60	V/mV Min	
Output Voltage Swing		$V_S = \pm 15V$ , $R_L = 10k\Omega$	±13	±13	V Min	
Input Voltage Range		$V_S = \pm 15V$	±13.5	±14		

# LH2108/LH2308

# ELECTRICAL CHARACTERISTICS (CONT.)

PARAMETER	23 TEST CONDI	TEST CONDITIONS		ITS	GENER <mark>TIN</mark> DESC
XAM ANT OF XAM ANS Inchie		wol sh	LH2108	LH2308	Those differential inc
Common Mode Rejection Ratio	e Input Offset	brig. La	96 96	96	dB Min
Supply Voltage Rejection Ratio	testic inder	19VIIOU	96	96	chopper stabilized an

NOTES: 1. The maximum junction temperature of the LH2108/A is 150°C, and that of the LH2308/A is 85°C. The thermal resistance of the packages is 100°C C/W, junction to ambient.

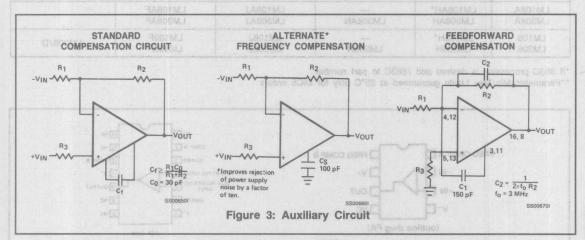
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

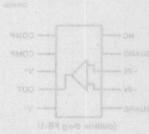
4. These specifications apply for ±5V  $\leq$  V<sub>S</sub>  $\leq$  ±20V and  $-55^{\circ}$ C  $\leq$  T<sub>A</sub>  $\leq$  125°C, unless otherwise specified, and the LH2308A/LH2308 for  $\pm$ 5V  $\leq$  V<sub>S</sub>  $\leq$  15V and 0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C.

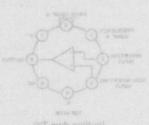
5. Input resistance is guaranteed by Input Bias Current test.

6. For Design only, not 100% tested.









#### **GENERAL DESCRIPTION**

These differential input, precision amplifiers provide low input currents and offset voltages comparable to FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of > 2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor. The LM108A and LM308A are high performance selections from the 108/308 amplifier family.

#### **FEATURES**

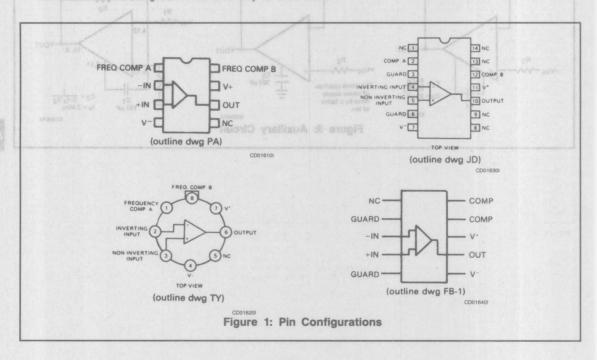
- Input Bias Current 2nA Max to 7nA Max
- Input Offset Current 0.2nA Max to 1nA Max
- Input Offset Voltage 0.5mV Max to 7.5mV Max
- ΔVos/ΔT 5μV/°C to 30μV/°C
- Δlos/ΔT 2.5pA/°C to 10pA/°C
- Pin for Pin Replacement for 101A/301A

#### ORDERING INFORMATION

PART NUMBER	TO-99 CAN	8 PIN MINIDIP	14 PIN CERDIP	10 PIN FLATPAK	** DICE
LM108A	LM108AH*	_	LM108AJ	LM108AF	
LM308A	LM308AH	LM308AN	LM308AJ	LM308AF	
LM108 LM308	LM108H* LM308H	LM308N	LM108J LM308J	LM108F LM308F	LM308/D

\*If 883C processing is desired add /883C to part number.

\*\*Parametric Min/Max Limits guaranteed at 25°C only for DICE orders.



# LM108/A, LM308/A

#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	Input Voltage (Note 3)±15V
108, 108A±20V	Output Short-Circuit DurationIndefinite
308, 308A±18V	Operating Temperature Range
Internal Power Dissipation (Note 1)	108, 108A55°C to +125°C
Metal CAn (TO-99)500mW	308, 308A0°C to +70°C
DIP500mW	Storage Temperature Range65°C to +150°C
Differential Input Current (Note 2) ±10mA	Lead Temperature (Soldering, 10sec)300°C

#### ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise specified) (Note 4)

4801		S 308 308A 108 108A												
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Input Offset Voltage			2.0	7.5	-36.5075	0.3	0.5	Miles I	0.7	2.0	TI	0.3	0.5	mV
Input Offset Current	Cartendon delicated to the	Total	0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current	M1 1001 2		1.5	7		1.5	7		0.8	2.0	27 54	0.8	2.0	nA
Input Resistance	Note 5	10	40		10	40		30	70	342 7	30	70		МΩ
Supply Current	V <sub>S</sub> = ±20V V <sub>S</sub> = ±15V		0.3	0.8		0.3	0.8		0.3	0.6		0.3	0.6	mA mA
Large Signal Voltage Gain	$V_S = \pm 15V$ , $V_{OUT} = \pm 10V$ $R_L > 10k\Omega$	25	300	OV B	80	300		50	300	tusu	80	300	Swot	V/m\
THE FOLLOWING SPE	CIFICATIONS APPLY OVE	R THE	OPER/	ATING	TEMPE	RATUR	E RAN	GES						
Input Offset Voltage				10			0.73			3.0	By174	2311	1.0	mV
Input Offset Current		1231	177	1.5		DE L	1.5		N BARIE	0.4	ecs-II		0.4	nA
Average Temperature Coefficient of Input Offset Voltage	Note 6		6.0	30		1.0	5.0	-	3.0	15	Z	1.0	5.0	μ\/°(
Average Temperature Coefficient of Input Offset Current	Note 6		2	10		2.0	10		0.5	2.5	Á	0.5	2.5	pA/°
Input Bias Current			Property land	10	TEST	1777	10		-	3.0		3781 ×	3.0	nA
Large Signal Voltage Gain	$V_S = \pm 15V$ , $V_{OUT} = \pm 10V$ $R_L \ge 10k\Omega$	15			60			25			40	1 4	A 1	V/m\
Input Voltage Range	V <sub>S</sub> = ±15V	±13.5	397	317	±13.5	(0)		±13.5	31 5/	#03	±13.5	-31	001	٧
Common Mode Rejection Ratio	$V_5 = \pm 15V$ $V_{CM} = \pm 13.5V$	80	100	A DW 31	96	110		85	100	Isut V	96	110		dB
Supply Voltage Rejection Ratio	±5V to ±20V	80	96		96	110		80	96		96	110		dB
Output Voltage Swing	$V_S = \pm 15V$ , $R_L = 10k\Omega$	±13	±14	Maria C	±13	±14	- E800	±13	±14	3590	±13	±14		٧
Supply Current	$T_A = +125$ °C, $V_S = \pm 20$ V						1		0.15	0.4	T. T.	0.15	0.4	mA

NOTES: 1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9mW/

°C for operation at ambient temperatures above 95°C.

voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

3. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

4. Unless otherwise specified, these specifications apply for supply voltages from +5V to ±20V for the 108, and 108A and +5V to ±15V for the 308 and 308A.

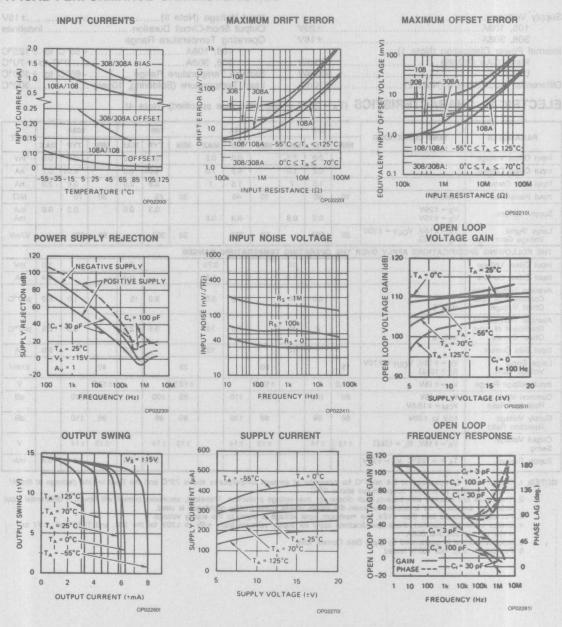
5. Input resistance is guaranteed by Input Bias Current test. 6. For Design only, not 100% tested.

<sup>2.</sup> The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input

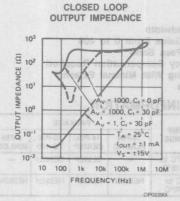
# LM108/A, LM308/A

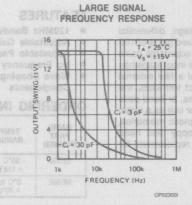
# & INTERSIL

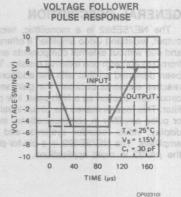
#### TYPICAL PERFORMANCE CHARACTERISTICS BUNITAR MUMIXAM STUJOSEA



## TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)







#### GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration).

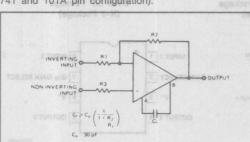


Figure 2: Frequency Compensation Circuit

STANDARD CIRCUIT

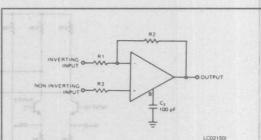


Figure 3: Frequency Compensation Circuit

ALTERNATE CIRCUIT IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN 4

# NE/SE592 Video Amplifier



#### GENERAL DESCRIPTION

The NE/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 0 to 400 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The NE/SE592 is a pin-for-pin replacement for the µA733 in most applications.

#### **FEATURES**

- 120MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required
- Wave Shaping With Minimal External Components

#### ORDERING INFORMATION

12	BASIC	75110	PACKAGE							
	PART NUMBER	TEMP	14-PIN PLASTIC	14-PIN CERDIP	10-PIN TO-100	8-PIN MINI DIP				
	SE592	-55°C to +125°C	841 HOOT	SE592F	SE592H	-				
	NE592	0°C to +70°C	NE592N	NE592F	NE592H	NE592N-8				

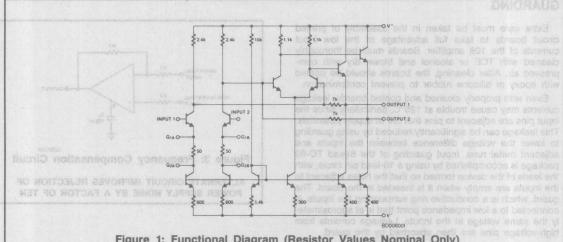
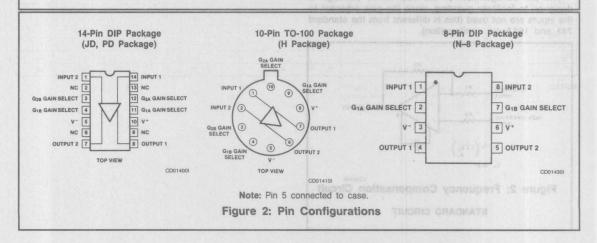


Figure 1: Functional Diagram (Resistor Values Nominal Only)



Super ' Chago	±8V	Operating Temperature Range	A CORPORATION OF THE PARTY OF T
Differential Input Voltage	±5V	SE592	55°C to +125°C
Common-Mode Input Voltage	±6V	NE592	0°C to +70°C
Output Current	10mA	Storage Temperature Range	65°C to +150°C
, 94031 34864 A	2411	Power Dissipation	500mW
1 1 1 POI x 2.1		Lead Temperature (Soldering, 1	0sec)300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

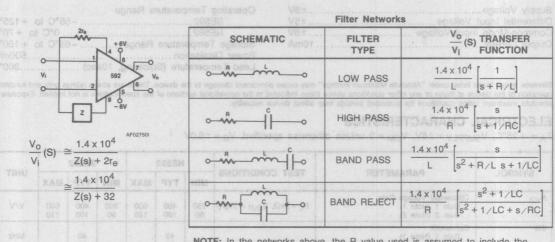
#### ELECTRICAL CHARACTERISTICS

 $T_A = +25$ °C,  $V_{SUPPLY} = \pm 6V$ ,  $V_{CM} = 0$  unless otherwise specified.  $V_S = \pm 6.0V$ 

ONL SELLO	PARAMETER		0	NE592		- 219	SE592	101	UNIT
SYMBOL		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
AVOL.	Differential Voltage Gain Gain 1 (Note 1) Gain 2 (Note 2)	$R_L = 2k\Omega$ , $V_{OUT} = 3Vp-p$	250 80	400 100	600 120	300 90	400 100	500 110	V/V
We include the	Gaill 2 (Note 2)	Et in the networks abo	TOM	40 90			40 90		MHz
t <sub>r</sub>	Gain 1 (Note 1) Gain 2 (Note 2) (Note 4)	V <sub>OUT</sub> = 1Vp-p		10.5 4.5	12		10.5 4.5	10	ns
<sup>t</sup> d	Propagation Delay Gain 1 (Note 1) Gain 2 (Note 2) (Note 4)	V <sub>OUT</sub> = 1Vp-p	971	7.5 6.0	10		7.5 6.0	10	ns
R <sub>IN</sub>	Input Resistance Gain 1 (Note 1) Gain 2 (Note 2)		10	4.0		20	4.0 30		kΩ
CIN	Input Capacitance (Note 2) (Note 4)	Gain 2		2.0			2.0		pF
los	Input Offset Current	7001	4 1 6	0.4	5.0	-	0.4	3.0	μΑ
IBIAS	Input Bias Current			9.0	30		9.0	20	μΑ
ēn	Input Noise Voltage	BW = 1kHz to 10MHz		12		10	12	100	μV rms
ΔVIN	Input Voltage Range	1 3 3	ELE		±1.0			±1.0	٧
CMRR	Common-Mode Rejection Ratio Gain 2 (Note 2) Gain 2 (Note 2)	V <sub>CM</sub> ±1V, f < 100kHz V <sub>CM</sub> ±1V, f = 5MHz	60	86 60	3	60	86 60		dB
PSRR	Supply Voltage Rejection Ratio Gain 2 (Note 2)	$\Delta V_S = \pm 0.5 V$	50	70	ALPE N	50	70		dB
V <sub>00</sub>	Output Offset Voltage Gain 2 (Note 2)	R <sub>L</sub> = ∞		0.35	0.75		0.35	0.75	٧
Vосм	Output Common-Mode Voltage	RL = 00 PRI PRIA PROYATE AND A	2.4	2.9	3.4	2.4	2.9	3.4	V
VO(DIFF)	Differential Output Voltage Swing	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
Ro	Output Resistance	belshipost egsTV	Disc	20	217		20		Ω
1+	Power Supply Current (Note 3)	R <sub>L</sub> = ∞		18	24		18	24	mA

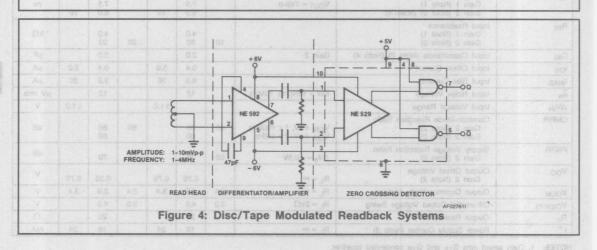
NOTES: 1. Gain select pins G<sub>1A</sub> and G<sub>1B</sub> connected together.
2. Gain select pins G<sub>2A</sub> and G<sub>2B</sub> connected together.
3. Recommended supply voltage = ±6V
4. For design reference only, not 100% tested.

#### TYPICAL APPLICATIONS



**NOTE:** In the networks above, the R value used is assumed to include the internal  $2r_{\rm e}$  of approximately  $32\Omega$ .

Figure 3: Basic Configuration



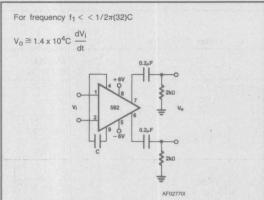


Figure 5: Differentiation with High Common Noise Rejection

The Oral servery

Figure 5: Differentiation with High Common Notes Rejection

# Section 5 — Special Analog Functions

Section 5 — Special Analog Functions

## AD590

## 2-Wire Current Output **Temperature Transducer**

# GENERAL DESCRIPTION

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1µA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2µA output at 298.2°K (+25°C).

The AD590 should be used in any temperature-sensing application between -55°C and +150°C (0°C and 70°C for TO-92) in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistancemeasuring circuitry and cold-junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.



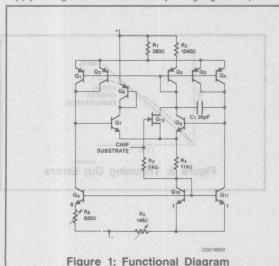
#### **FEATURES**

- Linear Current Output: 1µA/°K
- Wide Range: -55°C to +150°C
- Two-Terminal Device: Voltage In/Current Out
- Laser Trimmed to ±0.5°C Calibration Accuracy
- Excellent Linearity: ±0.5°C Over Full Range (AD590M)
- Wide Power Supply Range: +4V to +30V
- Sensor Isolation From Case
- Low Cost

#### ORDERING INFORMATION

com 0.0% ±	PART NUMBER/PACKAGE						
NON-LINEARITY	TO-52 PACKAGE	TO-92 PACKAGE	DICE**				
*** £±3.0	AD590IH	AD590IZR	AD590/D				
±1.5	AD590JH	AD590JZR	Summint Note:				
±0.8	AD590KH	Rajec <del>tio</del> ns	Power Suppl				
±0.4	AD590LH	<u>→</u> @+>	Y SWA				
±0.3	AD590MH	V31+ X	V > V84 + V				
TEMPERATURE RANGE	-55°C to +150°C	0°C to +70°C	DICE				

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



(outline dwg TO-52) SUBSTRATE (LEAVE FLOATING)

(outline dwg TO-92)

Figure 2: Pin Configurations

I VITTUIG TURAGE	( · · · · /		
Reverse Voltage	(V + to V -)		20V
Breakdown Volta	ge (Case to	V + or V -)	±200V
Storage Tempera	ature Range	65°C	to +150°C

riatou i oriormanos remperatur	e manye
TO-92	0°C to +70°C
TO-52	55°C to +150°C
Lead Temperature (Soldering,	10sec)+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **SPECIFICATIONS** (Typical values at T<sub>A</sub> = +25°C, V<sup>+</sup> = 5V unless otherwise noted)

CHARACTERISTICS	AD590I	AD590J	AD590K	AD590L	AD590M	UNIT
Output Nominal Output Current @ + 125°C(298.2°K)	298.2	298.2	298.2	298.2	298.2	μΑ
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μΑ/° Κ
Calibration Error @ + 25°C (Notes 1, 5)	±10.0 max	±5.0 max	±2.5 max	±1.0 max	±0.5 max	°C
Absolute Error (-55°C to +150°C) (Note 7) Without External Calibration Adjustment With External Calibration Adjustment	±20.0 max ±5.8 max	±10.0 max ±3.0 max	±5.5 max ±2.0 max	±3.0 max ±1.6 max	±1.7 max ±1.0 max	°C
Non-Linearity (Note 6)	(±3.0 max	±1.5 max	±0.8 max	±0.4 max	±0.3 max	°C
Repeatability (Notes 2, 6)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C
Long Term Drift (Notes 3, 6)	±0.1 max	±0.1 max	±0.1 max	±0.1 max	±0.1 max	°C/month
Current Noise ALOGADA HLOGADA	2 40	40	40	40	40	pA/√Hz
Power Supply Rejection: +4V < V + < +5V +5V < V + < +15V +15V < V + < +30V	0.5 0.2 0.1	0.5 0.2 0.1	0.5 0.2 0.1	0.5 0.2 0.1	0.5 0.2 0.1	μΑ/V μΑ/V μΑ/V
Case Isolation to Either Lead	1010	1010	1010	1010	1010	A era
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	20	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	рА
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	V

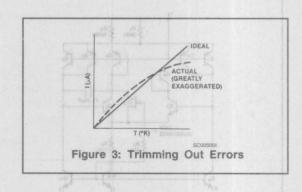
- NOTES: 1. Does not include self heating effects.
  - 2. Maximum deviation between +25°C reading after temperature cycling between -55°C and +150°C (0°C and 70°C for TO-92).
  - 3. Conditions: Constant +5V, constant +125°C.
  - 4. Leakage current doubles every + 10°C.
  - 5. Mechanical strain on package (especially TO-92) may disturb calibration of device.
  - 6. Guaranteed. But not tested.
  - 7. -55°C Guaranteed by testing @ +25°C and @ +150°C.

#### TRIMMING OUT ERRORS

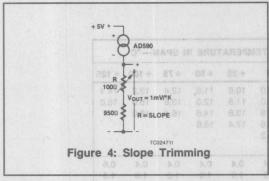
The ideal graph of current versus temperature for the AD590 is a straight line, but as Figure 3 shows, the actual shape is slightly different. Since the sensor is limited to the range of -55°C to +150°C (0°C to 70°C for TO-92), it is possible to optimize the accuracy by trimming. Trimming also permits extracting maximum performance from the lower-cost sensors.

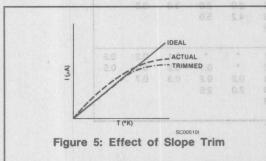
The circuit of Figure 4 trims the slope of the AD590 output. The effect of this is shown in Figure 5.

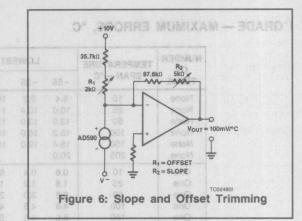
The circuit of Figure 6 trims both the slope and the offset. This is shown in Figure 7. The diagrams are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over the whole range, or over any selected part of the range. In fact, it is possible to adjust the I-grade device to give less than 0.1°C error over the range 0°C to 90°C and less than 0.05°C error from 25°C to 60°C.



5-2



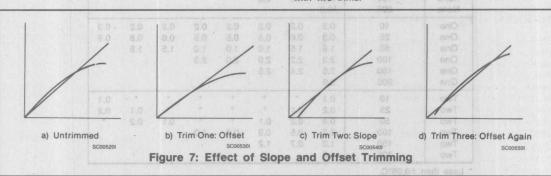




#### ACCURACY

Maximum errors over limited temperature spans, with  $V_S = +5V$ , are listed by device grade in the following tables. The tables reflect the worst-case linearities, which invariably occur at the extremities of the specified temperature range. The trimming conditions for the data in the tables are shown in Figures 4 and 5.

All errors listed in the tables are  $\pm$ °C. For example, if  $\pm$ 1°C maximum error is required over the +25°C to +75°C range (i.e., lowest temperature of +25°C and span of 50°C), then the trimming of a J-grade device, using the single-trim circuit (Figure 4), will result in output having the required accuracy over the stated range. An M-grade device with no trims will have less than  $\pm$ 0.9°C error, and an l-grade device with two trims (Figure 5) will have less than  $\pm$ 0.2°C error. If the requirement is for less than  $\pm$ 1.4°C maximum error, from -25°C to +75°C (100° span from -25°C), it can be satisfied by an M-grade device with no trims, a K-grade device with one trim, or an l-grade device with two trims.



AD590

primmirT

a following tables.



### I GRADE - MAXIMUM ERRORS, °C

NUMBER		LOWE	ST TE	MPERA	TURE I	N SPA	N-°C		
OF TRIMS	SPAN-°C	-55	-25	0	+ 25	+50	+75	+ 100	+ 125
None	10	8.4	9.2	10.0	10.8	11.6	12.4	13.2	14.4
None	25	10.0	10.4	11.0	11.8	12.0	13.8	15.0	16.0
None	50	13.0	13.0	12.8	13.8	14.6	16.4	18.0	
None	100	15.2	16.0	16.6	17.4	18.8			
None	150	18.4	19.0	19.2					
None	205	20.0							
One	10	0.6	0.4	0.4	0.4	0.4	0.4	0.4	0.6
One	25	1.8	1.2	1.0	1.0	1.0	1.2	1.6	1.8
One	50	3.8	3.0	2.0	2.0	2.0	3.0	3.8	description
One	100	4.8	4.5	4.2	4.2	5.0			
One	150	5.5	4.8	5.5					
One	205	5.8							
Two	10	0.3	0.2	0.1	*	*	0.1	0.2	0.3
Two	25	0.5	0.3	0.2	*	0.1	0.2	0.3	0.5
Two	50	1.2	0.6	0.4	0.2	0.2	0.3	0.7	Sec.
Two	100	1.8	1.4	1.0	2.0	2.5			16
Two	150	2.6	2.0	2.8					
Two	205	3.0							

Less than 0.05°C.

#### J GRADE - MAXIMUM ERRORS, °C

NUMBER TEMPERATURE		LOWEST TEMPERATURE IN SPAN-°C							
TRIMS	SPAN-°C	-55	-25	0	+ 25	+50	+75	+ 100	+ 125
None	newperiody if no	4.2	4.6	5.0	5.4	5.8	6.2	6.6	7.2
None	0°38- 25 10m	5.0	5.2	5.5	5.9	6.0	6.9	7.5	8.0
None	d belialiso ad had	6.5	6.5	6.4	6.9	7.3	8.2	9.0	
None	dive e100 b ebar	7.7	8.0	8.3	8.7	9.4			
None	150	9.2	9.5	9.6					
None	205	10.0				the second	-	LEVEL CONTRACTOR	
One	10	0.3	0.2	0.2	0.2	0.2	0.2	0.2	0.3
One	25	0.9	0.6	0.5	0.5	0.5	0.6	0.8	0.9
One	50	1.9	1.5	1.0	1.0	1.0	1.5	1.9	
One	100	2.3	2.2	2.0	2.0	2.3			
One	150	2.5	2.4	2.5					
One	205	3.0							
Two	10	0.1		*	*		*	*	0.1
Two	25	0.2	0.1	*		*	*	0.1	0.2
Two	50	0.4	0.2	0.1	*	*	0.1	0.2	*
Two	100	0.7	0.5	0.3	0.7	1.0			
Two	150	1.0	0.7	1.2					
Two	205	1.6	hime a						

<sup>\*</sup> Less than ±0.05°C.

#### K GRADE - MAXIMUM ERRORS, °C

NUMBER	TEMPERATURE	Payer	LOWE	ST TE	MPERA	TURE	IN SPA	N—°C	FID
OF	SPAN-°C	-55	-25	0	+ 25	+50	+75	+ 100	+ 125
None	9.010 9.0	2.1	2.3	2.5	2.7	2.9	3.1	3.3	3.6
None	25 8.0	2.6	2.7	2.8	3.0	3.2	0.3.5	3.8	4.2
None	50 8.0	3.8	3.5	3.4	3.6	3.8	4.3	5.1	
None	100	4.2	4.3	4.4	4.6	5.1			
None	150	4.8	4.8	5.3					
None	205	5.5							
One	10	0.2	0.1	0.1	0.1	0.1	0.1	0.1	0.2
One	25	0.6	0.4	0.3	0.3	0.3	0.4	0.5	0.6
One	50	1.2	1.0	0.7	0.7	0.7	1.0	1.2	
One	100	1.5	1.4	1.3	1.3	1.5			
One	150	1.7	1.5	1.7					-
One	205	2.0							
Two	enointoxe xloors	0.1	0(8/*	*		*	*	*	0.1
Two	25 URBONT	0.2	0.1	*	*	*	*	0.1	0.2
Two	50	0.3	0.1	*	une name	*	0.1	0.2	
Two	100	0.5	0.3	0.2	0.3	0.7			
Two	150	0.6	0.5	0.7					
Two	205	0.8							

<sup>\*</sup> Less than ±0.05°C.

#### L GRADE - MAXIMUM ERRORS, °C

NUMBER	TEMPERATURE		LOWE	EST TEMPERATURE IN SPAN-°C
TRIMS	OF SPAN-°C	-55	-25	0 +25 +50 +75 +100 +125
None None None None None	10 25 50 100 150 205	1.0 1.3 1.9 2.4 2.7 3.0	1.0 1.3 1.8 2.4 2.6	1.1 1.1 1.2 1.3 1.4 1.6 1.3 1.4 1.5 1.6 1.7 1.9 1.7 1.8 1.9 2.1 2.4 1.2 2.4 2.4 2.7
One One One One One One	10 25 50 100 150 205	0.2 0.5 1.0 1.3 1.4 1.6	0.1 0.4 0.8 1.2 1.3	0.1 0.1 0.1 0.1 0.1 0.2 0.3 0.3 0.3 0.3 0.4 0.5 0.6 0.6 0.6 0.8 1.0 1.1 1.1 1.3 1.4
Two Two Two Two Two Two	10 25 50 100 150 205	0.1 0.1 0.2 0.3 0.3 0.4	* * 0.2 0.2	***

<sup>\*</sup> Less than ±0.05°C.

#### M GRADE - MAXIMUM ERRORS, °C

NUMBER OF	TEMPERATURE		LOWEST TEMPERATURE IN SPAN-°C					
TRIMS SPAN-°C	-55	-25	0 +25 +50 +75 +100 +125					
None	10	0.6	0.5	0.6 0.6 0.7 0.7 0.7 0.9				
None	25	0.8	0.8	0.7 0.7 0.8 0.8 1.0 1.1				
None	50	1.0	0.9	0.8 0.9 0.9 1.1 1.2				
None	100	1.3	1.4	1.3 01 (1.4 m.1.5 mm begings and mil				
None	150	1.5	1.6	1,6 led serulategmet to nottarego suos				
None	205	1.7						

reference sunsor

NUMBER	TEMPERATURE	LOWEST TEMPERATURE IN SPAN-°C						
OF TRIMS	SPAN-°C	-55	-25	0	+ 25	+50 +75	+100 +125	
One One One One One One	10 25 50 100 150 205	0.2 0.4 0.5 0.8 0.9 1.0	0.1 0.3 0.4 0.8 0.9	0.1 0.2 0.3 0.7 0.9	0.1 0.2 0.3 0.7	0.1 0.1 0.2 0.2 0.3 0.4 0.8	0.1 0.2 0.3 0.4 0.5	
Two Two Two Two Two	10 25 50 100 150 205	0.1 0.1 0.2 0.2 0.3 0.3	* * 0.1 0.2	* * * * 0.3	0.1	* 300 * * 0.2	* 0.1 * 0.1 0.2	

\* Less than ±0.05°C.

#### NOTES

- 1. Maximum errors over all ranges are guaranteed based on the known behavior characteristic of the
- 2. For one-trim accuracy specifications, the 205°C span is assumed to be trimmed at +25°C; for all other spans, it is assumed that the device is trimmed at the midpoint.
- For the 205°C span, it is assumed that the two-trim temperatures are in the vicinity of 0°C and +140°C; for all other spans, the specified trims are at the endpoints.
- In precision applications, the actual errors encountered are usually dependent upon sources of error which are often overlooked in error budgets. These typically include:
  - a. Trim error in the calibration technique used
  - b. Repeatability error
  - c. Long-term drift errors

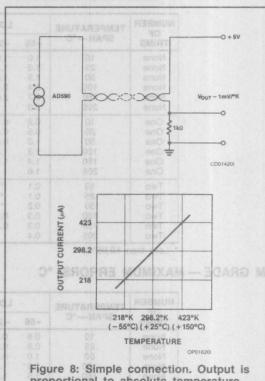
Trim error is usually the largest error source. This error arises from such causes as poor thermal coupling between the device to be calibrated and the reference sensor: reference sensor errors: lack of adequate time for the device being calibrated to settle to the final temperature; radically different thermal resistances between the case and the surroundings (RACA) when trimming and when applying the device.

Repeatability errors arise from a strain hysteresis of the package. The magnitude of this error is solely a function of the magnitude of the temperature span over which the device is used. For example, thermal shocks between 0°C and 100°C involve extremely low hysteresis and result in repeatability errors of less than ±0.05°C. When the thermalshock excursion is widened to -55°C to +150°C, the device will typically exhibit a repeatability error of ±0.05°C (±0.10 guaranteed maximum).

Long-term drift errors are related to the average operating temperature and the magnitude of the thermal shocks experienced by the device. Extended use of the AD590 at temperatures above 100°C typically results in long-term drift of ±0.03°C per month; the guaranteed maximum is ±0.10°C per month. Continuous operation at temperatures below 100°C induces no measurable drifts in the device. Besides the effects of operating temperature, the severity of thermal shocks incurred will also affect absolute stability. For

thermal-shock excursions less than 100°C, the drift is difficult to measure ( < 0.03°C). However, for 200°C excursions, the device may drift by as much as ±0.10°C after twenty such shocks. If severe, quick shocks are necessary in the application of the device, realistic simulated life tests are recommended for a thorough evaluation of the error introduced by such shocks.

#### TYPICAL APPLICATIONS



proportional to absolute temperature.

#### TYPICAL APPLICATIONS (CONT.)

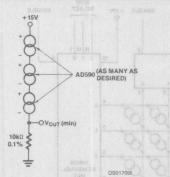


Figure 9: Lowest-temperature sensing scheme. Available current is that of the "coldest" sensor.

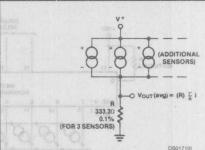


Figure 10: Average-temperature sensing scheme. The sum of the AD590 currents appears across R, which is chosen by the formula:

$$R = \frac{10k\Omega}{n}$$

n being the number of sensors.

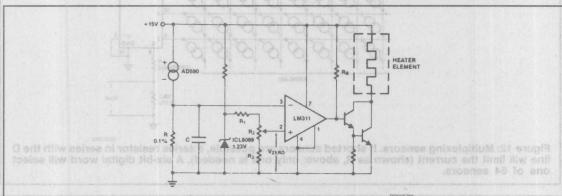


Figure 11: Single-setpoint temperature controller. The AD590 produces a temperature-dependent voltage across R (C is for filtering noise). Setting R<sub>2</sub> produces a scale-zero voltage. For the Celsius scale, make R =  $1k\Omega$  and  $V_{ZERO} = 0.273$  volts. For Fahrenheit, R =  $1.8k\Omega$  and  $V_{ZERO} = 0.460$  volts.

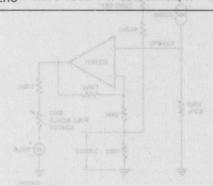


Figure 13: Centigrate thermometer (0°C-100°C), the utira-low bias current of the ICL2611 allows be use of large-value gain-resistors, keeping meter-current error under 1/2%, and therefore saving be exceeded to a saving meter-deleter amolting.

AD590

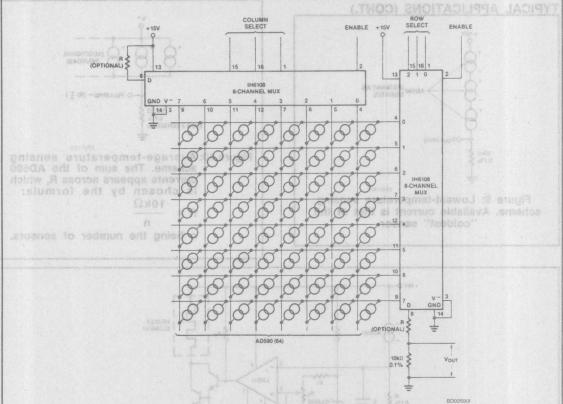


Figure 12: Multiplexing sensors. If shorted sensors are possible, a series resistor in series with the D line will limit the current (shown as R, above: only one is needed). A six-bit digital word will select one of 64 sensors.

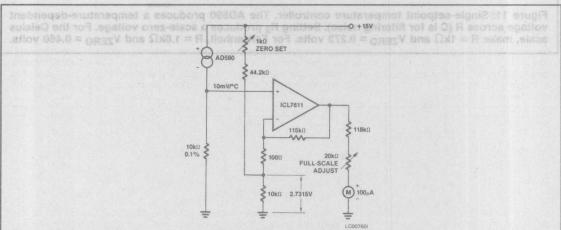


Figure 13: Centigrade thermometer (0°C-100°C) . the ultra-low bias current of the ICL7611 allows the use of large-value gain-resistors, keeping meter-current error under 1/2%, and therefore saving the expense of an extra meter-driving amplifier.

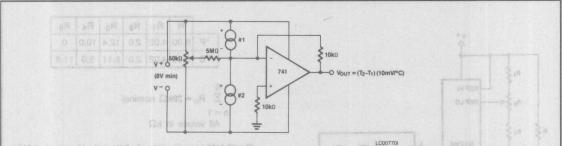


Figure 14: Differential thermometer. The  $50k\Omega$  pot trims offsets in the devices whether internal or external, so it can be used to set the size of the difference interval. This also makes it useful for liquid-level detection (where there will be a measurable temperature difference).

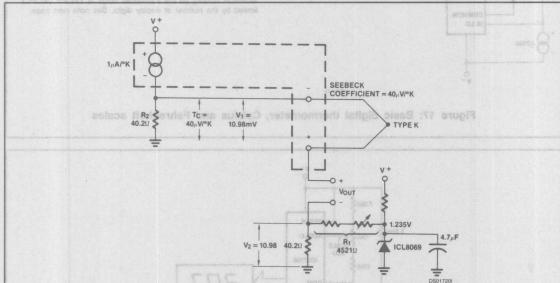


Figure 15: Cold-junction compensation for type K thermocouple. The reference junction(s) should be in close thermal contact with the AD590 case. V  $^{+}$  must be at least 4V, while ICL8069 current should be set at 1mA – 2mA. Calibration does not require shorting or removal of the thermocouple: set R<sub>1</sub> for V<sub>2</sub> = 10.98mV. If very precise measurements are needed, adjust R<sub>2</sub> to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V<sub>1</sub>, and set R<sub>1</sub> to buck out this voltage (i.e., set V<sub>2</sub> = V<sub>1</sub>). For other thermocouple types, adjust values to the appropriate Seebeck coefficient.

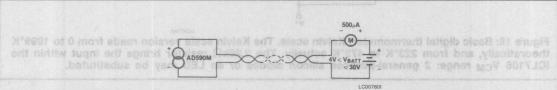
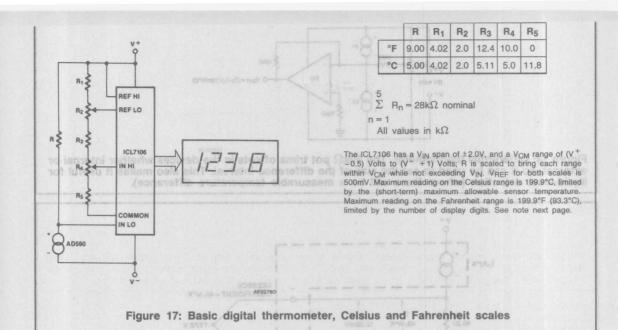


Figure 16: Simplest thermometer. Meter displays current output directly in degrees Kelvin. Using the AD590M, sensor output is within  $\pm$ 1.7 degrees over the entire range, and less than  $\pm$ 1 degree over the greater part of it.



2.28km Skn Scale Ref Hi
Ref Lo
Scale 15km Scale Icl7108
COM IN HI
Internal Books of the Scale Icl7108

Figure 18: Basic digital thermometer, Kelvin scale. The Kelvin scale version reads from 0 to 1999°K theoretically, and from 223°K to 473°K actually. The  $2.26 \mathrm{k}\Omega$  resistor brings the input within the ICL7106 V<sub>CM</sub> range: 2 general-purpose silicon diodes or an LED may be substituted.

I C007901

Figure 18: Simplest thermometer. Meter displays current output directly in degrees Kelvin. Using the AD596M, sensor output is within ±1.7 degrees over the entire range, and less than ±1 degree over the entire range, and less than ±1 degree over the entire range.

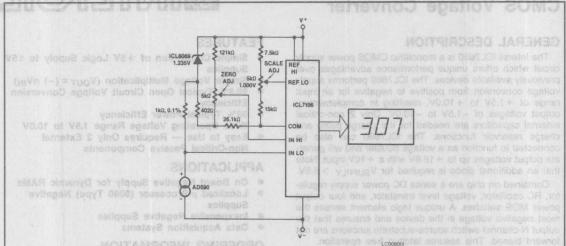


Figure 19: Basic digital thermometer, Kelvin scale with zero adjust. This circuit allows "zero adjustment" as well as slope adjustment. The ICL8069 brings the input within the common-mode range, while the  $5k\Omega$  pots trim any offset at 218°K (-55°C), and set the scale factor.

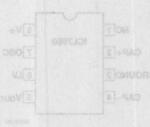
Note on Figure 17, Figure 18 and Figure 19: Since all 3 scales have narrow  $V_{\rm IN}$  spans, some optimization of ICL7106 components can be made to lower noise and preserve CMR. The table below shows the suggested values. Similar scaling can be used with the ICL7126/36.

SCALE	VIN RANGE (V)	$R_{INT}(k\Omega)$	C <sub>AZ</sub> (µF)
K	0.223 to 0.473	220	0.47
C	-0.25 to +1.0	220	0.1
F	-0.29 to +0.996	220	0.1

For all:

$$C_{REF} = 0.1 \mu F$$
  
 $C_{INT} = 0.22 \mu F$ 

$$C_{OSC} = 100 pF$$
  
 $R_{OSC} = 100 k\Omega$ 





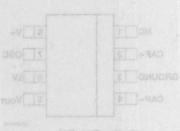


Figure 1: Pin Configurations

# ICL7660 CMOS Voltage Converter

# **WINTERSIL**

#### GENERAL DESCRIPTION

The Intersil ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of -1.5V to -10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input. Note that an additional diode is required for VSUPPLY > 6.5V.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, and four output-power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

#### **FEATURES**

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication (V<sub>OUT</sub> = (-) nV<sub>IN</sub>)
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 98% Typical Power Efficiency
- Wide Operating Voltage Range 1.5V to 10.0V
- Easy to Use Requires Only 2 External Non-Critical Passive Components

#### **APPLICATIONS**

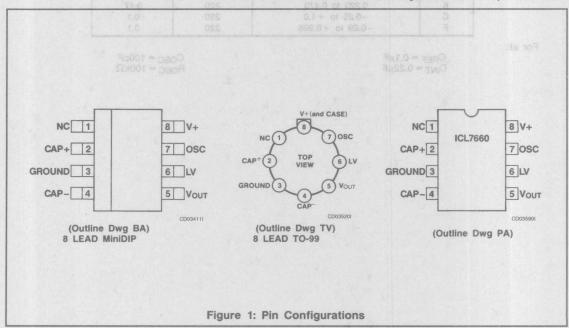
- On Board Negative Supply for Dynamic RAMs
- Localized μ-Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

#### ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE		
ICL7660CTV	0° to +70°C	TO-99		
ICL7660CBA	0°C to +70°C	8 PIN SOIC		
ICL7660CPA	0° to +70°C	8 PIN MINI DIP		
ICL7660MTV*	-55° to +125°C	TO-99		
ICL7660/D	w beau ed nac p	DICE**time2 souls		

\*Add /883B to part number if 883B processing is required.

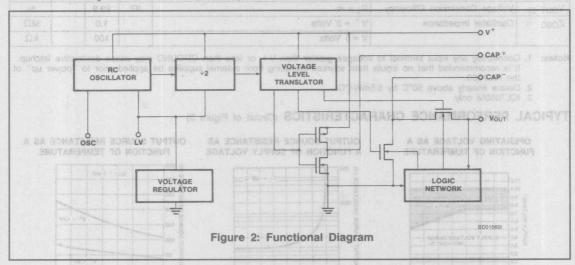
\*\*Parameter min/max limits guaranteed at 25°C only for DICE orders.



#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage  LV and OSC Input Voltage (Note 1)0.3V to (V± +0.3V)  (V+ -5.5V) to (V+ +0.3V)  Current into LV (Note 1)	for $V^+ < 5.5V$ for $V^+ > 5.5V$ Storage for $V^+ > 3.5V$ Lead T	ICL7660M ICL7660C e Temperature Range emperature	0°C to +70°C 65°C to +150°C
Output Short Duration (V <sub>SUPPLY</sub> ≤ 5.5V)  Power Dissipation (Note 2)  ICL7660CTV	500mW	0,000	
ICI 7660MTV	500mW		

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



#### **OPERATING CHARACTERISTICS**

V + = 5V, TA = 25°C, COSC = 0, Test Circuit Figure 3 (unless otherwise specified)

	PARAMETER &	DECLERATES TO MOROWAY A SOME TEST CONDITIONS		O 30 WLIMITS I A BA		
SYMBOL				TYP	MAX	UNIT
1+	Supply Current	R <sub>L</sub> = ∞	- Laure	170	500	μΑ
VH1	Supply Voltage Range - Hi	$0^{\circ}\text{C} \le T_{\text{A}} \le 70^{\circ}\text{C}, R_{\text{L}} = 10\text{k}\Omega, \text{ LV Open}$	3.0		6.5	V
	(D <sub>X</sub> out of circuit) (Note 3)	$-55^{\circ}\text{C} \le T_{A} \le 125^{\circ}\text{C}$ , $R_{L} = 10\text{k}\Omega$ , LV Open	3.0		5.0	V
V <sub>L</sub> <sup>+</sup> 1	Supply Voltage Range - Lo (D <sub>X</sub> out of circuit)	MIN $\leq$ T <sub>A</sub> $\leq$ MAX, R <sub>L</sub> = 10k $\Omega$ , LV to GROUND	1.5		3.5	٧
VH2	Supply Voltage Range - Hi (D <sub>X</sub> in circuit)	MIN $\leq$ T <sub>A</sub> $\leq$ MAX, R <sub>L</sub> = 10k $\Omega$ , LV Open	3.0		10.0	٧
V <sub>L2</sub>	Supply Voltage Range - Lo (D <sub>X</sub> in circuit)	MIN $\leq$ T <sub>A</sub> $\leq$ MAX, R <sub>L</sub> = 10k $\Omega$ , LV to GROUND	1.5	poset page	3.5	٧

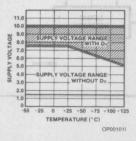
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SYMBOL	PARAMETER OUISING	TEST CONDITIONS		LIMITO		
		TEST CONDITIONS	MIN	TYP	MAX	UNIT
to +150°C	ornitire Range65°C	I <sub>OUT</sub> = 20mA, T <sub>A</sub> = 25°C	O at A	55	100	Ω
		$J_{OUT} = 20 \text{mA}, \ 0^{\circ}\text{C} \le T_{A} \le +70^{\circ}\text{C}$	(	alov)	120	Ω
		$I_{OUT} = 20 \text{mA}, -55^{\circ}\text{C} \le T_{A} \le +125^{\circ}\text{C} \text{ (Note 3)}$	Mans.	) noiler	150	0 0
ROUT	Output Source Resistance	$V^+ = 2V$ , $I_{OUT} = 3mA$ , LV to GROUND $0^{\circ}C \le T_A \le +70^{\circ}C$	(2)	VT	300	Ω
		$V^+ = 2V$ , $I_{OUT} = 3mA$ , LV to GROUND, -55°C $\leq T_A \leq +125$ °C, $D_X$ in circuit (Note 3)			400	Ω
fosc	Oscillator Frequency	lute Maximum Railings may gause permanent damage to the	ider Abso	10	RON SW	kHz
PEf	Power Efficiency	$R_L = 5k\Omega$ and allow solved totals year above the because the	95	98	a munac	%
Vout Ef	Voltage Conversion Efficiency	R <sub>L</sub> = ∞	97	99.9		%
Zosc	Oscillator Impedance	V <sup>+</sup> = 2 Volts		1.0		МΩ
	TV a	V = 5 Volts		100		kΩ

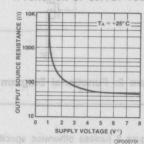
- Notes: 1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL 7660.
  - 2. Derate linearly above 50°C by 5.5mW/°C.
  - 3. ICL7660M only.

#### TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

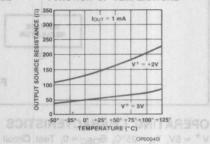
# OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



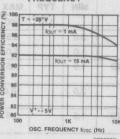
#### OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



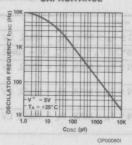
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



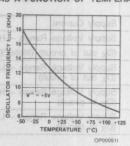
POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



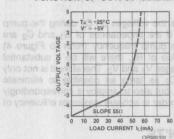
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC.



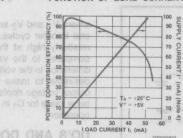
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



#### **OUTPUT VOLTAGE AS A** FUNCTION OF OUTPUT CURRENT

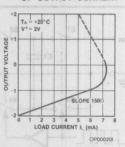


#### SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A **FUNCTION OF LOAD CURRENT**

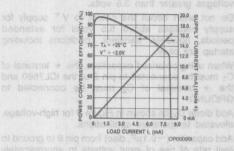


#### OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

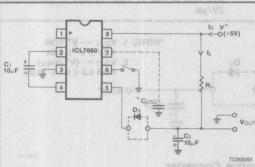
should be connected to GROUND, disabline the



#### SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



NOTE 4. These curves include in the supply current that current fed directly into the load R1 from V+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, Vout ≅ 2 VIN, IS = 2 IL, SO VIN · IS = VOUT · IL.



#### NOTES:

- 1. For large values of COSC (> 1000pF) the values of C1 and C2 should be increased to 100 µF
- 2. DX is required for supply voltages greater than 6.5V @ -55°C ≤ T<sub>A</sub> ≤ +70°C; refer to performance curves for additional information

Figure 3: ICL7660 Test Circuit

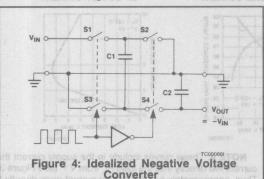
#### **DETAILED DESCRIPTION**

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10 µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C<sub>1</sub> is charged to a voltage, V<sup>+</sup>, for the half cycle when switches S1 and S3 are closed. (Note: Switches S2 and S4 are open during this half cycle.) During the second half cycle of operation, switches S2 and S4 are closed, with S<sub>1</sub> and S<sub>3</sub> open, thereby shifting capacitor C<sub>1</sub> negatively by V + volts. Charge is then transferred from C1 to C2 such that the voltage on C2 is exactly V+, assuming ideal switches and no load on C2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical

In the ICL7660, the 4 switches of Figure 4 are MOS power switches; S<sub>1</sub> is a P-channel device and S<sub>2</sub>, S<sub>3</sub> & S<sub>4</sub> are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S<sub>3</sub> & S<sub>4</sub> must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions (VOUT = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (VOLT) together with the level translators, and switches the substrates of Sa & S4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin ENERGY IS LOST ONLY IN THE TRANSFER OF should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.



#### THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

- The drive circuitry consumes minimal power.
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage conversion if large values of C1 and C2 are used.

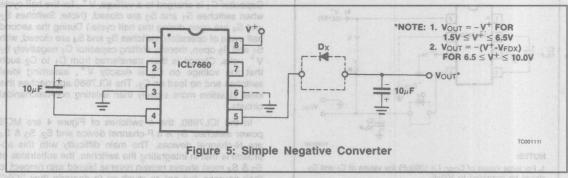
CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by:

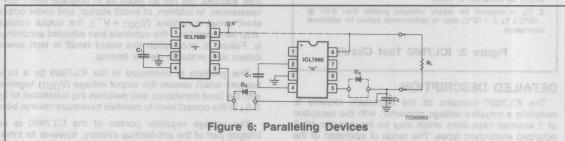
$$E = 1/2 C_1 (V_1^2 - V_2^2)$$

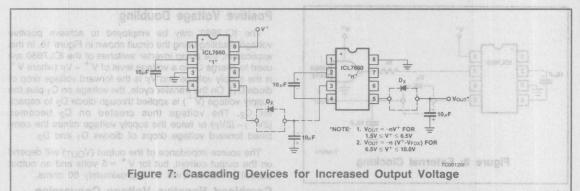
where V<sub>1</sub> and V<sub>2</sub> are the voltages on C<sub>1</sub> during the pump and transfer cycles. If the impedances of C1 and C2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of RL, there will be a substantial difference in the voltages V1 and V2. Therefore it is not only desirable to make C2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C<sub>1</sub> in order to achieve maximum efficiency of operation.

#### DO'S AND DON'TS

- 1. Do not exceed maximum supply voltages.
- 2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
- Do not short circuit the output to V+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
- When using polarized capacitors, the + terminal of C<sub>1</sub> must be connected to pin 2 of the ICL7660 and the + terminal of Co must be connected to GROUND.
- Add diode Dx as shown in Figure 3 for high-voltage, elevated temperature applications.
- Add capacitor (~0.1 µF, disc) from pin 8 to ground to limit rate of rise of input voltage to approximately 2V/μs.







#### CONSIDERATIONS FOR HIGH VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (storage & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latchup of the ICL7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latchup can be achieved by adding a general purpose diode in series with the ICL7690 output, as shown by "Dx" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

# TYPICAL APPLICATIONS

## Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +10.0 volts is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts, and that diode  $D_X$  must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 55 ohms. Thus for a load current of  $-10 \mathrm{mA}$  and a supply voltage of +5 volts, the output voltage will be -4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately  $1/\omega\mathrm{C}$ , where:

which gives 
$$\frac{1}{\omega C} = \frac{1}{2\pi} \frac{1}{\text{fpUMp} \times 10^{-5}} \approx 3 \text{ ohms}$$

for C =  $10\mu F$  and fpUMP = 5kHz (1/2 of oscillator frequency)

#### Paralleling Devices level bad well to day Jol and

Any number of ICL7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor,  $C_2$ , serves all devices while each device requires its own pump capacitor,  $C_1$ . The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

#### Cascading Devices

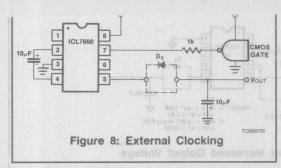
The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n (V_{IN}),$$

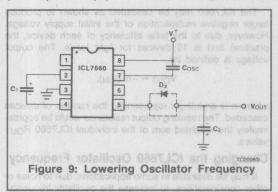
where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 ROUT values.

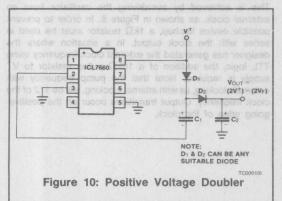
#### Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent possible device latchup, a  $1k\Omega$  resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a  $10k\Omega$  pullup resistor to Vf supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.



It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C<sub>1</sub>) and reservoir (C<sub>2</sub>) capacitors; this is overcome by increasing the values of C<sub>1</sub> and C<sub>2</sub> by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V <sup>+</sup> will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C<sub>1</sub> and C<sub>2</sub> (from 10µF to 100µF).



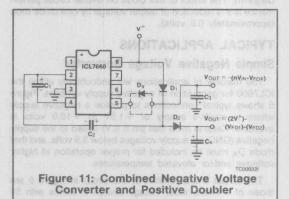


voltage doubling using the circuit shown in Figure 10. In this application, the pump inverter switches of the ICL7660 are used to charge  $C_1$  to a voltage level of  $V^+ - V_F$  (where  $V^+$  is the supply voltage and  $V_F$  is the forward voltage drop of diode  $D_1$ ). On the transfer cycle, the voltage on  $C_1$  plus the supply voltage  $(V^+)$  is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V^+) - (2V_F)$  or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 5$  volts and an output current of 10mA it will be approximately 60 ohms.

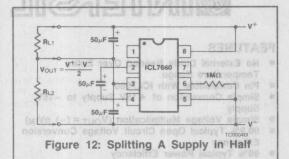
# Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C<sub>1</sub> and C<sub>3</sub> perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C<sub>2</sub> and C<sub>4</sub> are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.



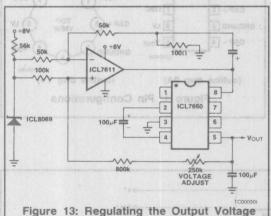
#### Voltage Splitting

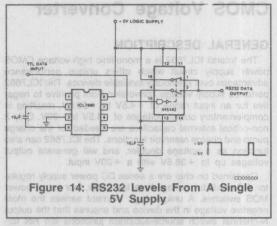
The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250 $\Omega$ ).



Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 13 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than  $5\Omega$  to a load of 10mA.





#### OTHER APPLICATIONS

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter" by Peter Bradshaw and Dave Bingham.

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# ICL7662 CMOS Voltage Converter

#### GENERAL DESCRIPTION

The Intersil ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10 to +20V), the LV pin is left floating to prevent device latchup.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7662CTV	0°C to +70°C	TO-99
ICL7662CPA	0°C to +70°C	8 PIN MINI DIP
ICL7662MTV	-55°C to +125°C	TO-99
ICL7662/D		DICE**

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

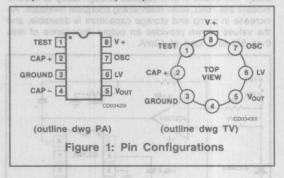


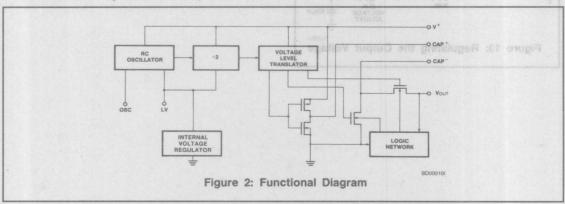
#### **FEATURES**

- No External Diode Needed Over Entire Temperature Range
- Pin Compatible With ICL7660
- Simple Conversion of +15V Supply to -15V Supply
- Simple Voltage Multiplication (Vout = (-) nVIN)
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 96% Typical Power Efficiency
- Wide Operating Voltage Range 4.5V to 20.0V
- Easy to Use Requires Only 2 External Non-Critical Passive Components

# APPLICATIONS bed and II whatestrang melding a en

- On Board Negative Supply for Dynamic RAMs
- Localized μ-Processor (8080 Type) Negative
   Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- Up to -20V for Op Amps





# ABSOLUTE MAXIMUM RATINGS SENTENSTICS (SENTENSTICS SENTENSTINGS MUMIXAM SENTENSTINGS

Supply Voltage22V	Power Dissipation (Note 2)
Oscillator Input Voltage (Note 1)	ICL7662CTY500mW
$-0.3V$ to $(V^+ + 0.3V)$ for $V^+ < 10V$	ICL7662CPA300mW
$(V^+ - 10V)$ to $(V^+ + 0.3V)$ for $V^+ > 10V$	ICL7662MTY500mW
Current into LV (Note 1)20µA for V <sup>+</sup> > 10V	Lead Temperature (Soldering, 10sec)300°C
Output Short Duration Continuous	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **ELECTRICAL CHARACTERISTICS** V<sup>+</sup> = 15V, T<sub>A</sub> = 25°C, C<sub>OSC</sub> = 0, unless otherwise stated. Test Circuit Figure 3.

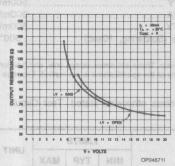
SYMBOL	PARAMETER	BERTSHRUGGERING	2 2 4 1 2 M M M M M M	LIMITS			
		TEST CON	DITIONS	MIN	TYP	MAX	UNIT
V <sup>+</sup> L V <sup>+</sup> H	Supply Voltage Range-Lo Supply Voltage Range-Hi	$R_L = 10k\Omega$ , $LV = GND$ $R_L = 10k\Omega$ , $LV = Open$	Min < T <sub>A</sub> < Max Min < T <sub>A</sub> < Max	4.5 9	PRIVACE	11 20	V
u. osc. +1	Supply Current	R <sub>L</sub> = ∞, 'LV = Open	T <sub>A</sub> = 25°C 0°C < T <sub>A</sub> < +70°C -55°C < T <sub>A</sub> < +125°C	EDUEN	.25 .30 .40	.60 .85 1.0	μΑ
Ro	Output Source Resistance	I <sub>O</sub> = 20mA, LV = Open	T <sub>A</sub> = 25°C 0°C < T <sub>A</sub> < +70°C -55°C < T <sub>A</sub> < +125°C		60 70 90	100 120 150	Ω
1+5	Supply Current	$V^+ = 5V$ , $R_L = \infty$ , $LV = GND$	T <sub>A</sub> = 25°C 0°C < T <sub>A</sub> < +70°C -55°C < T <sub>A</sub> < +125°C		20 25 30	150 200 250	μΑ
R <sub>05</sub>	Output Source Resistance	V <sup>+</sup> = 5V, I <sub>O</sub> = 3mA, LV = GND	T <sub>A</sub> = 25°C 0°C < T <sub>A</sub> < +70°C -55°C < T <sub>A</sub> < +125°C		125 150 200	200 250 350	Ω
Fosc	Oscillator Frequency	090800			10		kHz
Peff	Power Efficiency	$R_L = 2K\Omega$	T <sub>A</sub> = 25°C Min < T <sub>A</sub> < Max	93 90	96 95		%
VoEf	Voltage Conversion Effic.	R <sub>L</sub> = ∞	Min < T <sub>A</sub> < Max	97	99.9	o neu	%
losc A SA	Oscillator Sink or Source Current	$V^{+} = 5V (V_{OSC} = 0V \text{ to } +5V)$ $V^{+} = 15V (V_{OSC} = +5V \text{ to } +$		BAUFI A	0.5 4.0	ROUEN	μΑ

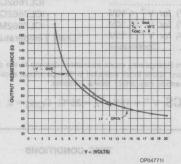
NOTES: 1. Connecting any terminal to voltages greater than V + or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7662.

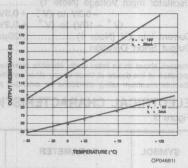
2. Derate linearly above 50°C by 5.5mW/°C.

3. Pin 1 is a Test pin and is not connected in normal use.

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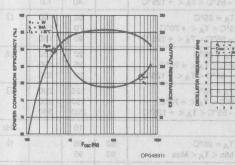


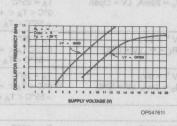


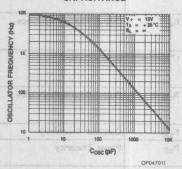
POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY OSC. FREQUENCY

POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSC. FREQUENCY

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



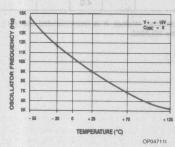


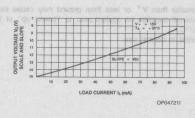


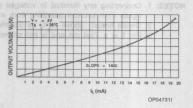
UNLOADED OSCILLATOR
FREQUENCY AS A FUNCTION OF
TEMPERATURE

OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT

OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



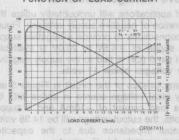


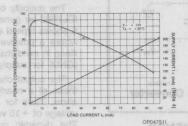


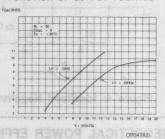
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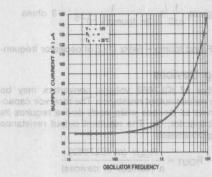
#### FREQUENCY OF OSCILLATION AS A FUNCTION OF SUPPLY VOLTAGE







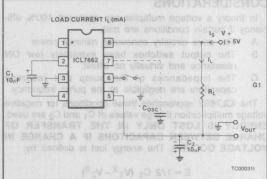
#### SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



NOTE 4.5 of misode as habspeen ad vam 5207 IOI adT Note that these curves include in the supply current that current fed directly into the load RL from V+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load.Ideally, VLOAD ~ 2VIN, IS ~ 2 IL, SO VIN . IS ~ VLOAD . IL

#### CIRCUIT DESCRIPTION

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10 µF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C<sub>1</sub> is charged to a voltage, V +, for the half cycle when switches S1 and S3 are closed. (Note: Switches S2 and S4 are open during this half cycle.) During the second half cycle of operation, switches S2 and S4 are closed, with S<sub>1</sub> and S<sub>3</sub> open, thereby shifting capacitor C<sub>1</sub> negatively by V + volts. Charge is then transferred from C1 to C2 such that the voltage on C2 is exactly V+, assuming ideal switches and no load on C2. The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.



NOTE: 1. For large value of COSC ( > 1000pf) the values of C1 and  $C_2$  should be increased to  $100\mu F$ .

Figure 3: ICL7662 Test Circuit

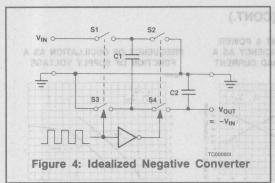
In the ICL7662, the 4 switches of Figure 4 are MOS power switches; S1 is a P-channel device and S2, S3 & S4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S<sub>3</sub> & S<sub>4</sub> must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions (VOLT = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (VOUT) together with the level translators, and switches the substrates of Sa & S4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 11 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

ICL7662





## THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

- A The drive circuitry consumes minimal power
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C1 and C2 are used. ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by:

$$E = 1/2 C_1 (V_1^2 - V_2^2)$$

where V<sub>1</sub> and V<sub>2</sub> are the voltages on C<sub>1</sub> during the pump and transfer cycles. If the impedances of C1 and C2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of RL, there will be a substantial difference in the voltages V1 and V2. Therefore it is not only desirable to make C2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C<sub>1</sub> in order to achieve maximum efficiency of operation.

# DO'S AND DON'TS

- 1. Do not exceed maximum supply voltages.
- Do not connect LV terminal to GROUND for supply 2. voltages greater than 11 volts.
- When using polarized capacitors, the + terminal of C<sub>1</sub> must be connected to pin 2 of the ICL7662 and

the + terminal of C2 must be connected to GROUND.

# TYPICAL APPLICATIONS Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 11 volts.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 65 ohms. Thus for a load current of -10mA and a supply voltage of +15 volts, the output voltage will be 14.35 volts. The dynamic output impedance due to the capacitor impedances is approximately  $1/\omega C$ , where:

which gives 
$$\frac{1}{\omega C} = \frac{1}{2\pi \text{ fpump x } 10^{-5}} = 3 \text{ ohms}$$

for C =  $10\mu$ F and fpump = 5kHz (1/2 of oscillator frequen-

# **Paralleling Devices**

Any number of ICL7662 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C2, serves all devices while each device requires its own pump capacitor, C1. The resultant output resistance would be approximately

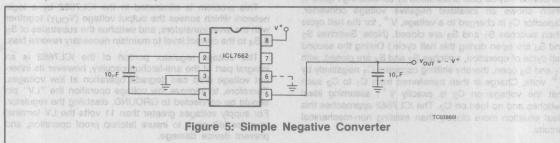
$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7662)}}{\text{n (number of devices)}}$$

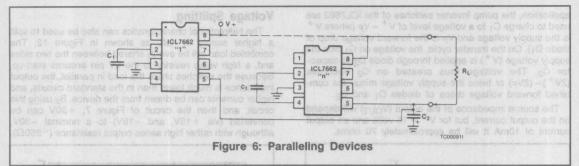
# **Cascading Devices**

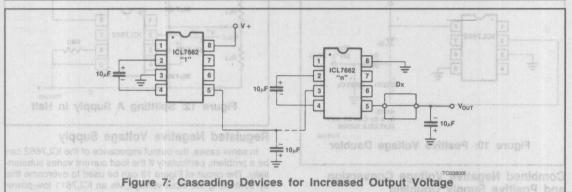
The ICL7662 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

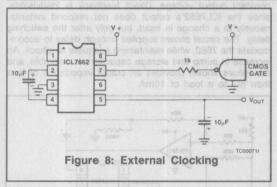
$$V_{OUT} = -n (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 ROUT values. I pasebaggo ud pootziebnu taud ed var solven e





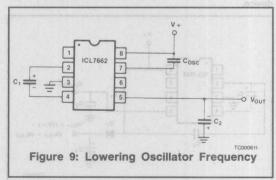




# Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent possible device latchup, a  $1k\Omega$  resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a  $10k\Omega$  pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor,  $C_{OSC}$ , as shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump  $(C_1)$  and reservoir  $(C_2)$  capacitors; this is overcome by increasing the values of  $C_1$  and  $C_2$  by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V  $^+$  will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of  $C_1$  and  $C_2$  (from  $10\mu F$  to  $100\mu F$ ).

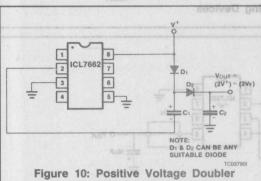


# Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 10. In this

is the supply voltage and  $V_F$  is the forward voltage drop of diode  $D_1$ ). On the transfer cycle, the voltage on  $C_1$  plus the supply voltage (V<sup>+</sup>) is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V^+) - (2V_F)$  or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 15$  volts and an output current of 10mA it will be approximately 70 ohms.



# Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C<sub>1</sub> and C<sub>3</sub> perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C<sub>2</sub> and C<sub>4</sub> are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

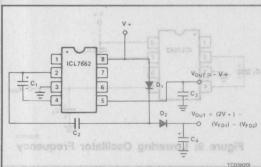
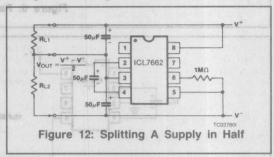


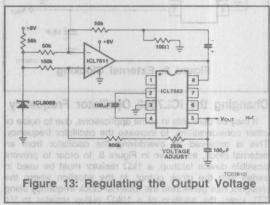
Figure 11: Combined Negative Converter and Positive Doubler

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7,  $\pm$ 30V can be converted (via  $\pm$ 15V, and  $\pm$ 15V) to a nominal  $\pm$ 30V, although with rather high series output resistance ( $\pm$ 250 $\pm$ 20).



# Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 13 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than  $5\Omega$  to a load of 10mA.



# OTHER APPLICATIONS

Further information on the operation and use of the ICL7662 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter" by Peter Bradshaw and Dave Bingham.

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#### GENERAL DESCRIPTION

The ICL7663 (positive) and ICL7664 (negative) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 10V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than  $4\mu$ A, regardless of load.

Output current sensing and remote shutdown are available on both devices, thereby providing protection for the regulators and the circuits they power. A unique feature, on the ICL7663 only, is a negative temperature coefficient output. This can be used, for example, to efficiently tailor the voltage applied to a multiplexed LCD through the driver (e.g., ICM7231/2/3/4) so as to extend the display operating temperature range many times.

The ICL7663 and ICL7664 are available in either an 8-pin plastic, TO-99 can, CERDIP, and SOIC packages.

### ORDERING INFORMATION

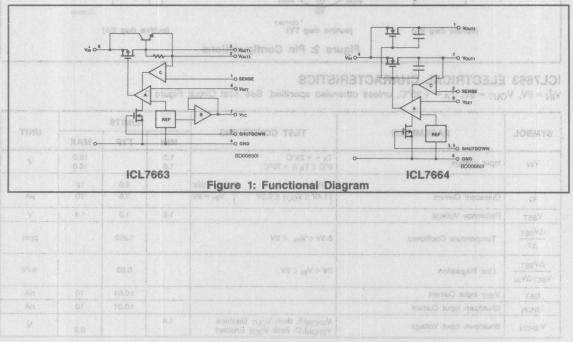
PC	SITIVE REGULAT	OR
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7663CBA ICL7663CPA ICL7663CJA ICL7663/D ICL7663CTV	0°C to +70°C 0°C to +70°C 0°C to +70°C	8-Lead SOIC 8-Lead MiniDIP 8-Lead CERDIP DICE** 8-Lead TO-99

#### FEATURES (VE.O- CMO)......(T, 6 . 6

- Ideal for Battery-Operated Systems: Less Than 4μA Typical Current Drain
- Will Handle Input Voltages From 1.6V to 16V
- Very Low Input-Output Differential Voltage
- 1.3V Bandgap Voltage Reference
- Output Shutdown Via Current-Limit Sensing or External Logic Signal
- Output Voltages Programmable From 1.3V to 16V
- Output Voltages With Programmable Negative Temperature Coefficients (ICL7663 Only)

NE SMENS) NE	GATIVE REGULAT	OR
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7664/D ICL7664CBA ICL7664CJA ICL7664CPA ICL7664CTV	0°C to +70°C 0°C to +70°C 0°C to +70°C 0°C to +70°C	DICE** 8-Lead SOIC 8-Lead CERDIP 8-Lead MiniDIP 8-Lead TO-99

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



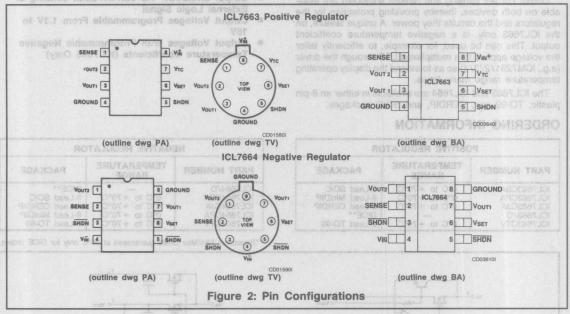
# ICL7663/7664



# ABSOLUTE MAXIMUM RATINGS, ICL7663 POSITIVE REGULATOR

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Input Supply Voltage + 18V	Output Sinking Current (Terminal 7)10mA
Any Input or Output Voltage (Note 1) (Terminals 1, 2,	Power Dissipation (Note 2)
3, 5, 6, 7)(GND -0.3V) to (ViN +0.3V)	MiniDIP200mW
Output Source Current	TO-99 Can300mW
Output Source Current (Terminal 2)	Operating Temperature Range 0°C to +70°C
(Terminal 3)	Storage Temperature

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# ICL7663 ELECTRICAL CHARACTERISTICS

 $V_{IN}^{+} = 9V$ ,  $V_{OUT} = 5V$ ,  $T_{A} = +25$ °C, unless otherwise specified. See Test Circuit Figure 3.

SYMBOL	nana martin	TEGT CONDITIONS		LIMITS			
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
VIN	Input Voltage	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$	1.5 1.6		16.0 16.0	٧	
	gram IGI,7804	( R <sub>L</sub> = ∞ ) V <sub>IN</sub> = 16V	600	4.0	12		
la	Quiescent Current	$1.4V \le V_{OUT} \le 8.5V \qquad V_{IN} = 9V$		3.5	10	μΑ	
VSET	Reference Voltage		1.2	1.3	1.4	V	
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	8.5V < V <sub>IN</sub> < 9V		±200		ppm	
ΔV <sub>SET</sub> V <sub>SET</sub> ΔV <sub>IN</sub>	Line Regulation	2V < V <sub>IN</sub> < 9V		0.03		%/V	
ISET	V <sub>SET</sub> Input Current			±0.01	10	nA	
ISHDN	Shutdown Input Current	Input Current		±0.01	10	, nA	
V <sub>SHDN</sub>	Shutdown Input Voltage	V <sub>SHDN</sub> HI: Both V <sub>OUT</sub> Disabled V <sub>SHDN</sub> LO: Both V <sub>OUT</sub> Enabled	1.4		0.3	٧	

# ICL7663 ELECTRICAL CHARACTERISTICS (CONT.) VIOLED MITAR MUMIXAM STUJOSSA

	(S etoN) notagisal			LIMITS	Voltage.	UNIT	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX		
ISENSE	Sense Pin Input Current	MistagO		0.01	10	nA nA	
°00VcL	Sense Pin Input Threshold Voltage	V <sub>CL</sub> = V <sub>OUT2</sub> - V <sub>SENSE</sub> (Current-Limit Threshold)		0.7	L COUNT	٧	
RSAT	Input-Output On-Resistance (Note 3)	V <sub>IN</sub> = 2V	Noneo tertie	70	0.18 lugivou	opened Ω of the	
$\frac{\Delta V_{\text{OUT}}}{\Delta I_{\text{OUT}}}$	Load Regulation & energia munico see T	$\Delta I_{OUT1} = 100 \mu A$ @ $V_{OUT1} = 5V$ $\Delta I_{OUT2} = 10 mA$ @ $V_{OUT2} = 5V$	ARARA + 25°C, u		ELECTI	101 7664 Viv = -8V,	
100Т2	Available Output Current (VOUT2)	V <sub>IN</sub> = 3V V <sub>OUT</sub> = V <sub>SET</sub> V <sub>IN</sub> = 9V V <sub>OUT</sub> = 5V V <sub>IN</sub> = 15V V <sub>OUT</sub> = 5V	10 25 40	TEMARAS		JomA ya	
V <sub>TC</sub>		Open-Circuit Voltage		0.9	January Comment	٧	
ITC	Negative-Tempco Output (Note 4)	Maximum Sink Current	0	8	2.0	mA	
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient of V <sub>TC</sub> Output	Open Circuit		+ 2.5	Dulescent	mV/°C	
I <sub>L</sub> (min)	Minimum Load Current	(Includes V <sub>SET</sub> Divider)	1.0	ega#joV	Peterence	μΑ	

NOTES: 1. Connecting any terminal to voltages greater then (V<sub>IN</sub> + 0.3V) or less than (GND-0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663B power-up.

2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

3. This parameter refers to the on-resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V<sub>SET</sub>, a negative coefficient results in the output voltage. See Figure 4 for details. Pin will not source current.

# ICL7663/7664



# ABSOLUTE MAXIMUM RATINGS, ICL7664 NEGATIVE REGULATOR JACKSTOLIS SASTION

Input Supply Voltage	Power Dissipation (Note 2)
Any Input or Output Voltage (Note 1) Terminals 1, 2, 3,	MiniDIP
4, 5, 6, 7)(GND +0.3V) to (V <sub>IN</sub> -0.3V)	TO-99300mW
Output Sink Current	Operating Temperature Range 0°C to +70°C
(Terminals 1, 7)	Storage Temperature Range65°C to +150°C
A SEMPLE AND A SEM	Lead Temperature (Soldering, 10sec)300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# ICL7664 ELECTRICAL CHARACTERISTICS

VIN = -9V, VOUT = -5V, TA = +25°C, unless otherwise specified. See Test Circuit Figure 3.

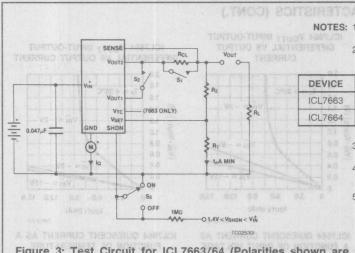
	07	TERV = TUOV VC = MV	en volVS. Im-	LIMITS		UNIT
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	TYP MAX	
VIN	Input Voltage	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$	-1.5 -1.6	tuO opgma	-16.0 -16.0	V
o la	Quiescent Current	$\left\{ \begin{array}{l} \text{R}_{L} = \infty \\ -1.4 \text{V} \leq \text{V}_{OUT} \leq -8.5 \text{V} \end{array} \right\} \qquad \begin{array}{l} \text{V}_{IN} = 16 \text{V} \\ \text{V}_{IN} = 9 \text{V} \end{array}$	orV to It	4.0	12 10	ΔΨ. Αμ
VSET	Reference Voltage	(disolutes Vage Divider)	-1.2	-1.3	-1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	-8.5V < V <sub>IN</sub> < -9V	to voltage	±200	is gáltaenn emmous e	ppm
$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	Line Regulation	-2V < VIN < -9V	ting on-	0.03	perametrical designation of the control of the cont	%/V
ISET	VSET Input Current	store coefficient. Veing it in combination wi		±0.01	10	nA
ISHDN	Shutdown Input Current	THE POLICE THE PROPERTY OF THE PROPERTY AND THE WIND	DC 0/11 (5)	±0.01	10	nA
VSHDN	Shutdown Input Voltage	V <sub>SHDN</sub> HI: Both V <sub>OUT</sub> Disabled V <sub>SHDN</sub> LO: Both V <sub>OUT</sub> Enabled	-0.3		-1.6	٧
SENSE	Sense Pin Input Current			0.01	10	nA
VCL	Sense Pin Input Threshold Voltage	V <sub>CL</sub> = V <sub>OUT2</sub> - V <sub>SENSE</sub> (Current-Limit Threshold)		-0.35		٧
RSAT	Input-Output On-Resistance (Note 3)	V <sub>IN</sub> = 2V V <sub>IN</sub> = 9V V <sub>IN</sub> = 15V		150 40 30		Ω
ΔV <sub>OUT</sub>		AL 400 A 6 V		0.0		0
Δlout	Load Regulation	$\Delta l_{OUT1} = 100 \mu A$ @ $V_{OUT} = -5V$		2.0		Ω
Гоит	Output Current VOUT1 or VOUT2	V <sub>IN</sub> = 3V V <sub>OUT</sub> = V <sub>SET</sub> V <sub>IN</sub> = 9V V <sub>OUT</sub> = -5V V <sub>IN</sub> = 15V V <sub>OUT</sub> = -5V		-2 -20 -40		mA
I <sub>L</sub> (min)	Minimum Load Current (Includes V <sub>SET</sub> Divider)		1.0			μА

NOTES: 1. Connecting any terminal to voltages greater then (GND +0.3V) or less then  $(V_{1N}^{-}-0.3V)$  may cause destructive device latchup.

It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664 power-up.

2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

3. This parameter refers to the on-resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.



- NOTES: 1. S<sub>1</sub> when closed, disables output current
  - For ICL7664, exchange Vout1 and VOUT2. S2 action differs, as follows:

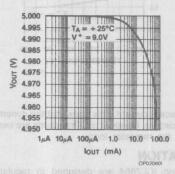
	DEVICE	S2 CLOSED	S <sub>2</sub> OPEN
I	ICL7663	V <sub>OUT1</sub>	VOUT2
1	ICL7664	Vout1 + Vout2	VouT1

- R<sub>2</sub> + R<sub>1</sub> V<sub>SET</sub> R<sub>1</sub>
- IQ quiescent current is measured at GND pin by meter M.
- S<sub>3</sub> when ON, permits normal operation, 5. when OFF, shuts down both VouT1 and VOUT2-

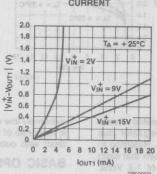
Figure 3: Test Circuit for ICL7663/64 (Polarities shown are for ICL7663. Reverse for ICL7664)

# TYPICAL PERFORMANCE CHARACTERISTICS

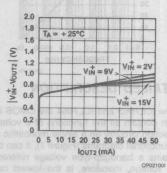
ICL7663 OUTPUT VOLTAGE AS A **FUNCTION OF OUTPUT CURRENT** 



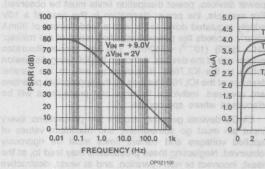
ICL7663 VOUT1 INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



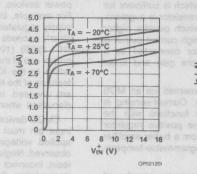
ICL7663 VOUT2 INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



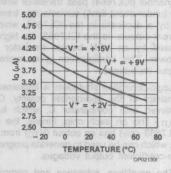
ICL7663 INPUT POWER SUPPLY ICL7663 QUIESCENT CURRENT AS



A FUNCTION OF INPUT VOLTAGE



ICL7663 QUIESCENT CURRENT AS A

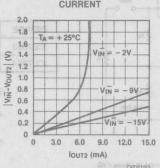


# TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

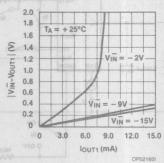
FUNCTION OF OUTPUT CURRENT -4.995 TA = + 25°C -4.990  $V_{IN} = -9.0V$ -4.985 **BOTH OUTPUTS** CONNECTED -4.980TOGETHER -4.975-4.970 -4.965-4.960-4.955-4.9501μΑ 10μΑ 100μΑ 1.0 10.0 100.0

ICL7664 OUTPUT VOLTAGE AS A

ICL7664 VOUT1 INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT

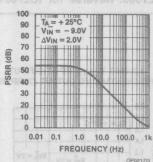


ICL7664 VOUT2 INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT

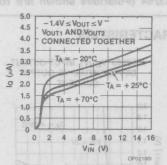


ICL7664 INPUT POWER SUPPLY
REJECTION RATIO

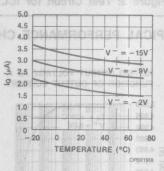
lour (mA)



ICL7664 QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



ICL7664 QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



#### DETAILED DESCRIPTION

The ICL7663 and ICL7664 are CMOS integrated circuits which contain all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the functional diagrams (Figure 1), it can be seen that each contains a bandgap-type voltage reference of 1.3 Volts. This voltage, therefore, is the lowest output voltage the regulators can control ( -1.3V for the ICL7664). Error amplifier A drives either a P-channel (ICL7663) or an N-channel (ICL7664) pass transistor which is sufficient for low (under about 5mA) currents; this transistor is augmented by a duplicate in the ICL7664, which permits higher current outputs. In the ICL7663, the high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via an MOS transistor of the appropriate polarity. Current-sensing is achieved with comparator C, which functions with the VouT2 line on each chip. Finally, the positive regulator (ICL7663 only) has an output (VTC) from a buffer amplifier (B), which can be used to generate programmable-temperature-coefficient output voltages.

The amplifiers, reference and comparator circuitry all operate at bias levels well below  $1\mu\mathrm{A}$  to achieve the

extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

#### BASIC OPERATION

The ICL7663 and ICL7664 are designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30mA clearly exceeds the power dissipation rating of the minidip: (10 – 2)(30) (10 – 3) = 240mW. The test circuit illustrates proper use of the devices. Although the following discussion refers to the ICL7663, it applies as well to the parallel features of the ICL7664 as long as the appropriate polarities are reversed. Individual features and precautions will be discussed where appropriate.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or non-operation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Input Voltages — These regulators accept working inputs of 1.4V to 18V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The  $0.047\mu\mathrm{F}$  capacitor on the device side of the switch will limit inputs to a safe level around  $2\mathrm{V}/\mu\mathrm{s}$ . Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output Voltages — The resistor divider  $R_2/R_1$  is used to scale the reference voltage,  $V_{SET}$ , to the desired output using the formula  $V_{OUT} = (1 + R_2/R_1)$   $V_{SET}$ . In the ICL7664,  $V_{IN}$  and  $V_{SET}$  are negative, so  $V_{OUT}$  will also be negative. Suitable arrangements of these resistors, using a potentiometer, enables exact values for  $V_{OUT}$  to be obtained. Because of the low leakage current of the  $V_{SET}$  terminal, these resistors can be tens of megohms for minimum additional quiescent drain current. However, *some* load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least  $1\mu A$ . This can include the current for  $R_2$  and  $R_1$ .

Output voltages up to nearly the  $V_{IN}$  supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the  $V_{OUT1}$  terminal.

Output Currents — For the ICL7663, low output currents of less than 5mA are obtained with the least input-output differential from the  $V_{OUT1}$  terminal (connect  $V_{OUT2}$  to  $V_{OUT1}$ ). Either output may be used on the ICL7664, with the unused output connected to  $V_{\citiNL}$ . Where higher currents are needed, use  $V_{OUT2}$  on the ICL7663 ( $V_{OUT1}$  should be left open in this case) and parallel  $V_{OUT1}$  and  $V_{OUT2}$  on the ICL7664

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing — The on-chip comparator (C in the block diagrams) permits shutdown of the regulator output in the event of excessive current drain. As the test circuits show, a current-limiting resistor,  $R_{CL}$ , is placed in series with  $V_{\rm OUT2}$ , and the SENSE terminal is connected to the load side of  $R_{CL}$ . When the current through  $R_{CL}$  is high enough to produce a voltage drop equal to  $V_{CL}$  (0.7V for ICL7663, 0.35V for ICL7664) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I $_{\rm LOAD}$ ) is determined, simply divide  $V_{CL}$  by  $I_{\rm LOAD}$  to obtain the value for  $R_{\rm CL}$ .

**Logic-Controllable Shutdown** — When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it is required. This usually means switches, with their unreliable contacts. Instead, the ICL7663 and ICL7664 can be shut down by a logic signal, leaving only  $I_Q$  (under  $4\mu A$ ) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663, and greater than

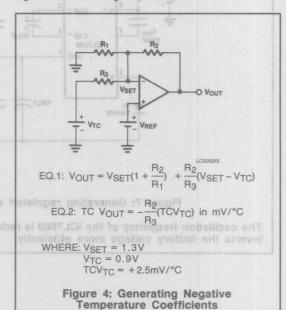
-0.3V for the ICL7664 will keep the regulator ON, and a voltage level of more than 1.4V but less than  $V_{1N}^{-}$  for the ICL7663, and less than -1.4V but not less than  $V_{1N}^{-}$  for the ICL7664 control will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V<sub>1N</sub> or V<sub>1N</sub>), the current from this signal should be limited to  $100\mu A$  maximum by a high-value (1M $\Omega$ ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

Additional Circuit Precautions — These regulators have poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

$$I = C \frac{\Delta V}{\Delta t}, C = I_{OUT} \frac{(20 \times 10^{-3})}{0.9 V_{OUT}} = 0.022 \frac{I_{OUT}}{V_{OUT}}$$

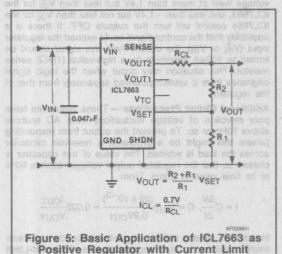
In addition, where such a capacitor is used, a currentlimiting resistor is also suggested (see "Current-Limit Sensing").

Producing Output Voltages With Negative Temperature Coefficients — The ICL7663 has an additional output (not present on the ICL7664) which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V<sub>SET</sub> pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R<sub>2</sub>/R<sub>3</sub> ratio (see Figure 4 and its design equations).

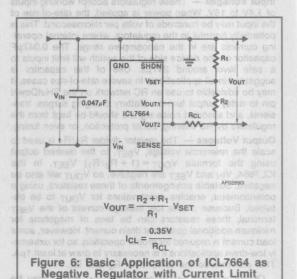


5-33

# APPLICATIONS IT GOOD HAVE AGE LOT AND TO VS.O.



Producing Output Voltages With Regalive Temperature



-O - 5V

\*Values depend on load characteristics

Figure 7: Generating regulated split supplies from a single supply.

ICL7664 SENSE

The oscillation frequency of the ICL7660 is reduced by the external oscillator capacitor, so that it inverts the battery voltage more efficiently.

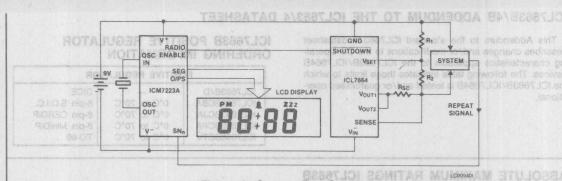


Figure 8: Once a Day System.

This circuit will turn on a regulated supply to a system for one minute every day, via the SHUTDOWN pin on the ICL7664, and under control of the ICM7223A Alarm Clock circuit. If the system decides it needs another one minute activation, pulling the REPEAT line to V<sup>+</sup> (GND) during one activation will trigger a subsequent activation after a snooze interval set by the choice of SN pins (2 mins shown). Alternatively, activation of the Sleep timer, without pause, can be achieved. See ICM7223A data sheet for details.

				LIMITS	
		PARAMETER TEST CONDITIONS		qvr.	
day					
	Quiescenti Cunent				
TREVA 7A	Tampenature Countrient	Ve > d₁V > va.e			
		2V < VĀ < 8V			
MONEY	Shutdown Input Vallage				
You		Vol. = Vours = VacNati (Current-Limit Transhold)			V
	Load Regulation				
		Open-Circuit Veltage			
			0		



# ICL7663B/4B ADDENDUM TO THE ICL7663/4 DATASHEET

This Addendum to the standard ICL7663/4 datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7663B/ICL7664B devices. The following table indicates those limits to which the ICL7663B/ICL7664B is tested and/or guaranteed operational.

# ICL7663B POSITIVE REGULATOR ORDERING INFORMATION

P(	OSITIVE REGULA	TOR
ICL7663B/D ICL7663BCBA ICL7663BCJA ICL7663BCPA	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	DICE 8-pin S.O.I.C. 8-pin CERDIP 8-pin MiniDIP TO-99

# **ABSOLUTE MAXIMUM RATINGS ICL7663B**

Input Supply Voltage	Output Sinking Current (Terminal 7)10mA Power Dissipation (Note 2)
4, 5, 6, 7)(GND $-0.3V$ ) to $(V_{1N}^{-1} + 0.3V)$	MiniDIP200mW
Output Source Current	TO-99 Can
(Terminal 2)	Alternatively, activation of the Sleep timer, with

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# ICL7663B OPERATING CHARACTERISTICS VIN = 9V, VOUT = 5V, TA = +25°C, unless otherwise specified.

				LIMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNI
ν <sub>ι</sub> τ΄	Input Voltage	T <sub>A</sub> = +25°C 20°C ≤ T <sub>A</sub> ≤ +70°C	1.5 1.6		10 10	٧
Ia	Quiescent Current	$ \begin{cases} R_L = \infty \\ 1.4V \le V_{OUT} \le 8.5V \end{cases} $		3.5	10	μА
VSET	Reference Voltage		1.2	1.3	1.4	٧
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	8.5V < V <sub>IN</sub> < 9V		±200		ppn
$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	Line Regulation	2V < VIN < 9V		0.03		%/
ISET	V <sub>SET</sub> Input Current			±0.01	10	nA
ISHDN	Shutdown Input Current			±0.01	10	nA
VSHDN	Shutdown Input Voltage	V <sub>SHDN</sub> HI: Both V <sub>OUT</sub> Disabled V <sub>SHDN</sub> LO: Both V <sub>OUT</sub> Enabled	1.4		0.3	٧
ISENSE	Sense Pin Input Current			0.01	10	n/
VCL	Sense Pin Input Threshold Voltage	V <sub>CL</sub> = V <sub>OUT2</sub> - V <sub>SENSE</sub> (Current-Limit Threshold)		0.7		٧
RSAT	Input-Output Saturation Resistance (Note 3)	$V_{1\dot{N}}^{+} = 2V$ $V_{1\dot{N}}^{+} = 9V$		200 70		Ω
ΔV <sub>OUT</sub>	Lood Regulation	ΔΙ <sub>ΟUΤ1</sub> = 100μΑ @ V <sub>OUT1</sub> = 5V		2		Ω
ΔΙΟυΤ	Load Regulation	$\Delta I_{OUT2} = 10 \text{mA} @ V_{OUT2} = 5 \text{V}$		1		22
lout2	Available Output Current (VOUT2)	$V_{IN}^{\dagger} = 3V$ $V_{OUT} = V_{SET}$ $V_{IN}^{\dagger} = 9V$ $V_{OUT} = 5V$	10 25			m/
VTC	Negative-Tempco Output (Note 4)	Open-Circuit Voltage		0.9		V
ITC	Negative-Tempco Output (Note 4)	Maximum Sink Current	0	8	2	m/

# ICL7663/7664

# **WINTERSIL**

# ICL7663B OPERATING CHARACTERISTICS (CONT.)

OVERDOL	DADAMETED		TEST CONDITIONS MOVE	LIMITS			
SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient	SOLU	Open Circuit	off out	+ 2.5		mV/°C
. ΔΤ		36136 77	THE STORM NIGHT OF	dir de 20	or la	ACTION	805 151
I <sub>L</sub> (min)	Minimum Load Current	lagues au	(Includes V <sub>SET</sub> Divider)	to + XI	n-	vibes	μА

NOTES: 1. Connecting any terminal to voltages greater than (V<sub>IN</sub> +0.3V) or less than (GND -0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663B power-up.

2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance. 4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V<sub>SET</sub>, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

PARAMETER	PARAMETER TEST CONDITIONS		GYT	MAX			
SpattoV fugit							
				b.1-			
	V8->5/V>V\$-						
Soundown Input Violege	Vennulth Both Vour Disabled Ventual D Both Voor Embred						
Sensa Pin Input Threshold Voltage							
			s				
Misseum Load Conset (Includes Verry Divider)							

NOTES: 1 Commenting any terminal to veltages greater than (GND + 0.3V) or less than (Vig. +0.3V) may obuse districtive device latchup, it less recommended that no inputs from sources operating on external gower supplies as applied prior to ICL7664B power-up.

2 Distriction above 50°C at SmW/°C for ministip and 7.5mW/°C for TO-80 can

3 This parameter reters to the saturation resistance of the MOS pass transition. The minimum input output voltage oilliteratinal can be determined.

# ORDERING INFORMATION

	Negative Regulator						
ICL7664BCPA	0 to +70°C	8-pin MiniDIP					
ICL7664BCTV	0 to +70°C	TO-99					
ICL7664B/D	man cause destroys	DICE					
ICL7664BCBA	0 to +70°C	8-pin S.O.I.C					
ICL7664BCJA	0 to +70°C	8-pin CERDIP					

# ABSOLUTE MAXIMUM RATINGS ICL7664B

Input Supply Voltage	– 12V
Any Input or Output Voltage (Note 1)	
(Terminals 1,2,3,4,5,6,7,)	(GND + 0.3V)
erate linearly above 50°C at 5mWW°C for mindle and	to (VIN-0.3V)
Output Source Current	
(Terminal 1,7)	25mA
Power Dissipation (Note 2)	
MiniDIP	200mW
TO-99	300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# ICL7664B OPERATING CHARACTERISTICS $V_{\overline{1N}} = 9V$ , $V_{out} = -5V$ , $T_A = +25^{\circ}C$ , unless otherwise specified.

	DAGAMETER	TEST CONDITIONS				
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V <sub>IN</sub>	Input Voltage	T <sub>A</sub> = +25°C 0 ≤ T <sub>A</sub> ≤ +70°C	-1.5 -1.6		-10 -10	٧
la	Quiescent Current	$R_L = \infty$ $\{-1.4V \le V_{OUT} \le -8.5V\}$	3.5	10	μΑ	
VSET	Reference Voltage		-1.2	-1.3	-1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	-8.5V < V <sub>IN</sub> < -9V		±200		ppm
ΔV <sub>SET</sub> V <sub>SET</sub> ΔV <sub>IN</sub>	Line Regulation	-2V < V <sub>IN</sub> < -9V		0.03		%/\
ISET	V <sub>SET</sub> Input Current			±0.01	10	nA
ISHDN	Shutdown Input Current			±0.01	10	nA
VSHDN	Shutdown Input Voltage	VSHDNHI: Both VOUT Disabled VSHDNLO: Both VOUT Enabled	-0.3		-1.4	٧
ISENSE	Sense Pin Input Current			0.01	10	nA
VCL	Sense Pin Input Threshold Voltage	V <sub>CL</sub> = V <sub>OUT2</sub> - V <sub>SENSE</sub> (Current-Limit Threshold)		-0.35		٧
RSAT	Input-Output Saturation Resistance (Note 3)	V <sub>IN</sub> = 2V V <sub>IN</sub> = 9V		150 40		Ω
ΔV <sub>OUT</sub>	Lead Barden	ΔΙ <sub>ΟΙJT1</sub> = 100μΑ @			4000	0
ΔΙουτ	Load Regulation	$\Delta I_{OUT} = -5V$		2		Ω
Гоит	Output Current VOUT1 or VOUT2	V <sub>IN</sub> = 3V V <sub>OUT</sub> = V <sub>SET</sub> V <sub>IN</sub> = 9V V <sub>OUT</sub> = -5V		-2 -20		mA
I <sub>L</sub> (min)	Minimum Load Current (Includes V <sub>SET</sub> Divider)				1	μΑ

NOTES: 1. Connecting any terminal to voltages greater than (GND +0.3V) or less than (V<sub>IN</sub> -0.3V) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664B power-up.

2. Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

# **FEATURES**

- Exceptionally Low Supply Current ( < 3μA Typ)</li>
- Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels

PARAMETER

- Accurate On-Chip Bandgap Reference
- Up to 20mA Output Current Sinking Ability
- Wide Supply Voltage Range

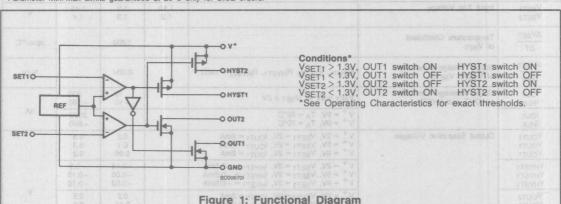
#### GENERAL DESCRIPTION

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only  $3\mu A$  typical for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. Typical applications are battery-backup computer memories, battery-operated medical devices, radiation dosimeters, pocket pagers, portable calibrators, test instruments, and charging systems.

# ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665CPA	0°C to +70°C	8 Lead MiniDIP
ICL7665CTV	0°C to +70°C	8 Lead TO-99
ICL7665/D	- 87	DICE
ICL7665CBA	0°C to 70°C	8 Lead SOIC
ICL7665CJA	0°C to 70°C	8 Lead CERDIP

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



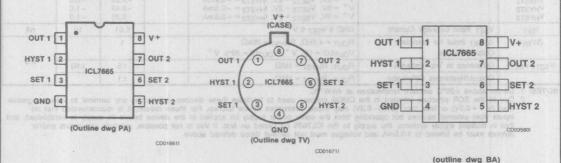


Figure 2: Pin Configurations

5-39

302067-002

Note: All typical values have been guaranteed by characterization and are not tested.

5

# ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....-0.3V to +18V Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2) .....-0.3V to +18V Output Voltages HYST1 and HYST2 (with respect to V<sup>+</sup>) (Note 2).....+0.3V to -18V Input Voltages SET1 and SET2 (Note 2) ......(GND - 0.3V) to (V<sup>+</sup> +0.3V)

Maximum Sink Output Current OUT1 and OUT2...25mA Maximum Source Output Current HYST1 and HYST2 .....-25mA 

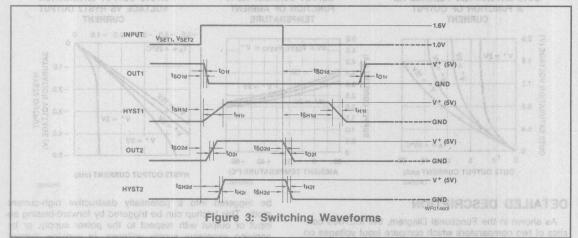
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

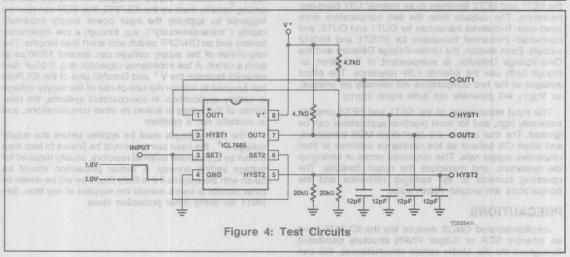
# **ELECTRICAL CHARACTERISTICS** DC OPERATING CHARACTERISTICS (V + = 5V, TA = +25°C, unless otherwise specified. See Test Circuit Fig. 4)

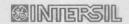
			SELECTION OF THE PARTY OF THE P			THE PERSON	AND THEFT
			Service Service	and a second	LIMITS		UNIT
SYMBOL	PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	
V+	Operating Supply Voltage	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$	9010	1.6 1.8		16 16	d/ssa,TC
1+	Supply Current	GND ≤ V <sub>SET1</sub> , V <sub>SET2</sub> All Outputs Open Cir	2 ≤ V to a baal a	70%	01'0'10	4	SLY665CE
		V + = 2V V + = 9V	E Lead CERDIP		2.5	10	1,7865CJ
		V + = 15V	enterio BOIG nel vino	0°85 to 6	2.9	15	μΑ
VSET1 VSET2	Input Trip Voltage			1.15	1.3 1.3	1.45 1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of VSET		'vo 1.	-	±200		ppm/°C
ΔV <sub>S</sub> ET ΔV <sub>S</sub>	Supply Voltage Sensitivity of VSET1, VSET2	ROUT1, ROUT2, RHYST1, RHYST2 = 1MΩ			0.004		%/V
OLK HLK	Output Leakage Currents on OUT and HYST	V <sub>SET</sub> = 0V or V <sub>SET</sub> =	≥ 2V		10 -10	200	
IOLK IHLK		V + = 9V, T <sub>A</sub> = 70°C V + = 9V, T <sub>A</sub> = 70°C	61V0 O	- Fail-	1	2000 -500	nA
VOUT1 VOUT1 VOUT1	Output Saturation Voltages	V + = 2V, V <sub>SET1</sub> = 2V V + = 5V, V <sub>SET1</sub> = 2V V + = 9V, V <sub>SET1</sub> = 2V	V. IOLIT1 = 2mA		0.2 0.1 0.06	0.5 0.3 0.2	0.00
VHYST1 VHYST1 VHYST1		V + = 2V, V <sub>SET1</sub> = 2V V + = 5V, V <sub>SET1</sub> = 2V V + = 9V, V <sub>SET1</sub> = 2V	$V$ , $I_{HYST1} = -0.5 \text{mA}$		-0.15 -0.05 -0.02	-0.3 -0.15 -0.10	
VOUT2 VOUT2 VOUT2		V + = 2V, V <sub>SET2</sub> = 0V V + = 5V, V <sub>SET2</sub> = 0V V + = 9V, V <sub>SET2</sub> = 0V	V. IOUT2 = 2mA		0.2 0.15 0.11	0.5 0.3 0.25	V
VHYST2 VHYST2 VHYST2		V <sup>+</sup> = 2V, V <sub>SET2</sub> = 2V V <sup>+</sup> = 5V, V <sub>SET2</sub> = 2V V <sup>+</sup> = 9V, V <sub>SET2</sub> = 2V	$V_{\rm HYST2} = -0.5 \text{mA}$		-0.25 -0.43 0.35	-0.8 -1.0 -1.0	
ISET	V <sub>SET</sub> Input Leakage Current	GND SVSET V	570 100	DE HE	0.01	10	nA
ΔV <sub>SET</sub>	ΔV <sub>SET</sub> Input for Complete Output Change	$R_{OUT} = 4.7k\Omega$ , $R_{HYS}$ $V_{OUTLO} = 1\% V^+$ ,		0.700	1	y	1 100
VSET1-VSET2	Difference in Trip Voltages	ROUT, RHYST = 1MS	2		±5	±50	mV
	Output/Hysteresis Difference	ROUT, RHYST = 1MS	2 10 1 - 700	SET 2	8 ±1		1 738

NOTES: 1. Derate above ±25°C ambient temperature at 4mW/°C.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V + +0.3V) or less than (GND-0.3V) may cause destructive device latchup. For these reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

	HYSTI OUTPUT TEST CONDITIONS IN		MA SDAT.	LIMITS AND		
	PARAMETER TEST CONDITIONS	MIN	TYP	MAX	UNITS	
tsO1d	Output Delay Time	V <sub>SFT</sub> Switched from 1.0V to 1.6V		70	5	0
tSH1d tSO2d tSH2d	Input Going HI	$R_{OUT} = 4.7k\Omega$ , $C_L = 12pF$ $R_{HYST} = 20k\Omega$ , $C_L = 12pF$	0.984 = 1	00	ty a	μs
tsO1d tsH2d tsO2d tsH2d	Output Delay Time Input Going LO	$V_{SET}$ Switched from 1.6V to 1.0V ROUT = 4.7k $\Omega$ , $G_L$ = 12pF RHYST = 20k $\Omega$ , $G_L$ = 12pF	1000	1040 610 70 30	21	μs
tO1r tO2r tH1r tH2r	Output Rise Times	$\begin{array}{l} \text{V}_{\text{SET}} \text{ Switched between 1.0V and 1.6V} \\ \text{R}_{\text{OUT}} = 4.7 k \Omega, \text{ C}_{\text{L}} = 12 \text{pF} \\ \text{R}_{\text{HYST}} = 20 k \Omega, \text{ C}_{\text{L}} = 12 \text{pF} \end{array}$		120 80 330 25	1 s	μs
<sup>†</sup> O1f <sup>†</sup> O2f <sup>†</sup> H1f <sup>†</sup> H2f	Output Fall Times	$V_{SET}$ Switched between 1.0V and 1.6V ROUT = 4.7k $\Omega$ , CL = 12pF RHYST = 20k $\Omega$ , CL = 12pF	08 81 (Am) 1913 usseno	30 60 180 30	i jituo Outiji	μs



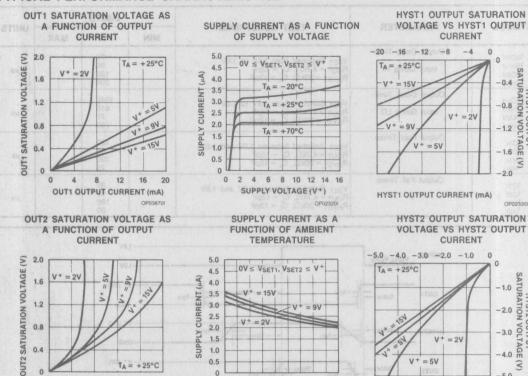




-5.0

OP02360I

# TYPICAL PERFORMANCE CHARACTERISTICS



0 +20

AMBIENT TEMPERATURE (°C)

+40

0

## DETAILED DESCRIPTION

8 4

**OUT2 OUTPUT CURRENT (mA)** 

As shown in the Functional Diagram, the ICL7665 consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal, so VSFT1 will generally not quite equal VSFT2.

12 16

The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

#### **PRECAUTIONS**

Junction-isolated CMOS devices like the ICL7665 have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can

be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low current analog circuits, such as the ICL7665, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/us in such a circuit. A low-impedance capacitor (e.g. 0.05 µF disc ceramic) between the V+ and GrouND pins of the ICL7665 can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rateof-rise of the supply is limited by other considerations, and is normally not a problem.

HYST2 OUTPUT CURRENT (mA)

If the SET voltages must be applied before the supply voltage V+, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

# **APPLICATIONS**

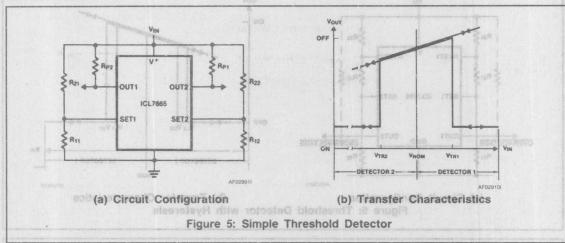


Figure 5 shows the simplest connection of the ICL7665 for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward VNOM (usually the eventual operating voltage), OUT2 goes high on reaching VTR2. If the voltage rises above VNOM as much as VTR1, OUT1 goes low. The equations giving VSET1 and VSET2 are, from Figure 1(a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})}; \quad V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value of  $V_{\mbox{\scriptsize IN}}$  for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}}$$
 for detector 1

and

$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}}$$
 for detector 2.

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V<sub>IN</sub> is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF

conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Figure 6(a) shows how to set up such hysteresis, while Figure 6(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether  $V_{\rm IN}$  is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out  $R_{\rm 31}$  or  $R_{\rm 32}$  when  $V_{\rm IN}$  is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by  $R_{\rm 1n}$ ,  $R_{\rm 2n}$  and  $R_{\rm 3n}$ , until the trip point is reached. As this value is passed, the detector changes state,  $R_{\rm 3n}$  is shorted out, and the trip point becomes controlled by only  $R_{\rm 1n}$  and  $R_{\rm 2n}$ , a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 7. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about  $100 \mathrm{k}\Omega.$ 

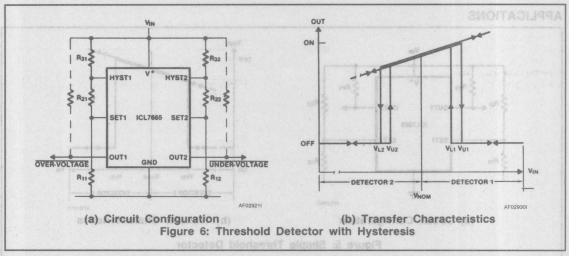
D) HYSTERESIS PER FIGURE SA

VUI = RII + R2I + R3I × VSETI

VUI = RII + R2I + R3I × VSETI

VII = RII + R2I + R3I × VSETI

VII = RII + R3I × VSETI



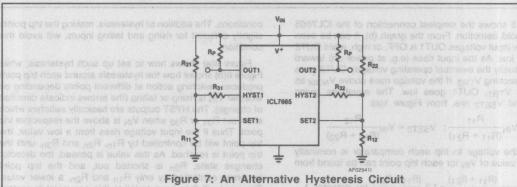


Table 1. Set-Point Equations

# a) NO HYSTERESIS Over-Voltage $V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$ Under-Voltage $V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$ b) HYSTERESIS PER FIGURE 6A $V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$ $V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$ Under-Voltage $V_{TRIP}$ $V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$ $V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$

c) HYSTERESIS PER FIGURE 7
$$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$
Over-Voltage  $V_{TRIP}$ 

$$V_{L1} = \frac{R_{11} + R_{21}R_{31}}{R_{21} + R_{31}} \times V_{SET1}$$

$$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$
Under-Voltage  $V_{TRIP}$ 

$$V_{L2} = \frac{R_{12} + R_{22}R_{32}}{R_{12}} \times V_{SET2}$$

# ICL7665B ADDENDUM TO THE ICL7665 DATASHEET

This Addendum to the standard ICL7665B datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7665B device. The following table indicates those limits to which the ICL7665B is tested and/or guaranteed operational.

# ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665BCPA	0 to +70°C	8 Lead MiniDIP
ICL7665BCTV ICL7665B/D	0 to +70°C	8 Lead TO-99 DICE Only
ICL7665BCJA ICL7665BCBA	0 to +70°C 0 to +70°C	8-Lead Cerdip 8-Lead S.O.I.C.

# ABSOLUTE MAXIMUM RATINGS, ICL7665B

Supply Voltage	0.3V to +12V
Output Voltages OUT1 and OUT2 (v	vith respect to
GND) (Note 2)	0.3V to +12V
Output Voltages HYST1 and HYST2	(with respect to
V <sup>+</sup> ) (Note 2)	+0.3V to -12V
Input Voltages SET1 and SET2	
(Note 2)(GND -0	.3V) to $(V^+ + 0.3V)$

Maximum Sink Output Current OUT1 and OUT2 25	5mA
Maximum Source Output Current HYST1	
and HYST225	5mA
Power Dissipation (Note 1)200	mW
Operating Temperature Range 0 to +7	O°C
Storage Temperature Range55°C to +12	5°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC OPERATING CHARACTERISTICS $V^+ = 5V$ , $T_A = +25$ °C, unless otherwise specified.

CVMDOI	BARAMETER	DADAMETER TEST COMPLETIONS		LIMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
٧+	Operating Supply Voltage	T <sub>A</sub> = +25°C 0 ≤ T <sub>A</sub> ≤ +70°C	1.6 1.8		10 10	٧
1+	Supply Current	GND ≤ V <sub>SET1</sub> , V <sub>SET2</sub> ≤ V <sup>+</sup> All Outputs Open Circuit V <sup>+</sup> = 2V V <sup>+</sup> = 9V		2.5 2.6	10	μΑ
VSET1 VSET2	Input Trip Voltage		1.15	1.3 1.3	1.45 1.4	٧
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of VSET			±200		ppm/°(
$\frac{\Delta V_{SET}}{\Delta V_{S}}$	Supply Voltage Sensitivity of V <sub>SET1</sub> , V <sub>SET2</sub>	$R_{OUT1}$ , $R_{OUT2}$ , $R_{HYST1}$ , $R_{HYST2} = 1M\Omega$		0.004		%/V
lolk IHLK	Output Leakage Currents on OUT and HYST	V <sub>SET</sub> = 0V or V <sub>SET</sub> ≥ 2V		10 -10	200 -100	
lolk lhlk		V + 9V, TA = 70°C V + 9V, TA = 70°C			2000 -500	nA
VOUT1 VOUT1 VOUT1	Output Saturation Voltages	V + 2V, V <sub>SET1</sub> = 2V, I <sub>OUT1</sub> = 2mA V + 5V, V <sub>SET1</sub> = 2V, I <sub>OUT1</sub> = 2mA V + 9V, V <sub>SET1</sub> = 2V, I <sub>OUT1</sub> = 2mA		0.2 0.1 0.06	0.5 0.3 0.25	
VHYST1 VHYST1 VHYST1		V + 2V, V <sub>SET1</sub> = 2V, I <sub>HYST1</sub> = -0.5mA V + 5V, V <sub>SET1</sub> = 2V, I <sub>HYST1</sub> = -0.5mA V + 9V, V <sub>SET1</sub> = 2V, I <sub>HYST1</sub> = -0.5mA		-0.15 -0.05 -0.02	-0.3 -0.15 0.15	
VOUT2 VOUT2 VOUT2		V + 2V, V <sub>SET2</sub> = 0V, I <sub>OUT2</sub> = 2mA V + 5V, V <sub>SET2</sub> = 0V, I <sub>OUT2</sub> = 2mA V + 9V, V <sub>SET2</sub> = 0V, I <sub>OUT2</sub> = 2mA		0.2 0.15 0.11	0.5 0.3 0.3	٧
VHYST2 VHYST2 VHYST2		V + 2V, VSET2 = 2V, IHYST2 = -0.2mA V + 5V, VSET2 = 2V, IHYST2 = -0.5mA V + 9V, VSET2 = 2V, IHYST2 = -0.5mA		-0.25 -0.43 0.35	-0.8 -1 -1	

# ICL7665



# DC OPERATING CHARACTERISTICS (CONT.)

SYMBOL	DADAMETER	TEST COMPLETIONS	LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ISET	V <sub>SET</sub> Input Leakage Current	GND ≤ V <sub>SET</sub> ≤ V +	OF STRUCTURE	0.01	10	nA
ΔVSET	ΔV <sub>SET</sub> Input for Complete Output Change	$R_{OUT} = 4.7k\Omega$ , $R_{HYST} = 20k\Omega$ $V_{OUTLO} = 1\% \text{ V}^+$ , $V_{OUTHI} = 99\% \text{ V}^+$	nits to wis	osorti i	and and	der gniwo
VSET1-VSET2	Difference in Trip Voltages	ROUT, RHYST = 1MΩ	Manays le	±5	±50	mV.
Virgo	Output/Hysteresis Difference	Rout, Rhyst = 1MΩ		±1		

NOTES: 1. Derate above ±25°C ambient temperature at 4mW/°C.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V + 0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665B be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Assume Source Corput Current HYST?  and HYST?  Power Dissipation (Note 1) 200mV  Operating Temperature Range 0 to + 70°C  Storage Temperature Range55°C to + 125°C	### Voriages OUT and OUT# (with respect to the voltages hyST1 and HYST2 (with respect to the voltages SET1 and SET2
	sses above those listed under "Absolute Maximum Patings" may cause po

# DC OPERATING CHARACTERISTICS V+ = SV, TA = +25°C, unless otherwise specified.

		STIMIL			
CIMITS	36,00.9		MIN		
Ац		2.5			
V		67			
				Temporature Coefficient of Year	
				Supply Voltage Sensitivity of Vector Vecto	
				Output Semistion Voltages	

## GENERAL DESCRIPTION

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and 1.5A peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs (1.5A peak) minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control IC's.

- • 1.5A Peak Output Current
- Fast Rise and Fall Times | prills and reserved.
- 40ns With 1000pF Load
- Wide Supply Voltage Range - VCC = 4.5 to 15V
- Low Power Consumption -4mW With Inputs Low
  - 120mW With Inputs High
  - TTL/CMOS Input Compatible Power Driver  $-Rout = 6\Omega$
  - Direct Interface With Common PWM Control IC's
  - Pin Equivalent to DS0026/DS0056; TSC426

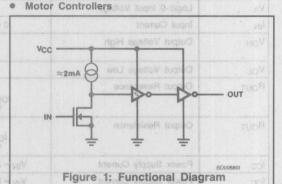
# TYPICAL APPLICATIONS

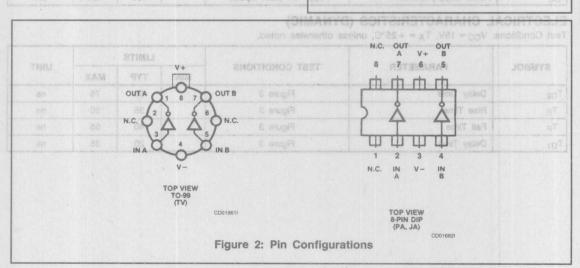
- Switching Power Supplies
- DC/DC Converters

# ORDERING INFORMATION

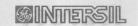
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7667MTV ICL7667MJA	-55°C to +125°C	TO-99 Can 8-Pin Cerdip
ICL7667CPA ICL7667CJA ICL7667CTV	0°C to +70°C	8-Pin Plastic 8-Pin Cerdip TO-99 Can
ICL7667/D		DICE**

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.





# ICL7667



# **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage		
Peak Output Curren		
Package Dissipation	, T <sub>A</sub> = 25°C	500mW
Linear Derati	ng Factors Plastic 5.6mW/°C	
TO-99	Plastic	Cerdip
6.7mW/°C	5.6mW/°C	6.7mW/°C
above 50°C	above 36°C	above50°C

Storage Temperature	65°C to +150°C
Operating Temperature Range	
ICL7667C	
ICL7667M	55°C to +125°C
Lead Temperature (Soldering, 10se	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **ELECTRICAL CHARACTERISTICS (STATIC)**

Test Conditions: V<sub>CC</sub> = 4.5 to 15V, T<sub>A</sub> = +25°C unless otherwise noted.

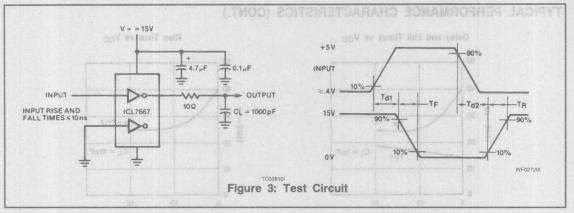
TSC426	quinalent to DS0026/DS0056;		ena aluqn	LIMITS	ce. The K	Bhosqao etag
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH	Logic 1 Input Voltage	STOR & STORY	2.4			٧
VIL	Logic 0 Input Voltage	07676 9			0.8	٧
I <sub>IN</sub>	Input Current	0 < VIN < VCC	-11/40	0	OFILE	μΑ
Vон	Output Voltage High	No Load	V <sub>CC</sub> -0.05	Vcc	T	TRAS
VoL	Output Voltage Low	No Load		0	0.05	V
ROUT	Output Resistance	$V_{IN} = V_{IL}$ $I_{OUT} = -10 \text{mA}$ $V_{CC} = 15 \text{V}$	6   O'85 6   O	6	20	ROLZBOZOPA
Rout	Output Resistance	$V_{IN} = V_{IH}$ $I_{OUT} = 10$ mA $V_{CC} = 15V$		6	20	VFOXΩ (JOI GAYBBYJOI
lcc	Power Supply Current	V <sub>IN</sub> = 3V (both inputs)	10 0°85 la	4 4 4	alimi 6 mili	M mA
Icc mark	Power Supply Current	V <sub>IN</sub> = 0V (both inputs)		150	400	μΑ

# **ELECTRICAL CHARACTERISTICS (DYNAMIC)**

Test Conditions: V<sub>CC</sub> = 15V, T<sub>A</sub> = +25°C, unless otherwise noted.

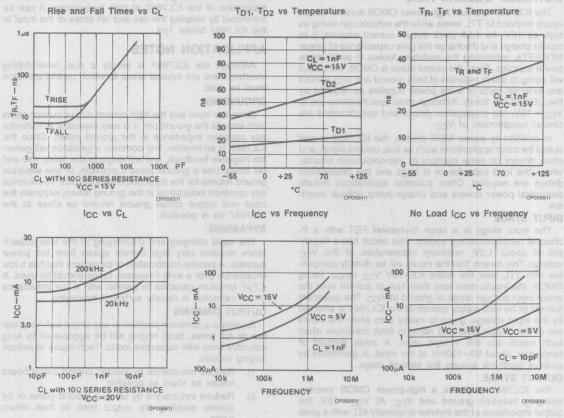
ovumo.	0 +V A	TEAT COMPLETIONS				
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>D2</sub>	Delay Time	Figure 3		50	75	ns
TR	Rise Time	Figure 3	3 6	35	50	ns
TF	Fall Time	Figure 3	44	40	55	ns
T <sub>D1</sub>	Delay Time	Figure 3		20	35	ns

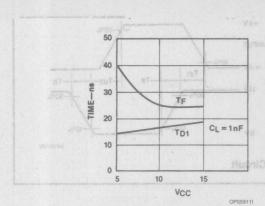
Floure 2: Pin Conflourations

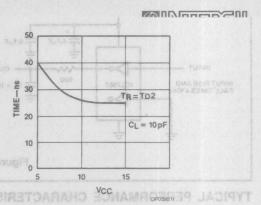


# TYPICAL PERFORMANCE CHARACTERISTICS

NOTE: With the  $10\Omega$  resistor shorted (or removed), the rise, fall and delay times will be decreased by typically 10%.







#### DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its 1.5A peak output current, enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and  $V_{\rm CC}$  without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at  $V_{\rm CC}=15V$ , the propagation delays and specifications are almost independent of  $V_{\rm CC}$ .

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

#### INPUT STAGE

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V<sub>CC</sub> voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5–15V V<sub>CC</sub> range. Being CMOS, the inputs draw less than 1 $\mu$ A of current over the entire input voltage range of ground to V<sub>CC</sub>. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 6mA maximum when both inputs are the 1 logic level. A small amount of hysteresis, about 50–100mV at the input, is generated by positive feedback around the second stage.

#### **OUTPUT STAGE**

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V<sub>CC</sub>. At V<sub>CC</sub> = 15V, the output impedance of the inverter is typically 6 $\Omega$ , with a peak current output of typically 1.5A. It is this high peak current capability that enables the ICL7667 to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V<sub>CC</sub> to ground) during output transitions. This crossover current is

responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below  $1\mu s$ .

# **APPLICATION NOTES**

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

#### GROUNDING

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

#### BYPASSING

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A  $4.7\mu\text{F}$  tantalum capacitor in parallel with a low inductance  $0.1\mu\text{F}$  capacitor is usually sufficient bypassing.

#### **OUTPUT DAMPING**

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

- Reduce inductance by making printed circuit board traces as short as possible.
- Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
- Use a 10 to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
- Use good bypassing techniques to prevent ringing caused by supply voltage ringing.

#### POWER DISSIPATION

The power dissipation of the ICL7667 has three main components:

- 1) Input inverter current loss
- 2) Output stage crossover current loss
- 3) Output stage I<sup>2</sup>R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I<sub>CC</sub> of 0.2mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. Caution: The inputs should never be allowed to remain between  $V_{\rm IL}$  and  $V_{\rm IH}$  since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. NEVER leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in  $I_{\rm CC}$  vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I<sup>2</sup>R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

Where C = Load Capacitance f = Frequency

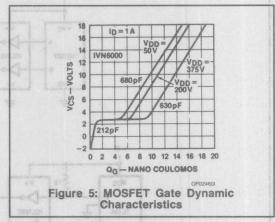
In cases where the load is a power MOSFET and the gate drive requirements are described in terms of gate charge, the ICL7667 power dissipation will be

Where  $Q_G$  = Charge required to switch the gate, in Coulombs. f = Frequency

# POWER MOS DRIVER CIRCUITS POWER MOS DRIVER REQUIREMENTS

Because it has a very high peak current output, the ICL7667 excels at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 5 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and

is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.



#### DIRECT DRIVE OF MOSFETS

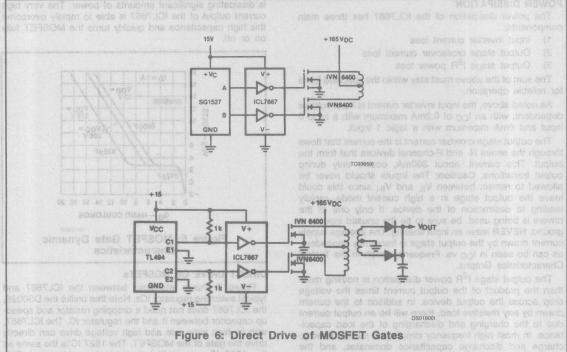
Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

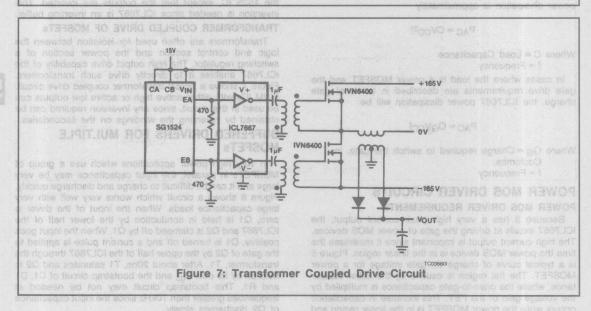
#### TRANSFORMER COUPLED DRIVE OF MOSFETS

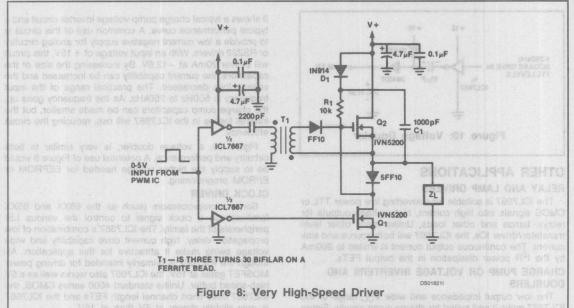
Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 7 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low outputs can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

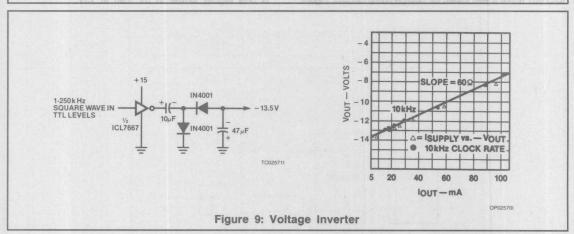
# BUFFERED DRIVERS FOR MULTIPLE MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own Cgs and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

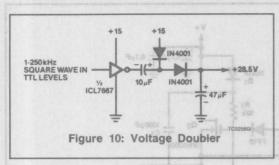












# OTHER APPLICATIONS

#### RELAY AND LAMP DRIVERS

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I<sup>2</sup>R power dissipation in the output FETs.

# CHARGE PUMP OR VOLTAGE INVERTERS AND DOUBLERS

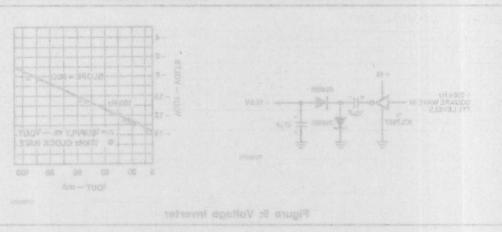
The low output impedance and wide V<sub>CC</sub> range of the ICL7667 make it well suited for charge pump circuits. Figure

9 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 10, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

# CLOCK DRIVER

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.



# ICL7673 Automatic Battery Back-up Switch

#### GENERAL DESCRIPTION

The Intersil ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alivebattery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

The ICL7673 is available in either an 8-pin plastic minidip package, a TO-99 metal can, or as dice.



#### **FEATURES**

- Automatically Connects Output to The Greater
   Of Either Input Supply Voltage
- If Main Power to External Equipment Is Lost,
   Circuit Will Automatically Connect Battery
   Backup
- Reconnects Main Power When Restored
- Logic Indicator Signaling Status Of Main Power
- Low Impedance Connection Switches
- Low Internal Power Consumption
- Wide Supply Range: 2.5 to 15 Volts
- Low Leakage Between Inputs
- External Transistors May Be Added If Very Large Currents Need to Be Switched

#### **APPLICATIONS**

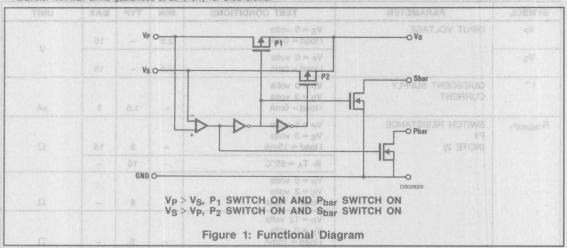
- On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs
- Over/Under Voltage Detector
- Peak Voltage Detector
- Other Uses:
  - Portable Instruments, Portable Telephones, Line Operated Equipment

(Gutline L

# ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7673CPA	0°C to +70°C	8-pin minidip
ICL7673CBA	0°C to +70°C	8-pin SOIC
ICL7673ITV	-25°C to +85°C	8-pin TO-99
ICL7673/D	malliners paterarity south: 3%	DICE ONLY**

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



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# ICL7673

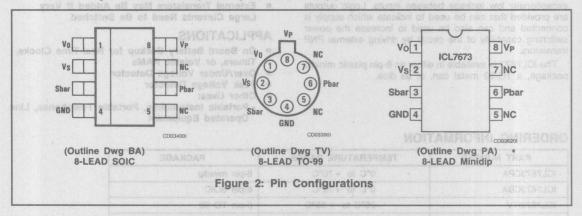


# **ABSOLUTE MAXIMUM RATINGS**

Input Supply (Vp or Vs) Voltage0.3 to	+18V
Output Voltages Pbar and Sbar0.3 to	
Peak Current	
induit $Ab = (a) Ab = bA = bA = bA$	JOHA
Input Vs (@ Vs = 3V)	.30mA
Phas or Shart Pasto V VIII To A Shart I will be	150mA
Continuous Current	
Input Vp (@ Vp = 5V) (note 1)	. 38mA
Input Vs (@ Vs = 3V)	.30mA
Phar or Shar	.50mA
gis Indicator Signaling Status Of Main Power	

Package Dissipation	300mW
Linear Derating Fac	tors
5.7mW/°C above 50°C	PLASTIC 6.1mW/°C above 36°C
Operating Temperature Ran ICL7673CPA/CBA	nge: 0°C to +70°C
Storage Temperature	
Lead Temperature (Soldering	ng, 10sec)300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>P</sub>	INPUT VOLTAGE	V <sub>S</sub> = 0 volts I load = 0mA	2.5	W _	15	V
Vs		V <sub>P</sub> = 0 volts I load = 0mA	2.5	w -	15	V
1+	QUIESCENT SUPPLY CURRENT	Vp = 0 volts Vs = 3 volts I load = 0mA	-	1.5	5	μΑ
R <sub>ds(on)P1</sub>	SWITCH RESISTANCE P1 (NOTE 2)	V <sub>P</sub> = 5 volts V <sub>S</sub> = 3 volts I load = 15mA	-	8	15	Ω
		@ T <sub>A</sub> = 85°C	-	16	-	
	SWITCH ON	V <sub>P</sub> = 9 volts V <sub>S</sub> = 3 volts I load = 15mA	g/L	6	_	Ω
	. эмітся он gram	Vp = 12 volts Vs = 3 volts I load = 15mA	-	5	_	Ω
T <sub>C(P1)</sub>	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P1	V <sub>P</sub> = 5 volts V <sub>S</sub> = 3 volts I load = 15mA	-	2.03	-	%/°C

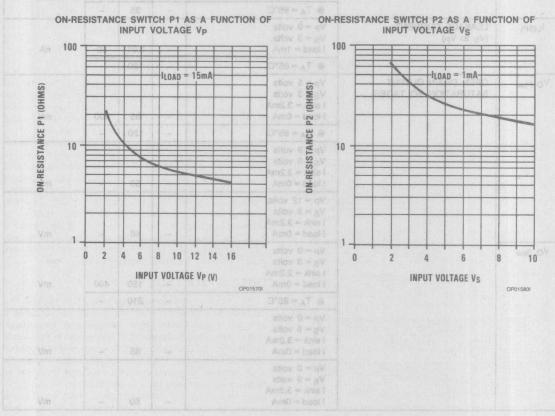
# ELECTRICAL CHARACTERISTICS (CONT.) (TMOO) BOITEIFFTOARANO JAORITOFIE

SYMBOL	PARAMETER 2000	TIONO TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rds(on)P2	SWITCH RESISTANCE P2 (NOTE 2)	V <sub>P</sub> = 0 volts V <sub>S</sub> = 3 volts I load = 1mA	30 -180	87 40	HEPAUS 100	Ω
	- 009 -	@ T <sub>A</sub> = 85°C	-	60	-	
	008 08	Vp = 0 volts Vs = 5 volts I load = 1mA	-	26		lt ster Ω
	008 -	Vp = 0 volts Vs = 9 volts I load = 1mA	A FIREQUIA	16	HOTIW	Ω
T <sub>C</sub> (P2)	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P2	Vp = 0 volts Vs = 3 volts I load = 1mA	\$ 0.00 EX		JAN K	%/°C
IL(PS)	LEAKAGE CURRENT (VP to Vs)	V <sub>S</sub> = 3 volts I load = 10mA		0.01	20	M ent 3 310
90 MOI	SHIP A SA ST HOTTWIS SONATSING	@ T <sub>A</sub> = 85°C	A 19 HO	35	MATER	25,40
I <sub>L</sub> (SP)	LEAKAGE CURRENT (Vs to Vp)	Vp = 0 volts Vs = 3 volts I load = 1mA	OLTAGE T-1	0.01	50	- 001 nA
		@ T <sub>A</sub> = 85°C		120		
VO Pbar	OPEN DRAIN OUTPUT SATURATION VOLTAGES	V <sub>P</sub> = 5 volts V <sub>S</sub> = 3 volts I sink = 3.2mA I load = 0mA		85	400	mV
		@ T <sub>A</sub> = 85°C	-	120	/-	3
		Vp = 9 volts Vs = 3 volts I sink = 3.2mA I load = 0mA		50		mV
		Vp = 12 volts Vs = 3 volts I sink = 3.2mA I load = 0mA		40		mV
Vo Sbar	0 2 4 0 HAPUT VOLTAGE IIS	Vp = 0 volts Vs = 3 volts 1 sink = 3.2mA 1 load = 0mA	SF E	150	400	mV
		@ T <sub>A</sub> = 85°C	-	210	-	
		Vp = 0 volts Vs = 5 volts I sink = 3.2mA I load = 0mA	_	85	-	mV
		Vp = 0 volts V <sub>S</sub> = 9 volts I sink = 3.2mA I load = 0mA		50	-	mV

SYMBOL	XAM PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>L</sub> Pbar	OUTPUT LEAKAGE CURRENTS	V <sub>P</sub> = 0 volts V <sub>S</sub> = 15 volts	SOMY	RESIS	SWITCH	Pds(on)Pg
	OF Pbar AND Sbar	I load = 0mA beat	-	50	500	nA
	- 39 - 1	@ T <sub>A</sub> = 85°C	-	900	-	
IL Sbar	- 85 -	Vp = 15 volts Vs = 0 volts I load = 0mA	_	50	500	nA
		@ T <sub>A</sub> = 85°C	-	900	-	
V <sub>P</sub> - V <sub>S</sub>	SWITCHOVER UNCERTAINTY FOR COMPLETE SWITCHING OF INPUTS AND OPEN DRAIN OUTPUTS.	V <sub>S</sub> = 3 volts I sink = 3.2mA I load = 0mA	OOEFFICE SIGTANCE	5	50	mV T

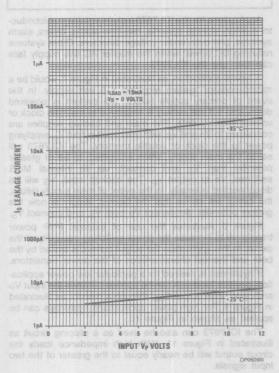
NOTE 2. The minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

# TYPICAL PERFORMANCE CHARACTERISTICS

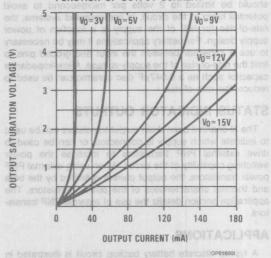


# SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE 1 9000 ICROAMPERES) 0.8 0.6 2 CURRENT 0.4 SUPPLY -40°C 0.2 +25°C +85°C 0 2 4 6 8 10 12 14 16 SUPPLY VOLTAGE (V)

IS LEAKAGE CURRENT VP to VS AS A FUNCTION OF INPUT VOLTAGE



Pbar OR Sbar SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



# DETAILED DESCRIPTION

As shown in the functional diagram (Figure 1), the ICL7673 includes a comparator which senses the input voltages VP and Vs. The output of the comparator drives the first inverter and the open-drain N-channel transistor Pbar. The first inverter drives a large P-channel switch, P1, a second inverter, and another open-drain N-channel transistor, Shar. The second inverter drives another large Pchannel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-beforemake switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs VP and VS must not be allowed to float, and, the difference in the two supplies must be greater than 50 millivolts. The leakage current through the reverse biased parasitic diode of switch P2 is very low.

#### **OUTPUT VOLTAGE**

The output operating voltage range is 2.5 to 15 volts. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V<sub>0</sub>. The ON-resistance of the P-channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5 volts, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50 microseconds.

#### INPUT VOLTAGE

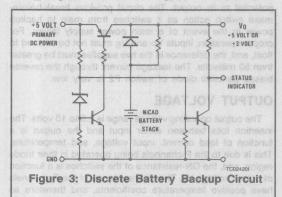
The input operating voltage range for Vp or Vs is 2.5 to 15 volts. The input supply voltage (Vp or Vs) slew rate should be limited to 2 volts per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a  $0.047\mu F$  disc ceramic can be used to reduce the rate-of-rise.

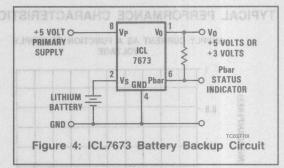
#### STATUS INDICATOR OUTPUTS

The N-channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

#### **APPLICATIONS**

A typical discrete battery backup circuit is illustrated in Figure 3. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 4, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 5. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663 micropower voltage regulator as shown in Figure 6.





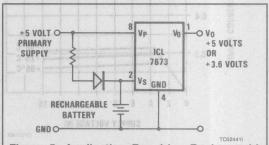


Figure 5: Application Requiring Rechargeable Battery Backup

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

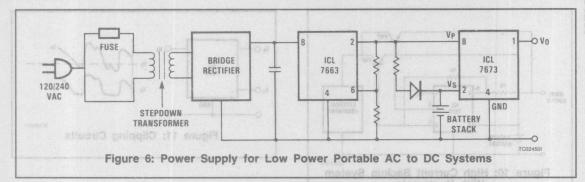
A typical application, as illustrated in Figure 7, would be a microprocessor system requiring a 5 volt supply. In the event of primary supply failure, the system is powered down, and a 3 volt battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to Vp and Vs, with the circuit output Vo supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than Vs and connect, via its internal MOS switches, Vp to output Vo. The backup input, Vs will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect Vp from Vo, and connect Vs.

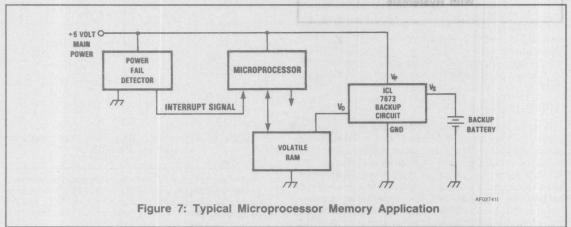
Figure 8 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

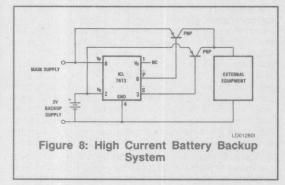
If hysteresis is desired for a particular low power application, positive feedback can be applied between the input  $V_{p}$  and open drain output  $S_{bar}$  through a resistor as illustrated in Figure 9. For high power applications hysteresis can be applied as shown in Figure 10.

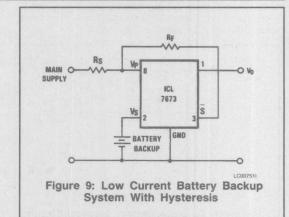
The ICL7673 can also be used as a clipping circuit as illustrated in Figure 11. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

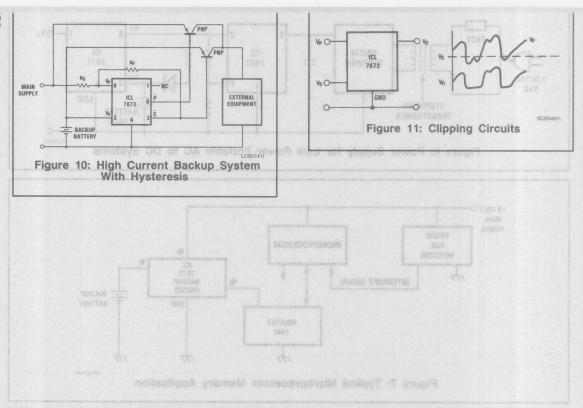
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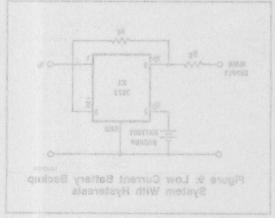


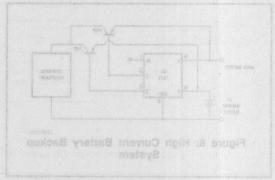












### ICL8013 Four Quadrant **Analog Multiplier**

#### GENERAL DESCRIPTION

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and and Square Root Functions feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment. frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.



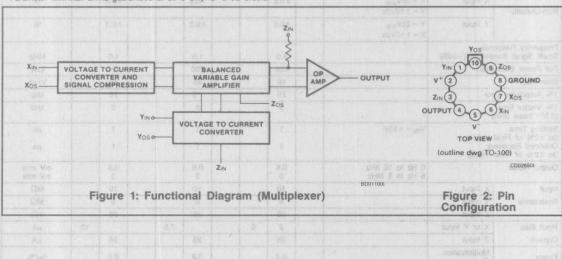
# FEATURES (1 stov) notice of several

- Accuracy of ±0.5% ("A" Version)
- Full ±10V Input Voltage Range
- 1MHz Bandwidth
- Uses Standard ±15V Supplies
- Built-in Op Amp Provides Level Shifting, Division

#### ORDERING INFORMATION

PART NUMBER	MULTIPLICATION ERROR	TEMPERATURE PACKAGE
ICL8013AM TZ ICL8013BM TZ ICL8013CM TZ ICL8013AC TZ	±0.5% ±1% MAX ±2% ±5%	-55°C to +125°C -55°C to +125°C -55°C to +125°C 10-LEAD 0°C to +70°C TO-100
ICL8013BC TZ ICL8013CC TZ ICL8013/D	±1% MAX ±2% ±2% TYP	0°C to +70°C 0°C to +70°C

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



### ICL8013



#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage±18V	Or
Power Dissipation (Note 1)500mW	
Input Voltages	
(XIN, YIN, ZIN, XOS, YOS, ZOS)VSLIPPLY	St

Operating Temperature Range:			
ICL8013XC	000	C to	+70°C
ICL8013XM55	5°C	to	+125°C
Storage Temperature Range65	5°C	to	+150°C
Lead Temperature (Soldering, 10sec)	00.		300°C

NOTE 1: Derate at 6.8mW/°C for operation at ambient temperature above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified T<sub>A</sub> = 25°C, V<sub>SUPPLY</sub> = ±15V, Gain and Offset Potentiometers Externally Trimmed)

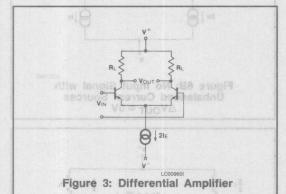
PARAMETER			10	L8013	A	IC	ICL8013B			CL8013	g noranut are	
		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Multiplier Function	n BDANDAS	EMPERATURE RANGE		XY 10	101	CATE	XY 10	Jal		XY 10	21.5	
Multiplication Erro	or	-10 < X < 10 -10 < Y < 10			0.5			1.0		2.0*	2.0	% Full Scale
Divider Function	10-LEAD	8°C (e + 128°C 8°C te + 128°C		10Z X			10Z X	229		10Z X	ZT 93	MCLSSTAD OLSSTAD OLSSTAD
Division Error		X = -10 X = -1		0.3			0.3	in aft		0.3 1.5	\$T 0	% Full Scale % Full Scale
Feedthrough	**soid	$X = 0 Y = 20V_{p-p} f = 50Hz$ $Y = 0 X = 20V_{p-p} f = 50Hz$			50 50		99	100		200* 150*	200	mV <sub>p-p</sub>
Non-Linearity	X Input	$X = 20V_{p-p}$ $Y = \pm 10Vdc$		±0.5	Elebio	SQNOL NO	±0.5	Jan III	Ecolotina economica	±0.8	75.7 K61	%
	Y Input	$Y = 20V_{p-p}$ $X = \pm 10Vdc$		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (-3dB)				1.0			1.0			1.0		MHz
Full Power Band	width		an Ir	750			750		THEST	750	PRATE	kHz
Slew Rate	(E) 14	TUSTINO	MAL	45	- 0	SERVICE OF	45		NOIS	45	O LAMO	V/μs
1% Amplitude E	rror (1)		1	75	and with the same		75	mest	-	75		kHz
1% Vector Error (0.5° Chase Shif		0		5	contractors of		5	7_	awY.	5		kHz
Settling Time (to ±2% of Final Value) Overload Recovery (to ±2% of Final Value)		V <sub>IN</sub> = ±10V		1	J DESTRUCTION OF THE PARTY OF T	uT#SVA	1		a 2007	1		μs μs
Output Noise		5 Hz to 10 kHz 5 Hz to 5 MHz		0.6		Zigi	0.6			0.6		mV rms mV rms
Input	X Input	E-WINCOM		10	des		10		1	10		МΩ
Resistance	Y Input		101102	6	11) 275	a spilling	6	SULPH		6		MΩ
116/15	Z Input		i sano tenga	36			36	or mal years	mark for many	-36	Action to the same	kΩ
Input Bias	X or Y Input			2	5			7.5			10	μΑ
Current	Z Input			25			25			25		μΑ
Power	Multiplication Error			0.2			0.2			0.2		%/%
Supply	Output Offset		The same		50			75			100	mV/V
Variation	Scale Factor		MARKET !	0.1			0.1	METER STATE		0.1		%1%
Quiescent Currer	nt			3.5	6.0		3.5	6.0	35,153	3.5	6.0	mA

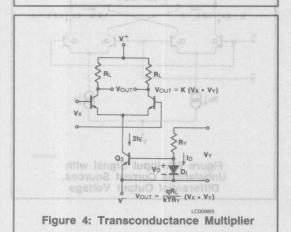
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#### **ELECTRICAL CHARACTERISTICS (CONT.)**

liposio religitium beorgaled a er		ICLOUISA		ICL8013B			ICL8013C					
PARA	METER	TEST CONDITIONS	MIN	MIN TYP MA		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
THE FOLLOV	WING SPECIFIC	ATIONS APPLY OVER	THE C	PERA	TING	TEMPI	ERATU	RE RA	ANGES	-		
Multiplication Error	İ	-10V < X <sub>IN</sub> < 10V, -10V < Y <sub>IN</sub> < 10V		1.5			2	The	20 x	3		% Full Scale
Average	Accuracy	1 1 1 3	3.5 31	0.06			0.06			0.06		%/°C
Temperature	Output Offset			0.2			0.2	CH4		0.2	4.6	mV/°C
Coefficients	Scale Factor	40-7-22-9		0.04			0.04	27 1 (27)		0.04	14.5	%/°C
Input Bias	X or Y Input	- 14 Marie 11 A			5		100	5			10	μΑ
Current	Z Input				25			25			35	μΑ
Input Voltage ()	X, Y, or Z)	10 94 T	TES		±10			±10		Maria.	±10	V
Output Voltage Swing		$R_L \ge 2k\Omega$ $C_L < 1000pF$	y	±10	12	rinna.	±10	16(0) ( (5)(8/1/2) (	n ni	±10	Inti-	V F governilit

\*Dice only





#### **DETAILED DESCRIPTION**

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 3.

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$
 Substituting  $r_e = \frac{1}{g_m} = \frac{kT}{ql_E}$  
$$V_{OUT} = V_{IN} \frac{R_L}{r_e} = V_{IN} \cdot \frac{ql_E R_L}{kT}$$

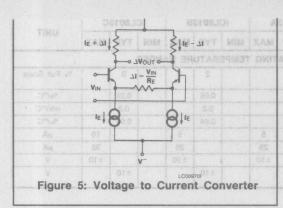
The output voltage is thus proportional to the product of the input voltage  $V_{IN}$  and the emitter current  $I_E$ . In the simple transconductance multiplier of Figure 4, a current source comprising  $Q_3$ ,  $D_1$ , and  $R_Y$  is used. If  $V_Y$  is large compared with the drop across  $D_1$ , then

$$I_D \simeq \frac{V_Y}{R_Y} = 2I_E$$
 and  $V_{OUT} = \frac{qR_L}{kTR_Y} (V_X \cdot V_Y)$ 

There are several difficulties with this simple modulator:

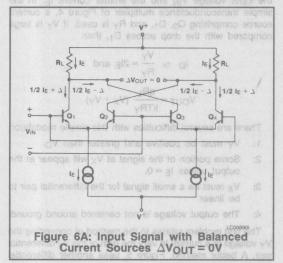
- 1: Vy must be positive and greater than VD.
- Some portion of the signal at V<sub>X</sub> will appear at the output unless I<sub>E</sub> = 0.
- V<sub>X</sub> must be a small signal for the differential pair to be linear.
- 4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V<sub>Y</sub> voltage to a current to vary the gain of the V<sub>X</sub> differential pair. A better method, Figure 5, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to  $\pm\,10$  volts with excellent linearity.



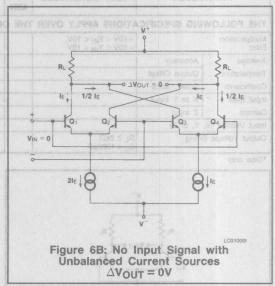
The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 6A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

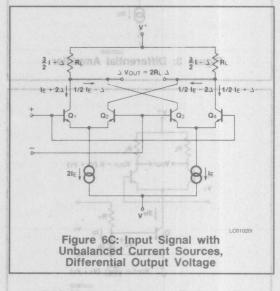
This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 6A of exactly equal current sources biasing the two pairs. With a small positive signal at V<sub>IN</sub>, the collector current of Q<sub>1</sub> and Q<sub>4</sub> will increase but the collector currents of Q<sub>2</sub> and Q<sub>3</sub> will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V<sub>IN</sub> input voltage.



In Figure 6B, notice that with  $V_{IN}=0$  any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 6C we apply a differential input voltage with unbalanced current sources. If  $I_{E1}$  is twice  $I_{E2}$ , the gain of differential pair  $Q_1$  and  $Q_2$  is twice the gain of pair  $Q_3$  and  $Q_4$ . Therefore, the change in cross coupled collector currents will be unequal and a

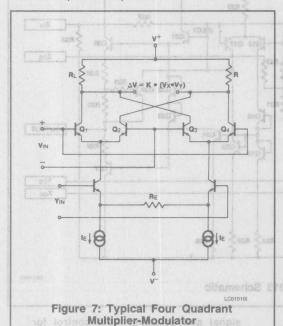
capable of four quadrant operation (Figure 7).

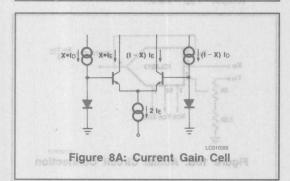




5-66

This circuit of Figure 7 still has the problem that the input voltage  $V_{\rm IN}$  must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.





If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias ourrent, the overall freedback forces the modulator output current to equal the current protects.

Therefore 
$$10 = X_{IM}^{-1}Y_{IM} = \frac{Z_{IM}}{R} = 10Z_{IM}$$
  
Since  $Y_{IM} = E_{OUT}$ ,  $E_{OUT} = \frac{10Z_{IM}}{X_{IM}}$ 

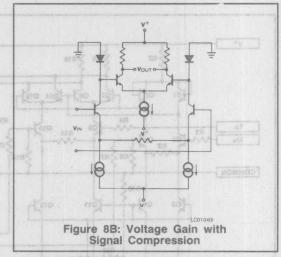


Figure 5 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 8A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 8A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 5, we have Figure 8B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

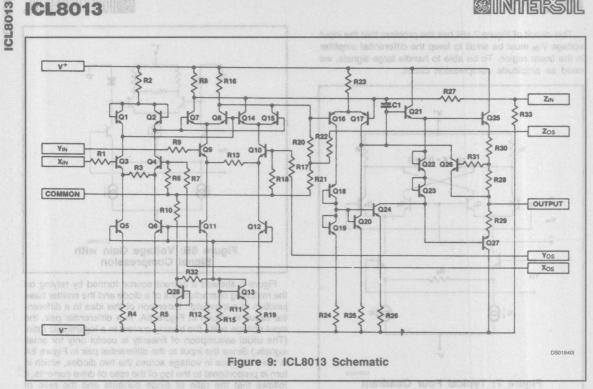
The complete schematic is shown in Figure 9. The differential pair  $Q_3$  and  $Q_4$  form a voltage to current converter whose output is compressed in collector diodes  $Q_1$  and  $Q_2$ . These diodes drive the balanced cross-coupled differential amplifier  $Q_7/Q_8$   $Q_{14}/Q_{15}$ . The gain of these amplifiers is modulated by the voltage to current converter  $Q_9$  and  $Q_{10}$ . Transistors  $Q_5$ ,  $Q_6$ ,  $Q_{11}$ , and  $Q_{12}$  are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors  $Q_{16}$  through  $Q_{27}$ .

or triangle) to Y<sub>IM</sub> with X<sub>IM</sub> = 0V, and adjust X<sub>OS</sub> minimum output.

Apply the aweep signal of Step 2 to X<sub>IM</sub> Y<sub>IM</sub> = 0V and adjust Y<sub>OS</sub> for minimum Output

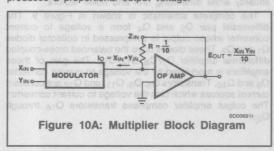
Multiplier Trimming Procedure

With  $X_{[N]}$  = 10.0V DC and the sweep signal of Step 2 applied to  $Y_{[N]}$  adjust the Gain potentiometer for Output =  $Y_{[N]}$ . This is easily accomplished with a differential acops plug-in (A + E) by inventing one



#### MULTIPLICATION

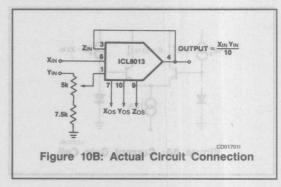
In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.



#### **Multiplier Trimming Procedure**

- 1. Set X<sub>IN</sub> = Y<sub>IN</sub> = 0V and adjust Z<sub>OS</sub> for zero Output.
- 2. Apply a ±10V low frequency (≤100Hz) sweep (sine or triangle) to YIN with XIN = 0V, and adjust XOS for minimum output.
- Apply the sweep signal of Step 2 to XIN with YIN = 0V and adjust YOS for minimum Output.
- 4. Readjust Zos as in Step 1, if necessary.
- 5. With XIN = 10.0V DC and the sweep signal of Step 2 applied to YIN, adjust the Gain potentiometer for Output = YIN. This is easily accomplished with a differential scope plug-in (A + B) by inverting one

signal and adjusting Gain control for  $(Output - Y_{IN}) = Zero.$ 

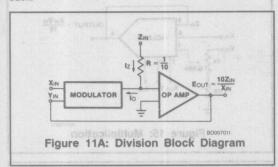


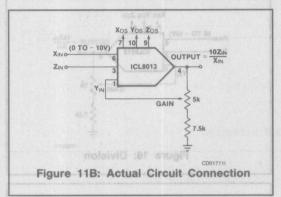
#### DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

Therefore 
$$I_O = X_{IN} \cdot Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{II}$$
  
Since  $Y_{IN} = E_{OUT}$ ,  $E_{OUT} = \frac{10Z_{IN}}{X_{IN}}$ 

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.



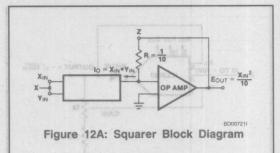


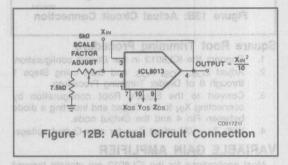
### **Divider Trimming Procedure**

- Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X<sub>OS</sub>, Y<sub>OS</sub>, Z<sub>OS</sub>) for zero volts.
- With Z<sub>IN</sub> = 0V, trim Z<sub>OS</sub> to hold the Output constant, as X<sub>IN</sub> is varied from -10V through -1V.
- 3. With  $Z_{IN} = 0V$  and  $X_{IN} = -10.0V$  adjust  $Y_{OS}$  for zero Output voltage.
- With Z<sub>IN</sub> = X<sub>IN</sub> (and/or Z<sub>IN</sub> = -X<sub>IN</sub>) adjust X<sub>OS</sub> for minimum worst-case variation of Output, as X<sub>IN</sub> is varied from −10V to −1V.
- Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
- 6. With  $Z_{\text{IN}} = X_{\text{IN}}$  (and/or  $Z_{\text{IN}} = -X_{\text{IN}}$ ) adjust the gain control until the output is the closest average around +10.0V (-10V for  $Z_{\text{IN}} = -X_{\text{IN}}$ ) as  $X_{\text{IN}}$  is varied from -10V to -3V.

#### SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since  $\cos^2 \omega t = 1/2$  (cos  $2\omega t + 1$ ).



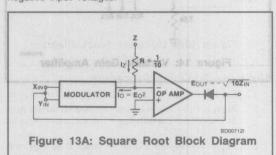


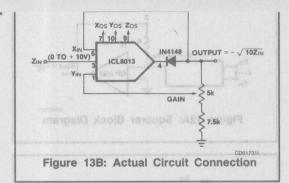
#### SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_0 = X_{IN}Y_{IN} = (-E_{OUT})^2 = 10Z_{IN}$$
  
 $E_{OUT} = -\sqrt{10Z_{IN}}$ 

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.



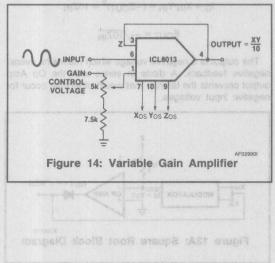


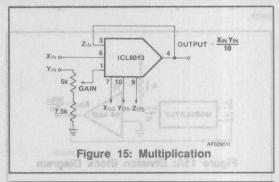
#### Square Root Trimming Procedure

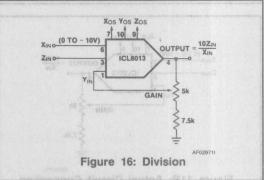
- 1. Connect the ICL8013 in the *Divider* configuration.
- Adjust Zos, Yos, Xos, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
- Convert to the Square Root configuration by connecting X<sub>IN</sub> to the Output and inserting a diode between Pin 4 and the Output node.
- 4. With ZIN = 0V adjust ZOS for zero Output voltage.

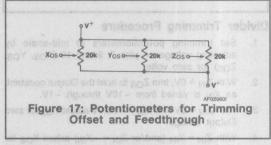
#### VARIABLE GAIN AMPLIFIER

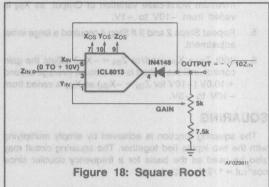
Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.







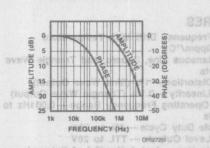


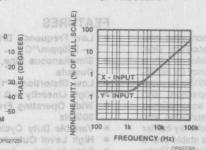


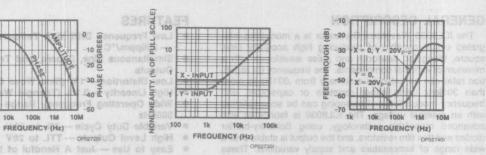
#### AMPLITUDE AND PHASE AS A **FUNCTION OF FREQUENCY**

#### NONLINEARITY AS A FUNCTION OF FREQUENCY

#### FEEDTHROUGH AS A FUNCTION OF FREQUENCY





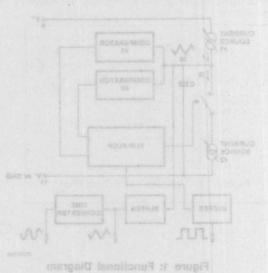


### DEFINITION OF TERMS Tupers atmanagement

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.



SALORO CACOTE (E

# ICL8038

### Precision Waveform Generator/Voltage Controlled Oscillator



FUNCTION OF FREDIENCY

#### GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

#### **FEATURES**

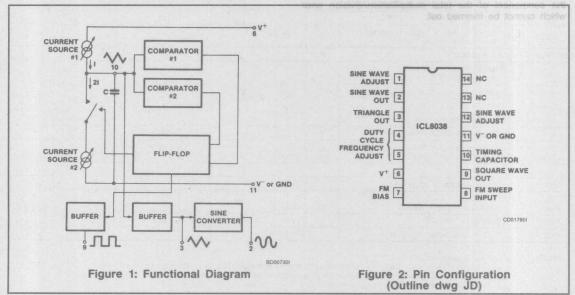
- Low Frequency Drift With Temperature
   250ppm/°C
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Low Distortion 1% (Sine Wave Output)
- High Linearity 0.1% (Triangle Wave Output)
   Wide Operating Frequency Range 0.001Hz to 300kHz
- Variable Duty Cycle 2% to 98%
- High Level Outputs TTL to 28V
- Easy to Use Just A Handful of External Components Required

#### ORDERING INFORMATION

PART NUMBER	STABILITY	TEMP. RANGE	PACKAGE
ICL8038CCJD	250ppm/°C typ	0°C to +70°C	CERDIP
ICL8038BCJD	180ppm/°C typ	0°C to +70°C	CERDIP
ICL8038ACJD	110ppm/°C typ	0°C to +70°C	CERDIP
ICL8038BMJD*	350ppm/°C max	-55°C to +125°C	CERDIP
ICL8038AMJD*	250ppm/°C max	-55°C to +125°C	CERDIP
ICL8038/D	Market - Ar English	es and business purch front	DICE**

<sup>\*</sup>Add /883B to part number if 883 processing is required.

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



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#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V <sup>-</sup> to V <sup>+</sup> )	Storage Temperature Range65°C to +150°C Operating Temperature Range:
Input Voltage (any pin)V- to V+	8038AM, 8038BM55°C to +125°C
Input Current (Pins 4 and 5)25mA	8038AC, 8038BC, 8038CC0°C to +70°C
Output Sink Current (Pins 3 and 9)25mA	Lead Temperature (Soldering, 10sec)300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

#### ELECTRICAL CHARACTERISTICS (V<sub>SUPPLY</sub> = ±10V or +20V, T<sub>A</sub> = 25°C, R<sub>L</sub> = 10kΩ, Test Circuit Unless Otherwise Specified)

6 460	33nE Gosed Wavelorm st.	4.78(2)	1 9	240F	. Challe			(8 e)	old) son	Fatt Tin	has esti	
Pm 9		1000	8038CC	18.1-	8038BC(BM)			8038AC(AM)			Duty Dye	
SYMBOL	GENERAL CHARACTERISTICS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	TINU 5)	
VSUPPLY TO	Supply Voltage Operating Range	\$2503		MOT	Statio				noinoteil	sinem	BH ISTOT	
Valender	Single Supply	+10	8 mig g	+30	+ 10	sido ed	30	e+ 10	ol bris	30	:89 Vovi	
V+, V-	Dual Supplies	±5	WEEP 3	±15	±5	E PARE	±15	±5	bluoris	±15	V	
ISUPPLY	Supply Current (V <sub>SUPPLY</sub> = ±10V) <sup>(2)</sup>				Ver i.	2 7,1990	5V 2 V8	10 ,V08	2 *V)	Vot is		
	8038AM, 8038BM VQ.5- of next VQ.5	of Of T	d arriox	yd an	partition of	12	15	tude is t	12	15	mA	
	8038AC, 8038BC, 8038CC		12	20		12	20	rgilled to	12	20	mA	
FREQUENCY C	HARACTERISTICS (all waveforms)						- 42	BARIET	30	HOIT	MITTER	
fmax	Maximum Frequency of Oscillation	100		most a	100	oruse l	sint or	100	TVoire	americ	kHz	
fsweep	Sweep Frequency of FM Input		10			10			10		kHz	
	Sweep FM Range <sup>(3)</sup>		35:1	en the	ired fr	35:1	SHIND	supply	35:1	marru!	ylogy	
nn	FM Linearity 10:1 Ratio		0.5	alners	o beat g	0.2	e ,ealy	ob odi e	0.2	of yequ	%	
Δf/ΔT	Frequency Drift With Temperature <sup>(5)</sup> 8038 AC, BC, CC 0°C to 70°C	All 8 7	250	eseupa	ads its	180	yonet	AM Mg pent er	110	neme:	ppm/°C	
	8038 AM, BM, -55°C to 125°C			Destru	15.00.21	dollar	350	tion of	in albrid	250	ppm/-C	
Δf/ΔV	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05	ncy to lying a	topest yd	0.05	o ed	ne rebo	0.05	Marian Superi	%/V	
DUTPUT CHAR	ACTERISTICS	1.6.18		daems	901,00	Despe	Joe no	0,107	s miq o	Rage 1	by gasay	
lolk	Square-Wave Leakage Current (V <sub>9</sub> = 30V)			1			1	DID THE	IIIW UL	1	μА	
VSAT	Saturation Voltage (ISINK = 2mA)		0.2	0.5	YJANUS	0.2	0.4	S (A3) 4	0.2	0.4	V	
t <sub>r was a</sub>	Rise Time (R <sub>L</sub> = $4.7k\Omega$ )		180	la Autori	suits mu	180	blueda v	- none	180		ns	
- t <sub>f</sub>	Fall Time (R <sub>L</sub> = $4.7k\Omega$ )		40	COURTE	end hard	40	av and	tions loss	40	tino ec	ns	
ΔD	Typical Duty Cycle Adjust (Note 6)	2		98	2		98	2		98	%	
VTRIANGLE	Triangle/Sawtooth/Ramp Amplitude (R <sub>TRI</sub> = 100kΩ)	0.30	0.33	elautilg	0.30	0.33	k-10-pe	0.30	0.33	Ampillo Lat th	xVsuppl	
	Linearity		0.1	to note	the colle	0.05	office to	cituo en	0.05	BoV a	%	
Zout	Output Impedance (IOUT = 5mA)		200	3 101 b	muesen	200		sut ai ro	200	f airtr	or Ω	
VSINE	Sine-Wave Amplitude (R <sub>SINE</sub> = 100k $\Omega$ )	0.2	0.22	9V92W 6	0.2	0.22	eráuper	0.2	0.22	10 3ms	XVSUPPL	
THD	THD $(R_S = 1M\Omega)^{(4)}$		2.0	5	PO 1 08	1.5	3	of 960 h	711.0	1.5	011%	
THD	THD Adjusted (Use Figure 6)		1.5	The second		1.0			0.8		%	

NOTES: 2. RA and RB currents not included.

3.  $V_{SUPPLY} = 20V$ ;  $R_A$  and  $R_B = 10k\Omega$ ,  $f \cong 10kHz$  nominal; can be extended 1000 to 1. See Figures 7a and 7b.

4. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R<sub>A</sub> and R<sub>B</sub>.)
5. Figure 3, pins 7 and 8 connected, V<sub>SUPPLY</sub> = ±10V. See Typical Curves for T.C. vs V<sub>SUPPLY</sub>.

PAR	AMETER	RA	RB	RL	C <sub>1</sub>	SW <sub>1</sub>	MEASURE
Supply Current		10kΩ 08	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6 10 / 1001
Sweep FM Range <sup>(1)</sup>	0388C, 8036CC	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with	Supply Voltage(2)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude:	Sine	10kΩ	10kΩ	10kΩ	,3.3nF	Closed	Pk-Pk output at Pin 2
(Note 4)	Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off	)(3)	10kΩ	10kΩ	THE VENTER	3.3nF	Closed	Current into Pin 9
Saturation Voltage (d	on) <sup>(3)</sup>	10kΩ	10kΩ		3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times	(Note 5)	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust;	MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
(Note 5)	MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform L	inearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTES: 1. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (fhi) and then connecting pin 8 to pin 6 (fin). Otherwise apply Sweep Voltage at pin 8 (2/3 V<sub>SUPPLY</sub> +2V)  $\leq$  V<sub>SWEEP</sub>  $\leq$  V<sub>SUPPLY</sub> where V<sub>SUPPLY</sub> is the total supply voltage. In Figure 7b, pin 8 should vary between 5.3V and 10V with respect to ground.  $10V \leq V^+ \leq 30V$ , or  $\pm 5V \leq$  V<sub>SUPPLY</sub>  $\leq \pm 15V$ .

3. Oscillation can be halted by forcing pin 10 to +5 volts or -5 volts.

Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to -5.0V

5. Not tested; for design purposes only.

#### **DEFINITION OF TERMS:**

Supply Voltage (VSUPPLY). The total supply voltage from V+ to V-

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through RA and RB.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed. Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency

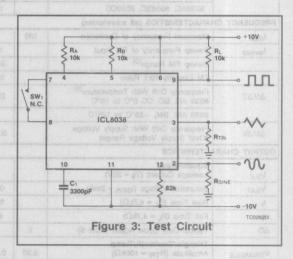
Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q23 when this transistor is turned on. It is measured for a sink current of 2mA.

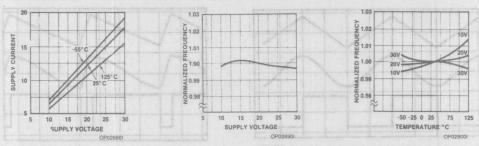
Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle

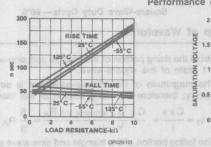
Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

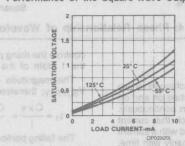


#### TYPICAL PERFORMANCE CHARACTERISTICS

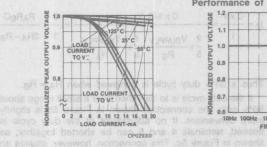


#### Performance of the Square-Wave Output



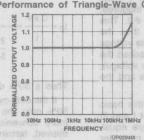


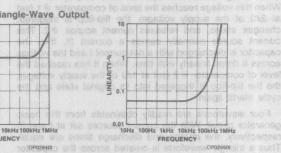
#### Performance of Triangle-Wave Output



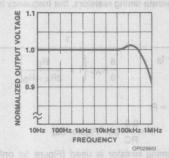
10/ DUTPUT

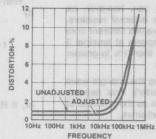
NORMALIZE

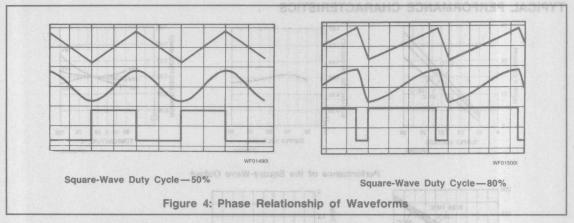




Square-Wave Duty Cycle

#### Performance of Sine-Wave Output and a second and a second and a second and a second and a second and a second and a second a second and 






# **DETAILED DESCRIPTION** (See Figure 1)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current 1, the voltage across the capacitor rises linearily with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

#### **WAVEFORM TIMING**

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 5. Best results are obtained by keeping the timing resistors R<sub>A</sub> and R<sub>B</sub> separate (a). R<sub>A</sub>

controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 VSUPPLY; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times \sqrt[1]{3} \times V_{SUPPLY} \times R_A}{\sqrt[1]{5} \times V_{SUPPLY}} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3 \text{ V}_{SUPPLY}}{\frac{2}{5} \times \frac{V_{SUPPLY}}{R_B} - \frac{1}{5} \times \frac{V_{SUPPLY}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50% duty cycle is achieved when RA = RB.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 5b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 5c. This connection, however, causes an inherently larger variation of the duty-cycle, frequency, etc.

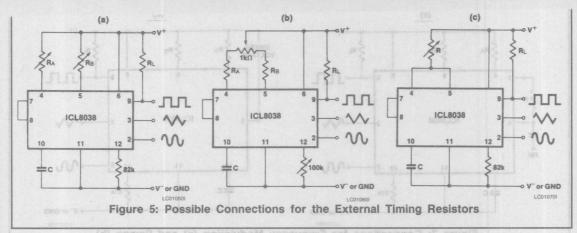
With two separate timing resistors, the frequency is given

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3}R_AC(1 + \frac{R_B}{2R_A - R_B})}$$
or, if  $R_A = R_B = R$ 

$$f = \frac{0.3}{RC}$$
 (for Figure 5a)

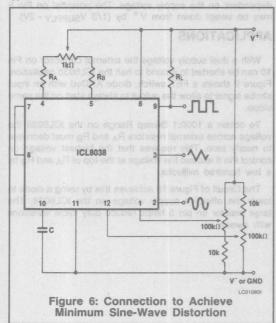
If a single timing resistor is used (Figure 5c only), the frequency is

$$f = \frac{0.18}{BC}$$



Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents and thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize sine-wave distortion the  $82k\Omega$  resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.



### SELECTING RA, RB and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than  $1\mu A$  are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of  $10\mu A$  to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to RA can be calculated from:

$$I = \frac{R_1 \times (V^+ - V^-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{(V^+ - V^-)}{5R_A}$$

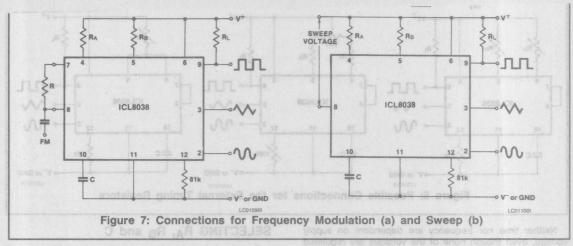
A similar calculation holds for RB.

The capacitor value should be chosen at the upper end of its possible range.

# WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V<sup>+</sup> and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

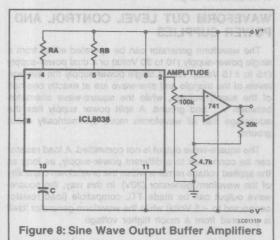
The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.



# FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V  $^+$ ). By altering this voltage, frequency modulation is performed. For small deviations (e.g.  $\pm 10\%$ ) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 7a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about  $8k\Omega$  (pins 7 and 8 connected together), to about  $(R+8k\Omega)$ .

The sine wave output has a relatively high output impedance (1k $\Omega$  Typ). The circuit of Figure 8 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.



For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 7b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at  $V_{sweep} = 0$ ). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V + by (1/3  $V_{SUPPLY} - 2V$ ).

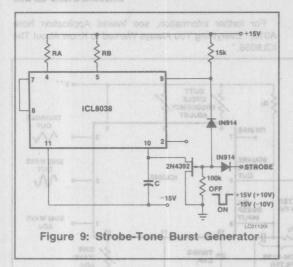
#### **APPLICATIONS**

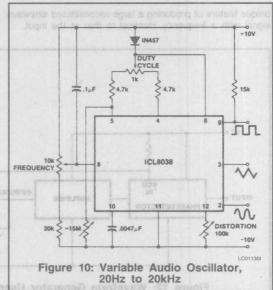
With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 9 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

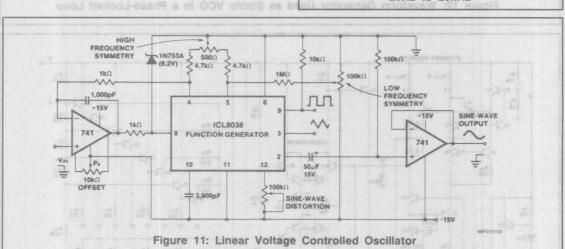
To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors  $R_A$  and  $R_B$  must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of  $R_A$  and  $R_B$  by a few hundred millivolts.

The Circuit of Figure 10 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

5-78







The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 11.

#### USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop as shown in Figure 12. In this application the remaining functional blocks, the phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC4344, NE562, HA2800, HA2820)

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input

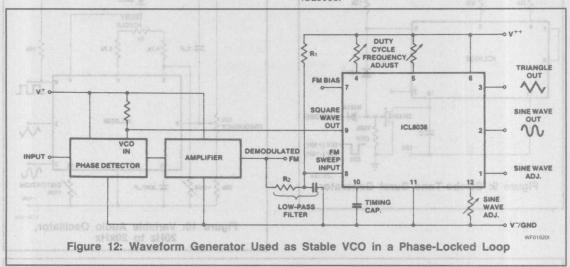
voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

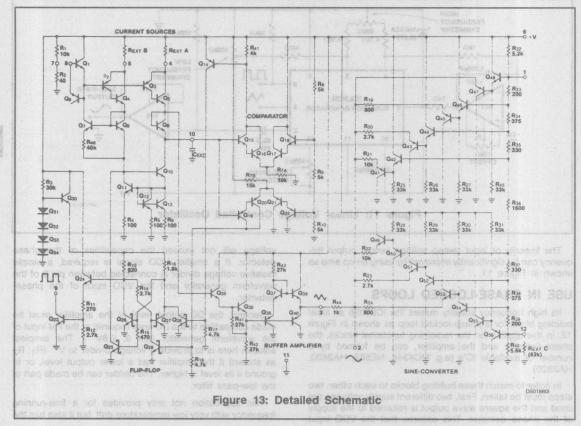
Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V  $^+$ ). The simplest solution here is to provide a voltage divider to V  $^+$  (R<sub>1</sub>, R<sub>2</sub> as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the

unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note A013, "Everything You Always Wanted to Know About The ICL8038."





#### GENERAL DESCRIPTION

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50 µA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

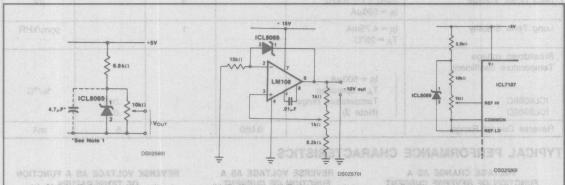
#### **FEATURES**

- Temperature Coefficient Guaranteed to 25ppm/°C Max
- Low Bias Current 50μA Min
- Low Dynamic Impedance
- Low Reverse Voltage Low Cost

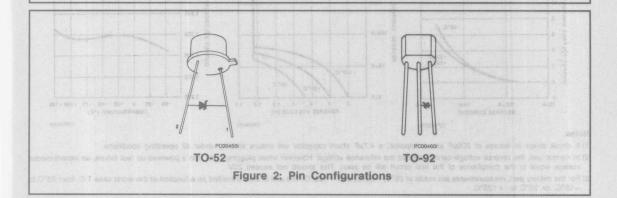
#### ORDERING INFORMATION

ORDER P/N TO-92	ORDER P/N TO-52	TEMPERATURE	MAX. TEMP. COEFF OF VREF
ICL8069CCZR	ICL8069CCSQ	0°C to +70°C	0.005%/°C
	ICL8069CMSQ	-55°C to +125°C	0.005%/°C
ICL8089DCZR	ICL8069DCSQ	0°C to +70°C	0.01%/°C
	ICL8069DMSQ	-55°C to +125°C	0.01%/°C
ICL8069/D			DICE**

\*\*Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



- (a) Simple Reference (1.2 volts or
- (b) Buffered 10V Reference using a
- (c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit. single supply. Figure 1: Functional Diagrams



Reverse VoltageSee Note 2	Sto
Forward Current	Ope
Reverse Current	908
Power Dissipation Limited by max forward/	
reverse current	Lea

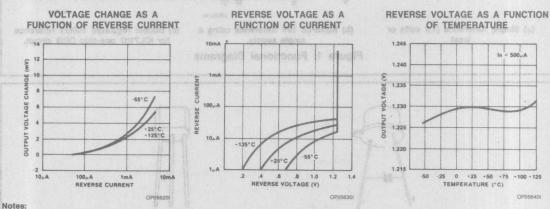
Storage Temperature65°C to +150°C
Operating Temperature
ICL8069C
ICL8069M55°C to +125°C
Lead Temperature (Soldering, 10sec)300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

#### ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)

CHARACTERISTICS	TEST CONDITIONS	MIN MA	TYP	MAX	UNITS
Reverse breakdown Voltage	I <sub>R</sub> = 500μA	1.20	1.23	1.25	V
Reverse breakdown Voltage change	50μA ≤ I <sub>R</sub> ≤ 5mA	OSAK	15	20	mV
Reverse dynamic impedance	I <sub>R</sub> = 50μA I <sub>R</sub> = 500μA	DANGO	0808.3	2 2	Ω
Forward Voltage Drop	I <sub>F</sub> = 500μA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I <sub>R</sub> = 500μA	SISDING SHOWS	.5	THE RESERVE AND THE AREA	μV
Long Term Stability	I <sub>R</sub> = 4.75mA T <sub>A</sub> = 25°C	gine con	1		ppm/kHR
Breakdown voltage Temperature coefficient ICL8069C ICL8069D	I <sub>R</sub> = 500μA T <sub>A</sub> = operating Temperature range (Note 3)	mar mar		.005	%/°C
Reverse Current Range	SPE	0.050	Aug/M	5	mA

#### TYPICAL PERFORMANCE CHARACTERISTICS



- 1) If circuit strays in excess of 200pF are anticipated, a 4.7 µF shunt capacitor will ensure stability under all operating conditions.
- 2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
- 3) For the military part, measurements are made at 25°C, -55°C, and +125°C. The unit is then classified as a function of the worst case T.C. from 25°C to -55°C, or 25°C to +125°C.

5

The Intersil ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE	PACKAGE				
ICL8211CPA ICL8211CBA	0°C to +70°C 0°C to +70°C	8 lead Mini DIP 8 lead SOIC				
ICL8211CTY ICL8211MTY*	0°C to + 70°C -55°C to + 125°C	TO-99 Can TO-99 Can				
ICL8212CPA ICL8212CBA	0°C to +70°C 0°C to +70°C	8 lead Mini DIP 8 lead SOIC				
ICL8212CTY	0°C to +70°C	TO-99 Can				
ICL8212MTY*	-55°C to +125°C	TO-99 Can DICE **				
ICL8212/D	88 -08	DICE **				

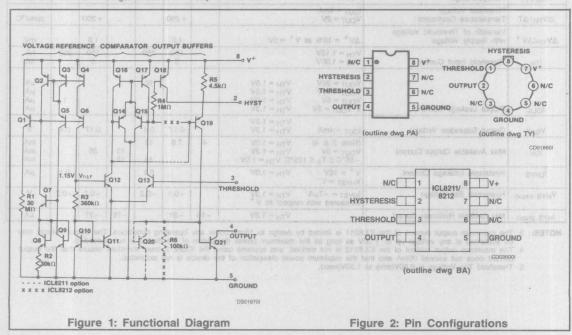
<sup>\*</sup> Add /883B to part number if 883B processing is required.

#### CHAIUMED

- High Accuracy Voltage Sensing and Generation: Internal Reference 1.15 Volts Typical
- Low Sensitivity to Supply Voltage and Temperature Variations
- Wide Supply Voltage Range: Typ. 1.8 to 30 Volts
- Essentially Constant Supply Current Over Full Supply Voltage Range
- Easy to Set Hysteresis Voltage Range
- Defined Output Current Limit ICL8211
   High Output Current Capability ICL8212

#### **APPLICATIONS**

- Low Voltage Sensor/Indicator
- High Voltage Sensor/Indicator
- Non Volatile Out-of-Voltage Range Sensor/ Indicator
- Programmable Voltage Reference or Zener Diode
- Series or Shunt Power Supply Regulator
- Fixed Value Constant Current Source



<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

### ICL8211/ICL8212

# **OINTERSIL**

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage0.5 to +30 volts
Output Voltage0.5 to +30 volts
Hysteresis Voltage+0.5 to -10 volts
Threshold Input Voltage
+30 to -5 volts with respect to GROUND and +0
to -30 volts with respect to V+

Current into Any Terminal ......±30mA

Power Dissipation (Note 1 & 2)	300mW
Operating Temperature Range:	THE THURSDAY
ICL8211M/8212M	
ICL8211C/8212C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/8212MTY products. Derate linearly at -10mW/°C for ambient temperatures above 100°C.

NOTE 2: Derate linearly above 50°C by -10mW/°C for ICL8211C/8212C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

#### **ELECTRICAL CHARACTERISTICS** (V + = 5V, T<sub>A</sub> = 25°C unless otherwise specified)

SYMBOL	en edura denotation en	lid v son * rotsoligt		ICL8211			ICL8212		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
1+	Supply Current	2.0 < V <sup>+</sup> < 30 V <sub>T</sub> = 1.3V V <sub>T</sub> = 0.9V	10 50	22 140	40 250	50 10	110 20	250 40	μA μA
V <sub>TH</sub>	Threshold Trip Voltage	V + 5V I <sub>OUT</sub> = 4mA V + 2V V <sub>OUT</sub> = 2V V + 30V	0.98	1.15 1.145 1.165	1.19 1.19 1.20	1.00 1.00 1.05	1.15 1.145 1.165	1.19 1.19 1.20	V V V
V <sub>THP</sub>	Threshold Voltage Disparity Between Output & Hysteresis Output	$I_{OUT} = 4mA$ $V_{OUT} = 2V$ $I_{HYST} = 7\mu A$ $V_{HYST} = 3V$	tips/ 6	-8.0	+ 70°C	01 0	-0.5	ABC	mV
VSUPPLY	Guaranteed Operating Supply Voltage Range (Note 5)	+25°C 0 to +70°C -55°C to +125°C	2.0 2.2 2.8		30 30 30	2.0 2.2 2.8		30 30 30	V V V
VSUPPLY	Typical Operating Supply Voltage Range	+25°C +125°C -55°C	1.4	oniana orașiu	30 30 30	1.8 1.4 2.5	man hi mid xal	30 30 30	V V
ΔV <sub>TH</sub> /ΔT	Threshold Voltage Temperature Coefficient	I <sub>OUT</sub> = 4mA V <sub>OUT</sub> = 2V		+ 200	La contra de la contra del la contra del la contra del la contra del la contra de la contra del la contra		+ 200		ppm/s
ΔV <sub>TH</sub> /ΔV +	Variation of Threshold Voltage with Supply Voltage	$\Delta V^{+} = 10\%$ at $V^{+} = 5V$		1.0			1.0		mV
ITH	Threshold Input Current	V <sub>TH</sub> = 1.15V V <sub>TH</sub> = 1.00V		100	250		100	250	nA nA
lolk	Output Leakage Current	V <sub>OUT</sub> = 30V V <sub>TH</sub> = 1.0V V <sub>OUT</sub> = 30V V <sub>TH</sub> = 1.3V V <sub>OUT</sub> = 5V V <sub>TH</sub> = 1.0V V V <sub>OUT</sub> = 5V V <sub>TH</sub> = 1.3V	39.5		10		80	10	μΑ μΑ μΑ
VSAT	Output Saturation Voltage	V <sub>TH</sub> = 1.0V V <sub>TH</sub> = 1.3V	910	0.17	0.4	1	0.17	0.4	V
Іон	Max Available Output Current	(Note 3 & 4) V <sub>TH</sub> = 1.0V V <sub>OUT</sub> = 5V V <sub>TH</sub> = 1.3V −55°C ≤ T <sub>A</sub> ≤ 125°C V <sub>TH</sub> = 1.0V	4	7.0	12	15 12	35		mA mA mA
ILHYS	Hysteresis Leakage Current	V <sup>+</sup> = 10V V <sub>HYST</sub> = V <sup>-</sup> V <sub>TH</sub> = 1.0V			0,1	200	Link	0.1	μА
VHYS (max)	Hysteresis Sat Voltage	I <sub>HYST</sub> = -7μA V <sub>TH</sub> = 1.3V measured with respect to V <sup>+</sup>		-0.1	-0.2		-0.1	-0.2	V
IHYS (max)	Max Available Hysteresis Current	V <sub>TH</sub> = 1.3V	-15	-21		-15	-21		μΑ

NOTES: 3. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.

4. The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output

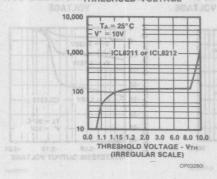
current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.

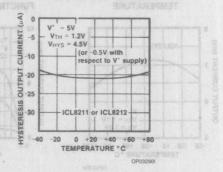
5. Threshold Trip Voltage is 0.80V(min) to 1.30V(max).

#### TYPICAL PERFORMANCE CHARACTERISTICS COMMON TO ICL8211 AND ICL8212

THRESHOLD INPUT CURRENT AS A FUNCTION OF HYS

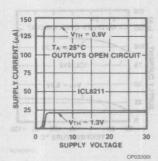
HYSTERESIS OUTPUT SATURATION CURRENT AS
A FUNCTION OF TEMPERATURE



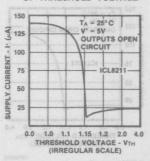


#### TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY

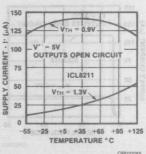
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



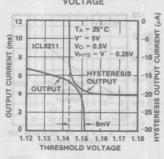
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



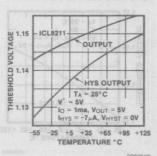
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



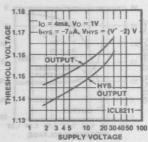
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

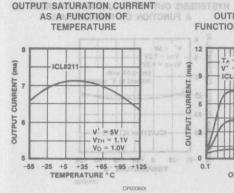


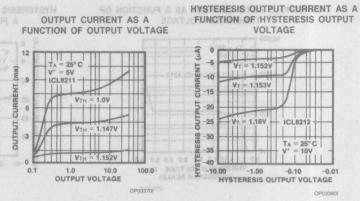
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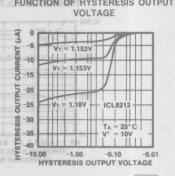
### ICL8211/ICL8212

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#### TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY (CONT.)

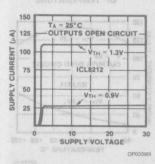




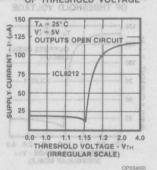


#### TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY

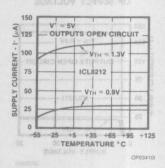
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



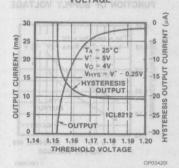
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



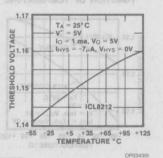
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



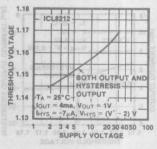
**OUTPUT SATURATION CURRENTS** AS A FUNCTION OF THRESHOLD VOLTAGE



THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A **FUNCTION OF TEMPERATURE** 

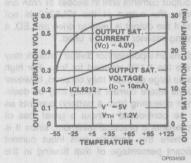


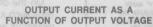
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A **FUNCTION OF SUPPLY VOLTAGE** 

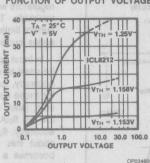


### TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY (CONT.)

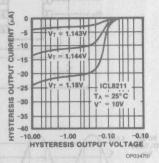
OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE







HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



#### **DETAILED DESCRIPTION**

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q<sub>1</sub> thru Q<sub>10</sub> and R<sub>1</sub>, R<sub>2</sub> and R<sub>3</sub> set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per °C).

Components  $Q_2$  thru  $Q_9$  and  $R_2$  make up a constant current source;  $Q_2$  and  $Q_3$  are identical and form a current mirror.  $Q_8$  has 7 times the emitter area of  $Q_9$ , and due to the current mirror, the collector currents of  $Q_8$  and  $Q_9$  are forced to be equal and it can be shown that the collector current in  $Q_8$  and  $Q_9$  is

I<sub>C</sub> (Q<sub>8</sub> or Q<sub>9</sub>) = 
$$\frac{1}{R_2} \times \frac{kT}{q} \ln 7$$
  
or approximately 1 $\mu$ A at 25°C

Where k = Boltzman's constant q = charge on an electron

and T = absolute temperature in °K

Transistors  $Q_5$ ,  $Q_6$ , and  $Q_7$  assure that the  $V_{CE}$  of  $Q_3$ ,  $Q_4$ , and  $Q_9$  remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of  $Q_1$  provides sufficient start up current for the constant source; there being two stable states for this type of circuit — either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

 $\mathrm{Q}_4$  is matched to  $\mathrm{Q}_3$  and  $\mathrm{Q}_2$ ;  $\mathrm{Q}_{10}$  is matched to  $\mathrm{Q}_9$ . Thus the I<sub>C</sub> and V<sub>BE</sub> of  $\mathrm{Q}_{10}$  are identical to that of  $\mathrm{Q}_9$  or  $\mathrm{Q}_8$ . To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of  $\mathrm{Q}_9$  to a voltage proportional to the difference of the base emitter voltages of two transistors  $\mathrm{Q}_8$  and  $\mathrm{Q}_9$  operating at two current densities.

Thus 1.15 = 
$$V_{BE}$$
 (Q<sub>9</sub> or Q<sub>10</sub>) +  $\frac{R_3}{R_2}$  x  $\frac{kT}{q}$  In 7 which provides  $\frac{R_3}{R_2 = 12}$  (approx.)

The total supply current consumed by the voltage reference section is approximately  $6\mu A$  at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors  $Q_{11}$  thru  $Q_{17}$ . The outputs from the comparator are limited to two diode drops less than V  $^+$  or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of  $Q_{19}$  to  $100\mu A$ .

In the case of the ICL8211,  $Q_{21}$  is proportioned to have 70 times the emitter area of  $Q_{20}$  thereby limiting the output current to approximately 7mA, whereas for the ICL8212 almost all the collector current of  $Q_{19}$  is available for base drive to  $Q_{21}$ , resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

#### **APPLICATIONS**

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

#### **General Information**

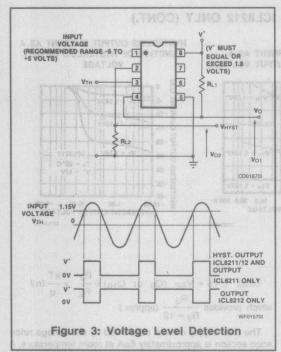
#### THRESHOLD INPUT CONSIDERATIONS

Although any voltage between -5V and V<sup>+</sup> may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6 volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

been limited to typically 7mA to permit direct drive of en

### ICL8211/ICL8212

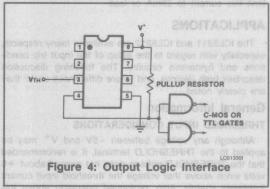




The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 3 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to  $10\mu A$  or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

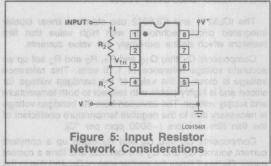


A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an

LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V<sub>TH</sub>. For high accuracy, currents as large as  $50\mu\text{A}$  may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as  $6\mu\text{A}$  may be considered without a great loss of accuracy.  $6\mu\text{A}$  represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.



Case 1. High accuracy required, current in resistor network unimportant Set I =  $50\mu A$  for  $V_{TH} = 1.15$  volts  $\therefore R_1 \rightarrow 20k\Omega$ .

Case 2. Good accuracy required, current in resistor network important Set I =  $7.5\mu A$  for  $V_{TH} = 1.15$  volts  $\therefore R_1 \rightarrow 150 k \Omega$ .

## SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection - no hysteresis

Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 7 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 8.

Conditions for correct operation of OUTPUT (terminal #4).

- 1. ICL8211 $1.8V \le V^+ \le 30V$
- 2. EICL8212 of a positive distance of the constant of the con

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications - refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 9.

The circuit (a) of Figure 9 requires that the full current flowing in the resistor network be sourced by the HYSTER-ESIS output, whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESH-OLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

#### **Practical Applications**

a) Low Voltage Battery Indicator

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The guiescent current taken by the system will be typically 35µA which will increase to 7mA when the lamp is turned on. R3 will provide hysteresis if required.

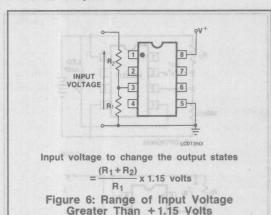
#### b) Non-Volatile Low Voltage Detector

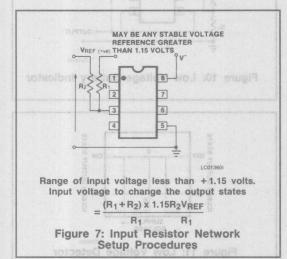
In this application the high trip voltage VTR2 is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S1 the operating point changes to B and will remain at B until the supply voltage drops below VTR1, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below VTR1 (even to zero volts) and then raised back to VNOM.

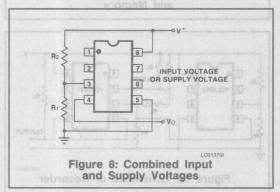
#### c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an out-of-operating range supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.





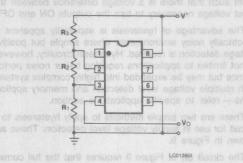


Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip

### ICL8211/ICL8212

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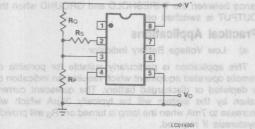


Harrier Low trip voltage of showler rotates with a privi

$$V_{TR1} = \left[ \frac{(R_1 + R_2 \times 1.15)}{R_1} + 0.1 \right]$$
 volts

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + RP\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$
High trip voltage

m the High trip voltage as 8 of separate mad prototed

value and amili double 
$$\frac{(R_P + R_Q)}{R_P} \times 1.15$$
 volts of the value and  $\frac{R_P + R_Q}{R_P} \times 1.15$  volts of the value and  $\frac{R_P}{R_P} = 1.00$ 

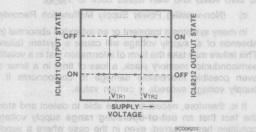


Figure 9: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

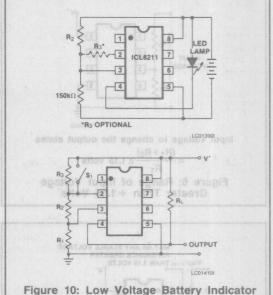
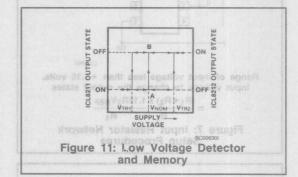
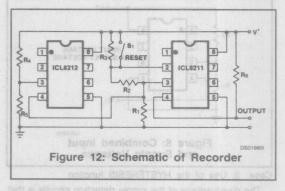


Figure 10: Low Voltage Battery Indicator





A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

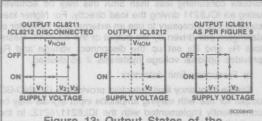


Figure 13: Output States of the ICL8211 and ICL8212 as a Function of the Supply Voltage

Referring to Figure 12, the ICL8212 is used to detect a voltage,  $V_2$ , which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range,  $V_1$ . Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range  $V_1$  to  $V_2$  by making  $V_3$ —the upper trip point of the ICL8211 much higher in voltage than  $V_2$ .

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above  $V_2$ . Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out  $R_3$  for values of supply voltage between  $V_1$  and  $V_2$ .

#### d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately  $25\mu A$  by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a  $130\mu A$  constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

#### e) Zener or Precision Voltage Reference

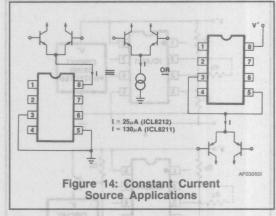
The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V<sub>Z</sub> output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

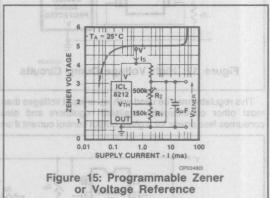
$$(V_{zener} = \frac{(R_1 + R_2)}{R_4} \times 1.15 \text{ volts}).$$

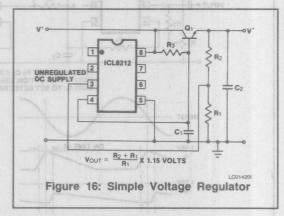
Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between  $300\mu A$  and 25mA will range from 4 to  $7\Omega$ . The knee is sharper and occurs at a significantly lower current than other similar devices available.







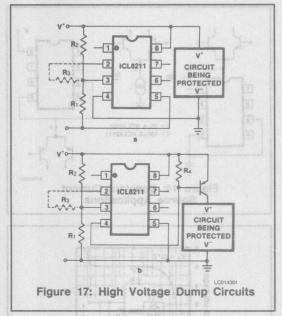


#### f) Precision Voltage Regulators

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R<sub>1</sub> and R<sub>2</sub>. Two capacitors C<sub>1</sub> and C<sub>2</sub> are required to ensure stability since the ICL8212 is uncompensated internally.

### ICL8211/ICL8212





This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than

any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

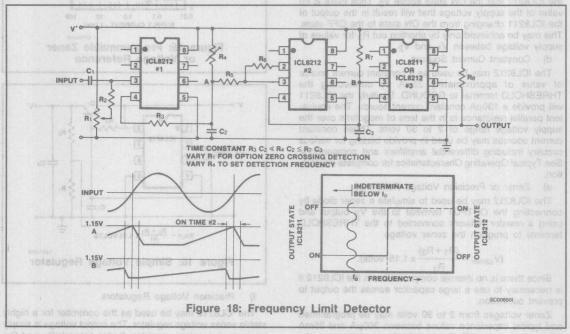
#### g) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R<sub>1</sub> and R<sub>2</sub> set up the disconnect voltage and R<sub>3</sub> provides optional voltage hysteresis if so desired.

#### h) Frequency limit detectors

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of  $\rm R_3,\,R_4$  and  $\rm C_2$  results in a slow output positive ramp. The negative range is much faster than the positive range.  $\rm R_5$  and  $\rm R_6$  provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge  $\rm C_3$ . The time constant of  $\rm R_7\,C_3$  is much greater than  $\rm R_4\,C_2$ . Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.



### ICL8211/ICL8212

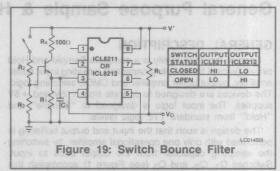
#### i) Switch bounce filter

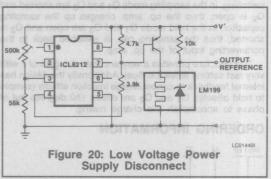
Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 19 provides a rapid charge up of C<sub>1</sub> to close to the positive supply voltage (V +) on a switch closure and a corresponding slow discharge of C1 on a switch break. By proportioning the time constant of R1 C1 to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/8212 will be a single transition of state per desired switch closure.

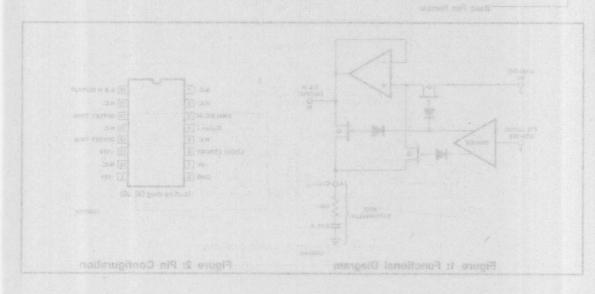
#### j) Low voltage power disconnector

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212" by D. Watson.







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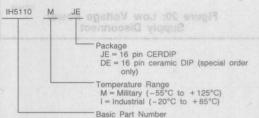
#### GENERAL DESCRIPTION

Each of the 5110 family is a complete Sample and Hold circuit, (except for sampling capacitor) including input buffer amplifier, output buffer amplifier and CMOS switching logic. The devices are designed to operate from ±15V and +5V supplies. The input logic is designed to "Sample" and "Hold" from standard TTL logic levels.

The design is such that the input and output buffering is performed with only one operational amplifier, by switching the sampling capacitor from the output back to input. Switches  $Q_1$ ,  $Q_2$ , and  $Q_3$  (see Figure 1) accomplish this switching. In the sampling mode  $Q_1$  and  $Q_3$  are shorted and  $Q_2$  is open; thus the op. amp. charges up the sampling capacitor. In the hold mode  $Q_1$  and  $Q_3$  are open and  $Q_2$  is shorted; thus the sampling cap. is switched back to the noninverting input of the op. amp.

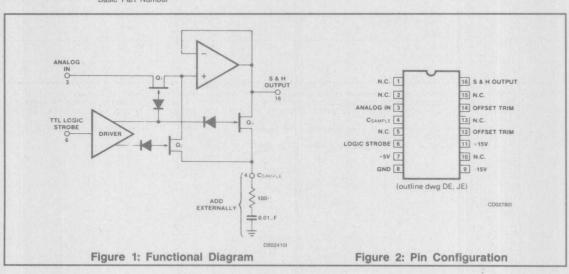
This structure provides a very accurate d.c. gain of 1 with very fast settling times (i.e.  $5\mu$ s). Additionally the design has internal feedback to cancel charge injection effects (sample to hold offsets).  $Q_1$  and  $Q_2$  are driven 180 degrees out of phase to accomplish this charge nulling.

#### ORDERING INFORMATION



### FEATURES was alog signis nam sides ava show bha

- . Low Cost
- Military and Industrial Temperature Ranges
- ± 10V Input Voltage Range
- 0.5mV/Sec Drift Typical @ C<sub>S</sub> = 0.01μF
- TTL and CMOS Compatible
- Short Circuit Protected
- Input Offset Voltage Adjustable to < 100μV Using A 20kΩ Potentiometer
- 0.1% Guaranteed Sample Accuracy With 10V Signals and C<sub>S</sub> = 0.01μF
- Sample to Hold Offset Is 5mV Max



### IH5110-IH5115

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#### ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range .....-65°C to 150°C Supply Voltages .....±16V Lead Temperature (Soldering, 10sec) ......300°C Power Dissipation .......500mW Operating Temperature ..... -25°C to 85°C -55°C to 125°C

#### ELECTRICAL CHARACTERISTICS (TA = 25°C, Pin 7 = 5V, Pin 8 = GND, Pin 9 = -15V, Pin 11 = 15V) Note 3

SYMBOL	HETEMOLTHATION S - BIT	THREE	IH511	0, 5112, 5114		IH5111, 5113,		5115	
	CHARACTERISTIC		MIN	ТҮР	MAX	MIN	TYP	MAX	UNIT
Close	Aperture Time		-	120			200		ns
tacq.	Acquisition Time for Max Analog Voltage Step $C_S = 0.1 \mu F$ (0.1% Accur.) $C_S = 0.01 \mu F$ (0.1% Accur.) See F	igure 5	ravgod :	25 4 4	35 6 6		25 4 4	35 6 6	μs
Vdrift) is sugree for	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	Figure 3	es polyab 2.4V.	0.3 0.5 2.0	5 000	Vino of te proside offi or look of	0.3 0.5 2.0	2.5 5 10	mV/s
Vinject	Charge Injection or Sample to Hold Offsets $ \begin{array}{ll} C_S = 0.1 \mu F \\ C_S = 0.01 \mu F \\ C_S = 0.001 \mu F \end{array} $ See Note 1 & Figure 4		Typical	< 1 < 1 12	5	ugnt appl	< 1 < 1 12	5 5 25	mVp-p
Vswitch	Switching Transients or Spikes (Duration Less than $2\mu$ s) $C_S = 0.1 \mu F$ $C_S = 0.01 \mu F$ $C_S = 0.001 \mu F$ See Figure 4			0.1 0.1 0.2	0.5 0.5 0.5		0.1 0.1 0.2	0.5 0.5 0.5	٧
V <sub>couple</sub>	A. C. Feedthrough Coupled to Output	dr	44	5			5		mVp-p
Voffset	D.C. Offset When in Sample Mode Trimmable	5110 5111	-	11001 3	40			40	
	to 0m V With Ext. 20kΩ Potentiometer  See Figure 3	5112 5113		- 28	10			10	mV
		5114 5115	- 1	100	5			5	
Rin	Input Impedance in Hold or Sample Mode (f ≤ 10Hz)			100			100		MΩ
l <sub>± 15V</sub>	Plus or Minus 15V Supply Quiescent Current	Transcore and the second	Year a journal province of	3.4	6		3.4	6	mA
I <sub>5V</sub>	5V Supply Quiescent Current	not onida	si englad	0.3	10	4	0.3	10	A
Vanalog	D.C. Input Voltage Range			-	±7.5	WAS DIE LE		±10	
ΔVIN	A.C. Input Voltage Range See Note 2 & Figure 6		15			20			٧
Istrobe	TTL Logic Strobe Input Current in Either Hold or Sample Mode			0.1	10		0.1	10	μΑ

NOTES: 1. Offset voltage of op. amp. must be adjusted to 0mV (using  $20k\Omega$  potentiometer) before charge injection is measured.

The A.C. input voltage range differs from the D.C. input voltage range. All versions will handle any analog input within the range of plus 10V to minus 10V; however the IH5110, 5112, 5114 has the added restriction that the peak to peak swing should be less than

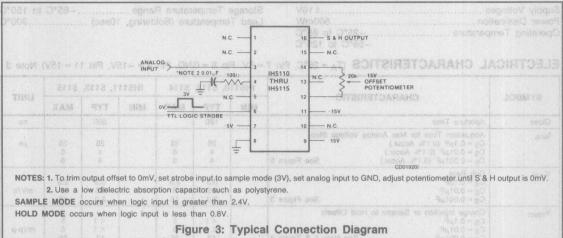
15Vp-p i.e.  $\pm 7.5$  Vac. 3. All of the electrical characteristics specs, are guaranteed with  $C_S = 0.01 \mu F$  in series with  $100\Omega$  as per Figure 3,  $C_S = 0.1 \mu F$  &  $C_S=0.001 \mu F$  are for design aid only. 4. If supplies are reduced to  $\pm 12 VDC$ , analog signal range will be reduced to  $\pm 7 Vp-p$ .

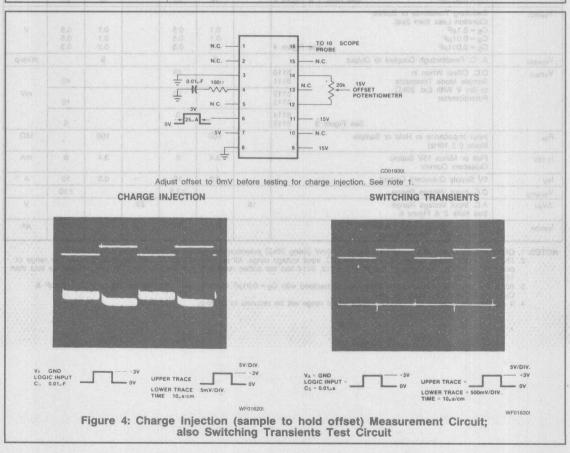
5-95

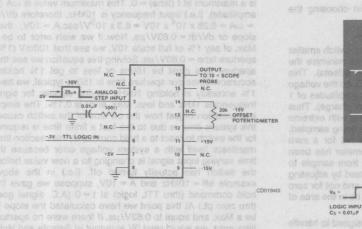
### IH5110-IH5115

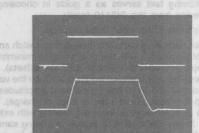
### **WINNERSIL**

#### APPLICATIONS INFORMATION







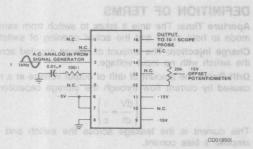


ACQUISITION TIME



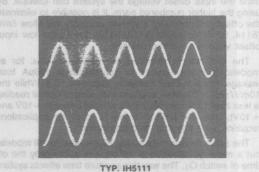
NOTE: The acquisition time is actually a settling time spec. since the reading is only taken when the output has settled within 1% of its final value. The 6µs spec. (IH5111, 5113 & 5115 is the worst reading of the t<sub>on</sub> or t<sub>off</sub> settling time shown above. The above test can be performed with a 0 to +7.5V or 0 to -7.5V step for the IH5110, I5112, 5114.

Figure 5: Typical Circuit for Measurement of A.C. Signal Handling Capability



To test this parameter, increase the amplitude of the signal generator until the output starts to distort (it will always show up on the positive excursion of the sine wave first); then back off until all distortion is gone. The resultant peak to peak swing must be greater than 15Vpp for the IH5110, 5112, 5114 and greater than 20Vpp for the IH5111, 5113, 5115.

#### A.C. PEAK TO PEAK



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WF01650

Figure 6: Typical Circuit for Measurement of A.C. Peak to Peak Signal Handling Capability

### IH5110-IH5115



#### **APPLICATION TIPS**

The following text serves as a guide in choosing the correct device from the IH5110 family.

First, determine the input voltage range.

The even numbered parts are designed to switch smaller A.C. signal amplitudes with the goal being to minimize the charge injection effects (sample to hold offsets). This charge injection error is shown in Figure 4. Once the voltage offset is zeroed, the 5110 has typical error amplitudes of to 2mVp-p (corresponds to 10pc to 20pc of charge). Thus one could sample very low level d.c. signals with extreme accuracy. If very low level A.C. signals are being sampled, voltage offset potentiometer can be adjusted for a zero charge injection effect. Once the potentiometer has been adjusted, there will be a zero error going from sample to hold; however there will be a d.c. error caused by adjusting the potentiometer for zero charge injection and not for zero voltage offset. In general, this d.c. error will be in the area of 2mV to 5mV.

The odd numbered parts are primarily designed to handle any input in the plus or minus 10V range, regardless of whether it is A.C. or D.C.; to obtain this, the charge injection is about a factor of 2 higher than the even numbered parts.

The use of Varafet switching elements similar to Intersil's IH401/401A leads to a trade-off between AC signal swing and charge injection.

After the voltage range and charge injection requirements have been determined, all that remains is to determine the input offset voltage the system can tolerate. By using the higher numbered parts, it is possible to eliminate the offset potentiometer if system accuracy will allow 5mV (5114, 5115) or 10mV (5112, 5113) due to the low input offset voltage on these devices.

The drift rate is specified at 10mV/sec. Max. for all models: this corresponds to approximately 100pA total leakage into a  $0.01\mu F$  sampling capacitor ( $C_S$ ). While the 10mV/sec. is the Max. encountered, a more typical reading is less than 1mV/sec. (true for any input between -10V and +10V); thus the IH5110 family is ideal for applications requiring very low drift or droop rates.

The aperture time is spec'd at 200ns Max. for all models, but a more typical value is 150ns; this is basically the off time of switch  $Q_1$ . The way this aperture time affects system accuracy is shown below:

Assume the input signal to the Sample and Hold is an A.C. signal of peak amplitude A (peak to peak swing is 2A) and frequency  $2\pi f = \omega$ , then  $V_{input} = Ae^{j\omega t}$  and dV/dt

=  $jA\omega e^{j\omega t}$ . This means the slope of input signal = (dV/dt)is a maximum at t (time) = 0. This maximum value is  $\omega A$  (in amplitude). (i.e.) input frequency is 10kHz, therefore dV/dt =  $\omega$ A = 6.28 x 10<sup>4</sup> x 10V = 6.3 x 10<sup>5</sup>V/sec.A = 10V, then slope or  $dV/dt = 0.63V/\mu s$ . Now if we wish error to be a Max. of say 1% of full scale 10V, we see that 100mV (1%/ aperture time =  $0.63V/\mu s$ . Solving this equation we see that aperture time must be 160ns or less to get 1% holding accuracy. Since our aperture time is 150ns typical, we have 1% accuracy in holding 10kHz varying signals; for signal frequencies 1kHz and less, Max. error is 0.1%. The simple interpretation of just how the off time of the switch causes this system error is due to the fact a finite time is required for the switch to react to a hold command: this reaction time manifests itself with a system voltage error because the time varying input signal is changing to a new value before the switch has actually turned off. (i.e.) in the above example off = 10kHz and A = 10V, suppose we gave the hold command (thru TTL logic) at t = 0 (A.C. signal goes thru zero pt.) At this point we have calculated the slope to be a Max. and equal to 0.63V/µs. If there were no aperture time error, we would read 0V at output of Sample and Hold; however because of finite time for switch to respond to hold command, 150ns passes before switch goes off. During this 150ns, the input signal has gone to 100mV above or below 0V, thus the stored value of signal will be 100mV and that is the reading at the output of the Sample and Hold. If the input frequency were 1kHz, the "error voltage" would be 10mV.

#### **DEFINITION OF TERMS**

Aperture Time: The time it takes to switch from sample mode to hold mode and the actual opening of switch.

Charge Injection: The amount of charge coupled across the switch with no input voltage.

**Drift Rate:** The amount of drift of output voltage at a rate caused by current flow through the storage capacitor.

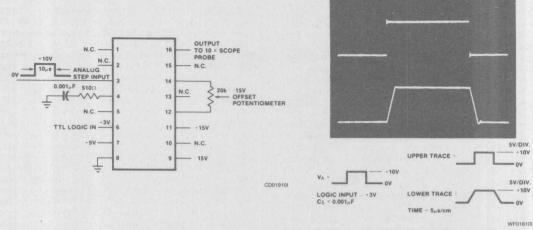
$$\left(\frac{dV}{dt} = \frac{i}{c}\right)$$

This current is the leakage across the switch and the amplifier's bias current.

Feed Through: The amount of input signal that appears at the output when in the hold mode. Normally caused by capacitance across the switch.

Offset Voltage: Voltage measured at output with no input voltage and circuit in sample mode.

Acquisition Time: The time it takes amplifier to reach full scale output either plus or minus.

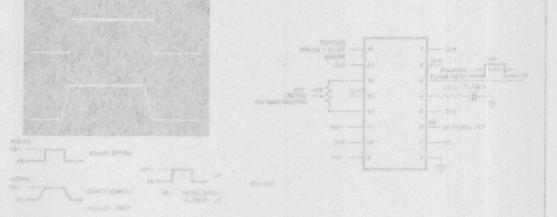


NOTE: Typical times for the Sample and Hold to acquire the input are 2μs for turn on (output) goes to +10V and 3μs for turn off (output goes down to 0V). As a general note, all the electrical specifications are guaranteed with a sampling capacitor equal to 0.01 μf. As the above application (Fig. 6) shows, other values of sampling capacitors can be used but the best combinations of S & H specs may not result with values other than 0.01 μF. The only advantage of using a 0.001 μF for C<sub>s</sub> is the acquisition time is 2μs typical instead of 5μs typical (with 0.01 μF; however the drift rate would be worse and charge injection would be affected). To minimize drift rate, use a 0.1 μF capacitor; this should produce a 0.1 mV/sec rate of change and a charge injection amplitude of 0.2 mVp-p. Of course the acquisition time will be slowed down to the 25μs area. Also use a 0.1 μs system for slow speed changes (i.e., input frequency is less than 1 kHz. The series resistor should be about 100Ω – 200Ω to stabilize the system.

Figure 7: Connection For Hi-Speed Sample and Hold With Following Typical Performance: W/C<sub>S</sub> = 0.001

- a. 2µs settling time (acquisition time) to 1% accuracy
- b. 25mV charge injection amplitude
- c. 10mV/sec drift rate

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NOTE: Typical breat or the Sample and Hold to appare the input on (output) goes for + 10V and 3 us for sum off (output) goes down to 20V. As a general inches all the steptical specifications are guaranteed with a sample countries of sample page o

Figure 7: Connection For HI-Speed Sample and Hold With Following Typical Performance:  $W/E_{\rm S} \approx 0.001$ 

- a 24s settling time (acquisition time) to 1% accuracy
  - SemV charce in ection amplitude
    - is finb as \Vmok a

## Section 6 — Data Acquisition

Section 6 - Data Acquisition

## AD7520/AD7530 AD7521/AD7531

10/12-Bit Multiplying D/A Converters

#### GENERAL DESCRIPTION

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Intersil's thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

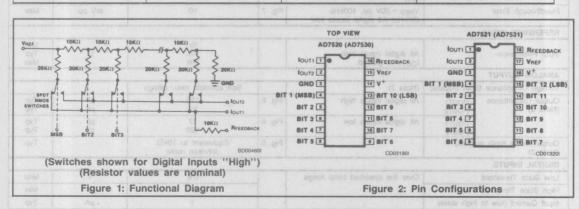
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#### **FEATURES**

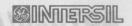
- AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity
- AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity
- Low Power Dissipation: 20mW (Max)
- Low Nonlinearity Tempco: 2 ppm of FSR/°C
- Current Settling Time: 500ns to 0.05% of FSR
- Supply Voltage Range: +5V to +15V
- TTL/CMOS Compatible
- Full Input Static Protection
- /883B Processed Versions Available

#### ORDERING INFORMATION

XSM FIGH to an	(86-0) 8.0		PART NUMBER/PACKAGE	
NONLINEARITY	PLASTIC DIP	10.0	CERDIP	CERDIP
0.2% (8-Bit)	AD75120JN AD7530JN AD7521JN AD7531JN	6.28	AD7520JD AD7530JD AD7521JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN		AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	A .(6)	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD
TEMPERATURE RANGE	0°C to +70°C	18 -UE	-25°C to +85°C	-55°C to +125°C



### AD7520/7530/7521/7531



#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C unless otherwise noted)

Supply Voltage (V <sup>+</sup> )+17V	Operating Temperature
V <sub>REF</sub> ±25V	JN, KN, LN Versions 0°C to +70°C
Digital Input Voltage RangeV+ to GND	JD, KD, LD Versions25°C to 85°C
Output Voltage Compliance100mV to V+	SD, TD, UD Versions55°C to +125°C
Power Dissipation (package)	Storage Temperature65°C to 150°C
up to +75°C450mW	Lead Temperature (Soldering, 10sec)300°C
dorate above +75°C @ 6mW/°C	STATE AND THE STATE OF THE STAT

#### CAUTION:

- 1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- 2) Do not apply voltages higher than VDD or less than GND potential on any terminal except VREF and RFEEDBACK.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS** (V + = +15V, V<sub>REF</sub> = +10V, T<sub>A</sub> = 25°C unless otherwise specified)

PARAM	ETER		TEST CONDITIONS		AD7520 (AD7530)	AD7521 (AD7531)	UNIT	LIMIT
DC ACCURACY (	Note 1)							
Resolution					10	12	Bits	MUN
Nonlinearity (Note 2)		J	S, T, U: over $-55^{\circ}$ C to = 125°C	Fig. 3	0.2 (	8-Bit)	% of FSR	Max
93	VERSION	K	9(0)30	Fig. 3	910 0.1 (	9-Bit)	% of FSR	Max
GSD.		L	-10V ≤ V <sub>REF</sub> ≤ = 10V	Fig. 3	0.05 (	10-Bit)	% of FSR	Max
Nonlinearity Tempo (Notes 2 and 3)	00		DETSETUR		47078870.2	2	ppm of FSR/°C	Max
Gain Error (Note 2	) and A		-10V ≤ V <sub>REF</sub> ≤ +10V		V//UE 0.	.3	% of FSR	Тур
Gain Error Tempco	(Notes 2	and	AD7530KD AD7521KD		Drssikn	0	ppm of FSR/°C	Max
Output Leakage Coutput)	urrent (eithe	r	Over the specified temperature range		/LJ0537 (30	00	nA	Max
Power Supply Reje	ection (Note	2)	U./U.c. CA	Fig. 4	±0.	005	% of FSR/%	Тур
AC ACCURACY (I	Note 3)		EL FERRICIA		LA LEPONICIA			
Output Current Set	ttling Time		To 0.05% of FSR (All digital inputs low to high and high to low)	Fig. 8	50°07 + 01°0		ns	Тур
Feedthrough Error			V <sub>REF</sub> = 20V pp, 100kHz (50kHz) All digital inputs low	Fig. 7	1	0	mV pp	Max
REFERENCE INPL	Taren		WORLY NOT					
Input Resistance	(B) (C) (B) (B) (B) (B) (B) (B) (B) (B) (B) (B		All digital inputs high IOUT1 at ground.		10	ok Ok	Ω	Min Typ Max
ANALOG OUTPUT	\$30 dWa		San Carlotte		7	The State of the S		
Voltage Complianc	e (both out)	puts)	(Note 3)		See absolute	max. ratings		
Output Capacitance (Note 3)	e loute		All digital inputs high	Fig. 6	3	20	pF pF	Тур Тур
8 THE TOTAL	lout:		All digital inputs low	Fig. 6	3		pF pF	Typ Typ
Output Noise (both (Note 3)	outputs)		8 \$10 [E]   (E)   Fig. 5	Equivalent Johnso	t to 10kΩ n noise		Тур	
DIGITAL INPUTS					"delir" etuşi	श सर्वाच्या ४०१	nworla seriotiw	4)
Low State Thresho	old		Over the specified temp range		0.	.8	V	Max
High State Thresho	old	000	Figure 2: Pin		100 2	4 lesceromi-	il oncyl	Min
Input Current (low	to high sta	te)				1	μΑ	Тур
Input Coding		199	See Tables 1 & 2		Binary/Off	set Binary		Contract of



### AD7520/7530/7521/7531

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

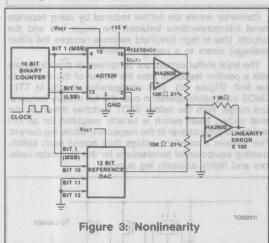
PARAMETER	TEST CONDITIONS	AD7520 (AD7530)	AD7521 (AD7531)	UNIT	LIMIT
POWER REQUIREMENTS		\$40000,0000		Parameter and	TENT
Power Supply Voltage Range	V-g-VV-g-VV-g-VV-g-VV-g-VV-g-VV-g-VV-g	+51	0 + 15	OF SECOND A TOTAL OF THE PERSON OF THE PERSO	NA U 200VA
1+ 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	All digital inputs at 0V or V+		1 5 ,2192	μΑ	Тур
nime } share s area.	All digital inputs high or low		2 5	mA	Max
Total Power Dissipation (Including the ladder network)	pile pile pilerane	internati	20	mW	Тур

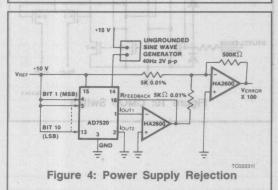
NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.

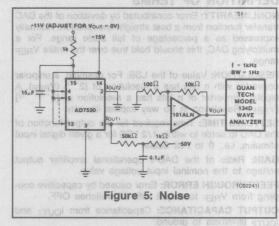
2. Using internal feedback resistor, RFEEDBACK.

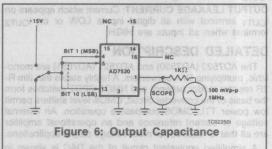
3. Guaranteed by design, not subject to test. 4. Accuracy not guaranteed unless outputs at GND potential.

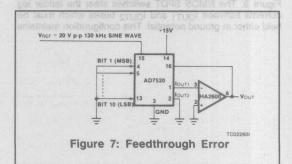
TEST CIRCUITS NOTE: The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.



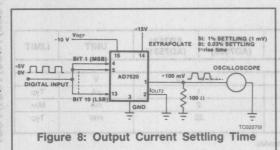








### AD7520/7530/7521/7531



#### **DEFINITION OF TERMS**

**NONLINEARITY:** Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V<sub>REF</sub> range.

**RESOLUTION:** Value of the LSB. For example, a unipolar converter with n bits has a resolution of  $(2^{-n})$  (V<sub>REF</sub>). A bipolar converter of n bits has a resolution of  $[2^{-(n-1)}]$  [V<sub>REF</sub>]. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V<sub>REF</sub> to output with all switches OFF.

**OUTPUT CAPACITANCE:** Capacitance from I<sub>OUT1</sub> and I<sub>OUT2</sub> terminals to ground.

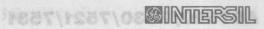
**OUTPUT LEAKAGE CURRENT:** Current which appears on I<sub>OUT1</sub> terminal with all digital inputs LOW or on I<sub>OUT2</sub> terminal when all inputs are HIGH.

#### **DETAILED DESCRIPTION**

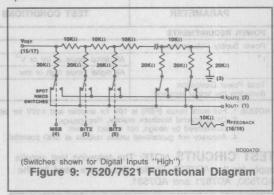
The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS SPDT switches steer the ladder leg currents between I<sub>OUT1</sub> and I<sub>OUT2</sub> buses which must be held either at ground potential. This configuration maintains



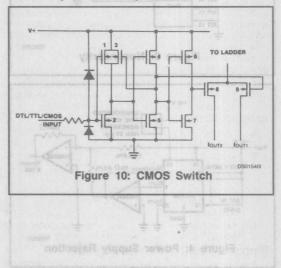


a constant current in each ladder leg independent of the input code.



Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 10). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.



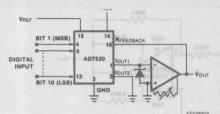


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

TABLE 1 CODE TABLE - UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	-V <sub>REF</sub> (1-2 <sup>-n</sup> )
100000001	-V <sub>REF</sub> (1/2 + 2 <sup>-n</sup> )
Mgib is yd 1000000000 w golsn	-V <sub>REF</sub> /2
0111111111	-V <sub>REF</sub> (1/2-2 <sup>-n</sup> )
000000001	-V <sub>REF</sub> (2 <sup>-n</sup> )
000000000	0 (561

**NOTE:** 1. LSB =  $2^{-n}$  VRFF 2. n = 10 for 7520, 7530 n = 12 for 7521, 7531

### **APPLICATIONS**

#### Unipolar Binary Operation

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 11. With positive and negative VRFF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

#### ZERO OFFSET ADJUSTMENT

- 1. Connect all digital inputs to GND.
- 2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at VOUT.

#### GAIN ADJUSTMENT

- 1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V+. to alled be a od! and a
- 2. Monitor VOLIT for a -VREE (1-2-n) reading. (n = 10 for AD7520 (AD7530) and n = 12 for AD7521 to 3 vd (AD7531)). reases or corolle line noticely
- 3. To decrease Vout, connect a series resistor (0 to 500Ω) between the reference voltage and the VREE
  - 4. To increase VOUT, connect a series resistor (0 to 500 $\Omega$ ) in the lour, amplifier feedback loop.

#### Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/ Analog Output Value" table for bipolar mode is given in Table 2.

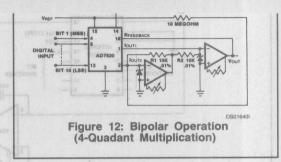


TABLE 2 CODE TABLE - BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
Er e-1111111111	-VREF (1-2-(n-1))
100000001	-V <sub>REF</sub> (2 <sup>-(n-1)</sup> )
100000000	0
0111111111	V <sub>REF</sub> (2 <sup>-(n-1)</sup> )
000000001	V <sub>REF</sub> (1-2 <sup>-(n-1)</sup> )
0000000000	NA VREFORM LEGISLACIONO

**NOTE:** 1. LSB =  $2^{-(n-1)}$  VREE 2. n = 10 for 7520 and 7521 n = 12 for 7530 and 7531

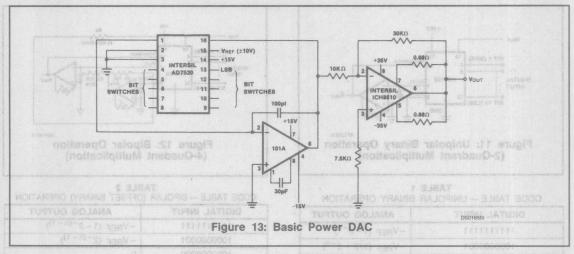
A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to lours bus. A "Logic 0" input forces the bit current to lours bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from VREF to IOUT2.

#### OFFSET ADJUSTMENT

- 1. Adjust VRFF to approximately +10V.
  - 2. Connect all digital inputs to "Logic 1".
- 3. Adjust IOUT2 amplifier offset adjust trimpot for 0V ±1mV at IOUT2 amplifier output.
- 4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic O".
  - Adjust IOUT1 amplifier offset adjust trimpot for 0V ±1 mV at VOUT.

### GAIN ADJUSTMENT

- Connect all digital inputs to V+
- Monitor VOUT for a -VRFF (1-2-(n-1)) volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
- To increase Vout, connect a series resistor of up to 500Ω between VouT and RFEEDBACK.
- To decrease Vout, connect a series resistor of up to  $500\Omega$  between the reference voltage and the VRFF terminal.



#### **POWER DAC DESIGN USING AD7520**

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 13. An INTERSIL IH8510 power operational amplifier (1 Amp continuous output at up to  $\pm 25V$ ) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the IH8510, by using a 25V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021: Power D/A Converters Using The IH8510 by Dick Wilenken.)

### Analog/Digital Division

With the AD7520 connected in its normal multiplying configuration as shown in Figure 13, the transfer function is:

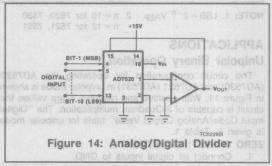
$$V_{O} = -V_{IN} \left( \frac{A_{1}}{2^{1}} + \frac{A_{2}}{2^{2}} + \frac{A_{3}}{2^{3}} + \cdots + \frac{A_{n}}{2^{n}} \right)$$

where the coefficients  $A_{\rm X}$  assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 14, the transfer function becomes:

$$V_{O} = \left(\frac{-V_{IN}}{\frac{A_{1}}{2^{1}} + \frac{A_{2}}{2^{2}} + \frac{A_{3}}{2^{3}} + \dots + \frac{A_{n}}{2^{n}}}\right)$$

This is division of an analog variable (Vi<sub>N</sub>) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).



For further information on the use of this device, see the following Application Bulletins:

A016 "Selecting A/D Converters," by David Fullagar

A018 "Do's and Don'ts of Applying A/D Converters," by
Peter Bradshaw and Skip Osgood

A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed

A021 "Power D/A Converters Using the IH8510," by Dick Wilenken

### AD7523 8-Bit Multiplying D/A Converter

### GENERAL DESCRIPTION STANDED

The AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.

Low noise audio gain controls, motor speed controls, digitally controlled gain and attenuators are a few of the and war at a few of wide range of applications of the 7523.

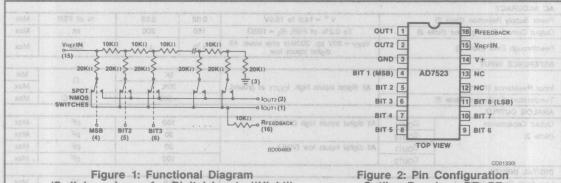
### FEATURES ..... egraph egation futural tableic

- 8, 9 and 10 Bit Linearity oneligned energy fuguro
- Low Gain and Linearity Temperature Coefficients
- Full Temperature Range Operation
- Static Discharge Input Protection
- DTL/TTL/CMOS Compatible
- +5 to +15 Volts Supply Range
- Fast Settling Time: 150ns Max at 25°C
- Four Quadrant Multiplication

#### ORDERING INFORMATION

	PART NUMBER/PACKAGE			
NONLINEARITY	PLASTIC DIP	CERDIP	CERDIP	
0.2% (8 Bit)	Marie and Services and the ser	AD7523AD	AD7523SD	
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD	
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD	
TEMPERATURE RANGE	0°C to +70°C	-25°C to +85°C	-55°C to +125°C	





(Switches shown for Digital Inputs "High")

Outline Drawings DE, PE

mW
1/°C
O°C
5°C
5°C
0°C
0°C
1

- 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- 2. Do not apply voltages higher than VDD and lower than GND to any terminal except VREF + RFEEDBACK.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS (V+ = +15V, VREF = +10V unless otherwise specified)

PARAMETEI	3	TEST CONDITIONS	T <sub>A</sub> +25°C	T <sub>A</sub> MIN-MAX	RIN TINUEOE	LIMIT
DC ACCURACY (Note 1)		CHANGE SHOW SHOW THE RESIDENCE	NPACKAG	PART WANGE		
Resolution		alcoes:	8 910	8 9 9	Bits	Min
Nonlinearity (Note 2)	(± ½ LSB)		±0.2	±0.2	% of FSR	Max
	(± 1/4 LSB)	-10V ≤ V <sub>REF</sub> ≤ +10V	±0.1	8 08±0.1 /LES	% of FSR	Max
	(± 1/8 LSB)	V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0V	±0.05	±0.05	% of FSR	Max
Monotonicity		Unuserve	Gu	aranteed	G.CA	(HE 9)
Gain Error (Note 2)		Digital Inputs high.	±1.5	±1.8	% of FSR	Max
Nonlinearity Tempco (Notes 2	and 3)	-10V V <sub>REF</sub> +10V	- June	2	ppm of FSR/°C	Max
Gain Error Tempco (Notes 2 a	ind 3)	-55°C 10	100	10	ppm of FSR/°C	Max
Output Leakage Current (either	output)	V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0	±50	±200	nA	Max
AC ACCURACY				THE PROPERTY OF		
Power Supply Rejection (Note	2)	V + = 14.0 to 15.0V	0.02	0.03	% of FSR	Max
Output Current Settling Time (Note 3)		To 0.2% of FSR, $R_L = 100\Omega$	150	200	ns	Max
Feedthrough Error (Note 3)	III sm	V <sub>REF</sub> = 20V pp, 200kHz sine wave. All digital inputs low.	± 1/2	11H01 ±1H01	LSB	Max
REFERENCE INPUT			2	3 5	- 3	100
26 61 2	SOLEM THE WASTER	N 1 340		5K		Min
Input Resistance (Pin 15)		All digital inputs high. IOUT1 at ground.	20K		Ω	Max
Temperature Coefficient (Note 3)		(Sheuci o	1.4	-500	ppm/°C	Max
ANALOG OUTPUT	101.0	the state of the s				
Output Capacitance	C <sub>OUT1</sub>	All digital inputs high (VINH)	30 30		pF	Max
(Note 3)	C <sub>OUT2</sub>				pF	Max
	C <sub>OUT1</sub>	All digital inputs low (VINL)			pF	Max
	C <sub>OUT2</sub>		100		pF	Max
DIGITAL INPUTS	CO VISION NO NA	Courses Course	Ser Incom	10 mm 12 - F . m	ment?	
Low State Threshold (VINL)	fine Drawit	DO Printelia Company	ni terimi	0.8	V	Max
High State Threshold (VINH)		Control for chighten control for so the region of the residence	Marie San Company	2.4	V	Min
Input Current (Low or high)		V <sub>IN</sub> = 0V or +15V	±1		μΑ	Max
Input Coding		See Tables 1 & 2	Binary/	Offset Binary		
Input Capacitance (Note 3)			4		pF	Max
POWER REQUIREMENTS					WEST OF BUILDING	
Power Supply Voltage Range		Accuracy is tested and guaranteed at V + = +15V, only.	+ 5	5 to +16	V	
1+		All digital inputs low or high.	2		mA	Max

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, RFEEDBACK.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

#### **APPLICATIONS**

#### UNIPOLAR OPERATION

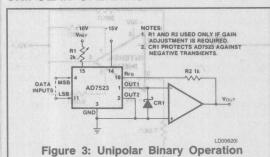


Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT		
11111111	-VREF (255)		
10000001	-V <sub>REF</sub> (129)		
10000000	$-V_{REF}$ $\left(\frac{120}{256}\right) = -\frac{V_{REF}}{2}$		
C. For example, a unio			
0000001			
0000000			

**NOTE:** 1 LSB =  $(2^{-8})$  (V<sub>REF</sub>) =  $\left(\frac{1}{256}\right)$  (V<sub>REF</sub>)

#### BIPOLAR OPERATION

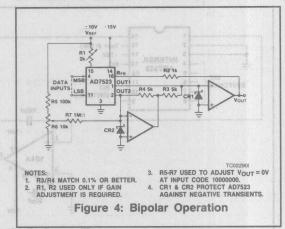


Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT		
11111111	-V <sub>REF</sub> (127)		
10000001	$-V_{REF}$ $\left(\frac{1}{128}\right)$		
10000000	2712 2/1 1 E		
01111111	+ VREF (128)		
0000001	+ V <sub>REF</sub> $\left(\frac{127}{128}\right)$		
00000000	+ V <sub>REF</sub> $\left(\frac{128}{128}\right)$		

**NOTE:** 1 LSB =  $(2^{-7})$  (V<sub>REF</sub>) =  $(\frac{1}{128})$  (V<sub>REF</sub>)

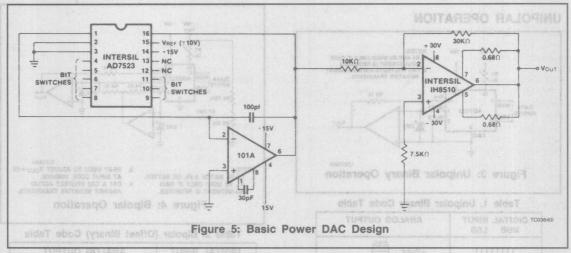
A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 5. The Intersil IH8510 power operational amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage, whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the IH8510, by using a 25 volt reference for the DAC.

Now were  $\left(\frac{R_1}{R_1+R_2}\right) \cdot \left(\frac{R_1R_2}{R_1-R_2}\right)$  where  $R_1 = \frac{R_1R_2}{R_1} \cdot \frac{R_1R_2}{R_2} \cdot \frac{R_1R_2}{R_2}$  (or  $R_2 = \frac{2R_2}{R_2}$ ).



#### POWER DAC DESIGN USING AD7523



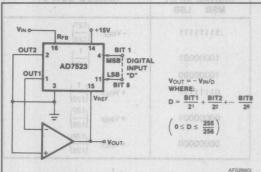
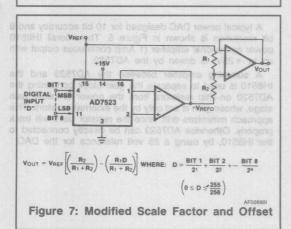


Figure 6: Divider (Digitally Controlled Gain)



#### **DEFINITION OF TERMS**

**NONLINEARITY:** Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V<sub>REF</sub> range.

**RESOLUTION:** Value of the LSB. For example, a unipolar converter with n bits has a resolution of  $(2^{-n})$  (V<sub>REF</sub>). A bipolar converter of n bits has a resolution of  $[2^{-(n-1)}]$  [V<sub>REF</sub>]. Resolution in no way implies linearity.

**SETTLING TIME:** Time required for the output function of the DAC to settle to within  $\frac{1}{2}$  LSB for a given digital input stimulus, i.e., 0 to Full Scale.

**GAIN:** Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

**FEEDTHROUGH ERROR:** Error caused by capacitive coupling from V<sub>REF</sub> to output with all switches OFF.

 $\mbox{\bf OUTPUT CAPACITANCE:}$  Capacity from  $\mbox{\bf I}_{\mbox{\scriptsize OUT1}}$  and  $\mbox{\bf I}_{\mbox{\scriptsize OUT2}}$  terminals to ground.

**OUTPUT LEAKAGE CURRENT:** Current which appears on I<sub>OUT1</sub> terminal with all digital inputs LOW or on I<sub>OUT2</sub> terminal when all inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

A016 "Selecting A/D Converters," by David Fullagar

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A020 ''A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing' by Ed Sliger

A021 ''Power D/A Converters Using the IH8510,'' by Dick Wilenken

## AD7533 10-Bit Multiplying D/A Converter

### GENERAL DESCRIPTION

The Intersil AD7533 is a low cost, monolithic 10-bit, fourquadrant multiplying digital-to-analog converter (DAC). Intersil's thin-film resistor on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V supply voltage range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Applications for the AD7533 include programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

#### ORDERING INFORMATION

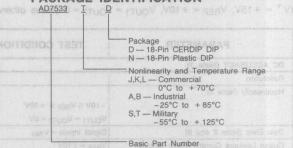
	TEMPERATURE RANGE				
NONLINEARITY	0°C to +70°C	-25°C to +85°C	-55°C to + 125°C		
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD		
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD		
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD		

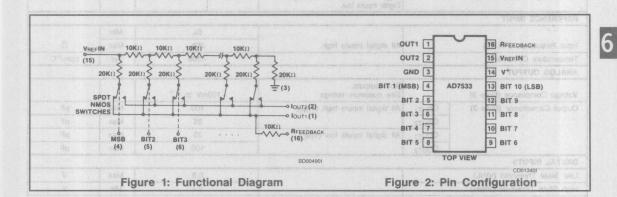
# MISK

### FEATURES Spane Spane Spane Vigni Island

- Lowest Cost 10-Bit DAC
- 8, 9 and 10 Bit Linearity
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- TTL/CMOS Direct Interface
- +5 to +15 Volts Supply Range Low Power Dissipation
- Fast Settling Time
- Four Quadrant Multiplication
- Direct AD7520 Equivalent
- 883B Processed Versions Available

### PACKAGE IDENTIFICATION





#### AD7533



### ABSOLUTE MAXIMUM RATINGS (TA = 25°C unless otherwise noted)

	DIA Converter
V <sup>+</sup> +17V	Plastic Package:
VRFF±25V	up to 70°C670mW
Digital Input Voltage RangeV <sup>+</sup> to GND	derates above 70°C by8.3mW/°C
Output Voltage Compliance -0.1V to V <sup>+</sup>	Operating Temperature Range:
Power Discipation OAC 16-01 7500 755WOJ 8	JN, KN, LN Versions 0°C to +70°C
Ceramic Package:	AD, BD, CD Versions25°C to 85°C
up to +75°C	SD, TD, UD Versions55°C to +125°C
derates above +75°C by6mW/°C	Storage Temperature Range65°C to 150°C
Full Imput States Protection	Lead Temperature (Soldering, 10sec)+300°C

#### CAUTION

- The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- 2. Do not apply voltages lower than ground or higher than V+ to any pin except V<sub>REF</sub> and R<sub>FB</sub>.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS

(V  $^+$  = +15V, V<sub>REF</sub> = +10V, V<sub>OUT1</sub> = V<sub>OUT2</sub> = 0 unless otherwise specified.)

PARAMETER	Paukag D— 18	TEST CONDITION	NS	T <sub>A</sub> +25°C	T <sub>A</sub> MIN-MAX	LIMIT	UNIT
DC ACCURACY (Note 1)			68288	NOA   GA	SOUTH ADVERS	SOAT I	(88-8)
Resolution	- 100		revens	10	10	Min	Bits
Nonlinearity (Note 2)	La A			±0,2	±0.2	Max	% of FSR
		-10V ≤ V <sub>REF</sub> ≤ +10V	QUES	MGA±0.1 GO	savoa±0.1 MJ688	Max	% of FSR
Williamy + 126°C		V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0V	Management	±0.05	±0.05	Max	% of FSR
Gain Error (Note 2 and 5)		Digital Inputs = VINH	1000	±1.4	±1.5	Max	% of FS
Output Leakage Current (either out	tput)	V <sub>REF</sub> = ±10V		±50	±200	Max	nA
AC ACCURACY							
Power Supply Rejection (Note 2)		V + = 14.0 to 17.0V		0.005	0.008	Max	% of FSR/%
Output Current Settling Time (Note	3)	To 0.05% of FSR, R <sub>L</sub> = 100	Ω	600 (Note 6)	800 (Note 3)	Max	ns
Feedthrough Error (Note 3)		V <sub>REF</sub> = ±10V, 100kHz sine wa Digital inputs low.	ve.	±0.05	±0.1	Max	% FSR
REFERENCE INPUT		Alternatives of the Control of the C					
	antena .	GILLERY TESTS	Shall to take		5k	Min	
Input Resistance (Pin 15)	[1] 170	All digital inputs high.		n Mitt	20k	Max	Ω
Temperature Coefficient	[2] 270	Elegation policy	1.7	protection in the second	-300	Тур	ppm/°C
ANALOG OUTPUT	[E] GHI		Same	Eanas Eana	in Samuel Su	me Zinnes	Challian I
Voltage Compliance (Note 3)	(B) (ac)	Both outputs. See maximum ratings	四生	-100	0mV to V+	- 1,10	
Output Capacitance (Note 3)	C <sub>OUT1</sub>	All digital inputs high (VINH)	15		100	Max	pF
	C <sub>OUT2</sub>	\$19 mus	11 00000		35	Max	pF
A A16 FE	C <sub>OUT1</sub>	All digital inputs low (VINL)	90-11/1		35	Max	pF
9 116 8	C <sub>OUT2</sub>				100	Max	pF
DIGITAL INPUTS		1803-0008					
Low State Threshold (VINL)	O -0			4 19% June	0.8	Max	V
High State Threshold (VINH)	1 10 41	Pit	TRATE	Marks Tollyno	2.4	Min	V
Input Current (I <sub>IN</sub> )		V <sub>IN</sub> = 0V and V <sup>+</sup>			±1	Max	μΑ
Input Coding		See Tables 1 & 2		Binary/	Offset Binary		
Input Capacitance (Note 3)					5	Max	pF

TA MIN-MAX	LIMIT	UNIT	
ADLIBIT H	IN THE	ARCAUO	

Max

+25°C	MIN-MAX	LIMIT	UNIT
MON	LTIPLICAT	UM THA	HCAUO-
+1	5 ±10%	-	V
+5	to +16		V
	2	Max	mA

Vnn

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes

Rated Accuracy

TEST CONDITIONS

Digital Inputs = VINI to VINIH Digital Inputs = 0V or V

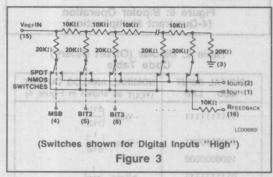
- 2. Using internal feedback resistor, REEEDBACK. 3. Guaranteed by design; not subject to test.
  - 4. Accuracy not guaranteed unless outputs at ground potential.
  - 5. Full scale (FS) = -(VRFF) (1023/1024)
  - 6. Sample tested to ensure specification compliance

#### DETAILED DESCRIPTION

POWER REQUIREMENTS

Power Supply Voltage Range

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

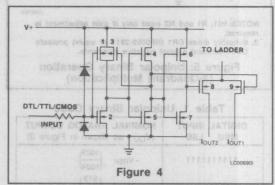


A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS SPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a change without notice.

μА

Specifications subject to

constant current in each ladder leg independent of the input code

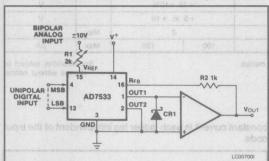


The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 4). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch. creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

6

#### **APPLICATIONS**

#### UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES: Inl1. R1 and R2 used only if gain adjustment is required.

2. Schottky diode CR1 (HP5082-2811 or equiv) protects OUT1 terminal against negative transients.

Figure 5: Unipolar Binary Operation (2-Quadrant Multiplication)

Table 1. Unipolar Binary Code

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 3)
11111111111	-VREF (1023)
100000001	-VREF (513)
100000000	/5121 VRFF
0111111111	
000000001	stande prop ( )
000000000	$-V_{REF}  \left(\frac{0}{1024}\right) = 0$

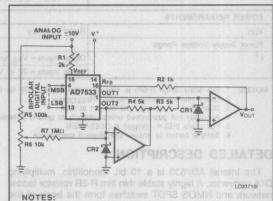
NOTES: 1. Nominal Full Scale for the circuit of Figure 3 is given by

$$FS = -V_{REF} \left( \frac{1023}{1024} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given

LSB = 
$$V_{REF}$$
  $\left(\frac{1}{1024}\right)$ 

#### **BIPOLAR OPERATION** (4-QUADRANT MULTIPLICATION)



1. R3/R4 match 0.05% or better.

2. R1 and R2 used only if gain adjustment is required.

3. Schottky diodes CR1 and CR2 (HP5082-2811 or equiv) protect OUT1 and OUT2 terminals against negative

> Figure 6: Bipolar Operation (4-Quadrant Multiplication)

Table 2. Bipolar (Offset Binary) Code Table

	The second secon					
DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (Vout as shown in Figure 4)					
1111111111	-V <sub>REF</sub> (511)					
1000000001	0 0 1 0 1					
0111111111 nworle et DAG entr	+ VREF (1/512)					
000000001	+ V <sub>REF</sub> (511)					
000000000	+ V <sub>REF</sub> (512) brushing is ble					

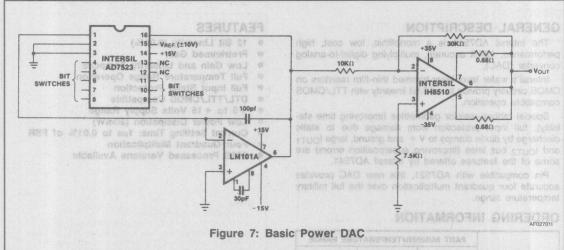
NOTES: 1. Nominal Full Scale for the circuit of Figure 4 is given by

$$SR = V_{REF} \left( \frac{1023}{512} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given

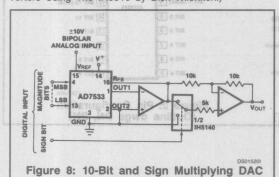
LSB = 
$$V_{REF}$$
  $\left(\frac{1}{512}\right)$ 

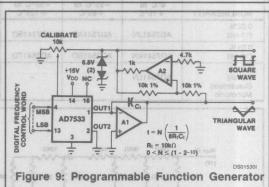
#### **POWER DAC DESIGN USING AD7533**



A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 7. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to  $\pm 25$ V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the LM101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)





#### INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.

#### GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V + and ground, large I<sub>OUT1</sub> and I<sub>OUT2</sub> bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

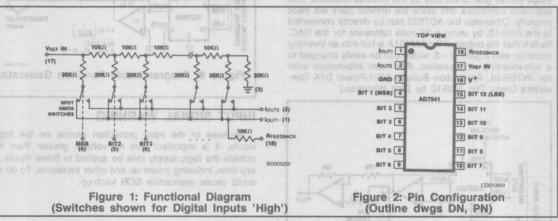
Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

#### ORDERING INFORMATION

	PART NUMB	BER/TEMPERAT	URE RANGE
NONLINEARITY	0°C to +70°C	-25°C to +85°C	-55°C to + 125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	147	-

#### **FEATURES**

- 12 Bit Linearity (0.01%)
- Pretrimmed Gain
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- DTL/TTL/CMOS Compatible
- +5 to +15 Volts Supply Range
- Low Power Dissipation (20mW)
- Current Settling Time: 1µs to 0.01% of FSR
- Four Quadrant Multiplication
- 883B Processed Versions Available



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		-		

V+	Operating Temperature Range:
VBEF±25V	JN, KN, LN Versions 0°C to +70°C
Digital Input Voltage RangeGND to V+	AD, BD Versions25°C to +85°C
Output Voltage Compliance100mV to V <sup>+</sup>	SD, TD Versions55°C to +125°C
Power Dissipation (package):	Storage Temperature65°C to +150°C
up to +75°C450mW	Lead Temperature (Soldering, 10sec)300°C
derate above +75°C by 6mW/°C	Diel Sargebrad (SU) Inscreen

#### CAUTION

- 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- 2. Do not apply voltages higher than VDD or less than GND potential on any terminal except VREF and Rfb.

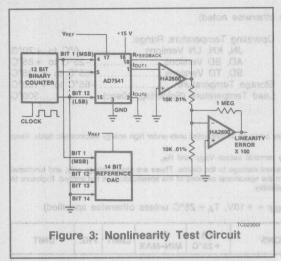
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

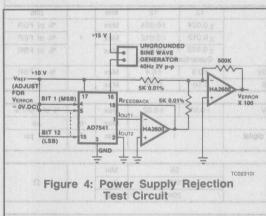
#### **ELECTRICAL CHARACTERISTICS** (V<sup>+</sup> = +15V, V<sub>REF</sub> = +10V, T<sub>A</sub> = 25°C unless otherwise specified)

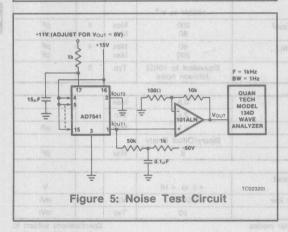
PARAMETER		TEST CONDITIONS	TA + 25°C	TA MIN-MAX	LIMIT	FIG.	UNIT
DC ACCURACY (Note 1)	RALEY TO					111 (11 (11 (11 (11 (11 (11 (11 (11 (11	
Resolution			12	12	Min		Bits
Nonlinearity (Note 2)	S		± 0.024	±0.024	Max		% of FSR
AND AND AND AND AND AND AND AND AND AND	Т	-10V ≤ V <sub>REF</sub> ≤ +10V	± 0.012	±0.012	Max	1	% of FSR
rough Error Test Circuit	2522	V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0V	± 0,012 Guarante	±0.012 ed Monotonic	Max		% of FSR
Gain Error (Note 2)		-10V ≤ V <sub>REF</sub> ≤ +10V	±0.3	±0.4	Max		% of FSR
Output Leakage Current (either output)		V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0	±50	±200	Max		nA
AC ACCURACY (Note 3)		Venton	Sult Su	75 G 5 7 G 100 100 100 100 100 100 100 100 100 1	216 J 31	111/02	MITTER POPULA
Power Supply Rejection (Note 2)		V <sup>+</sup> = 14.5 to 15.5V	±0.01	±0.02	Max	2	% of FSR/%
Output Current Settling Time	Vi Logos	To 0.01% of FSR	- 19	1	Max	6	μs
Feedthrough Error		V <sub>REF</sub> = 20V pp, 10kHz. All digital inputs low.		1	Max	5	mV pp
REFERENCE INPUT		TUPRI SATION	Applied .	1			
to our S homestion	- A(40.1	of 100 and topical		5K	Min		
Input Resistance		All digital inputs high.	Relectio	Montage 10Kagus and		th on	Ω
		IOUT1 at ground.		20K	Max		
ANALOG OUTPUT	minic	S. museum B.					
Voltage Compliance (Note 4)	rT .	Both outputs. See maximum ratings.	-100r	nV to V +	110000000000000000000000000000000000000		
Output Capacitance (Note 3)	Cour			200 60	Max Max	4	pF pF
	Cour			60 200	Max Max	4	pF pF
Output Noise (both outputs)	la mo	e telle transfer function f		ent to 10KΩ son noise	Тур	3	
DIGITAL INPUTS	note si	DACT residentials 1 Mars	20	7 (1001		ST ST	
Low State Threshold (VINL)		raches (single.	I FYY	0.8	Max		٧
High State Threshold (VINH)	in audi	JACOUTH JOODES   GRO	1001	2.4	Min	ACTOR	٧
Input Current		V <sub>IN</sub> = 0 or V <sup>+</sup>		±1	Max	2 8	μΑ
Input Coding	2011	See Tables 1 & 2	Binary/C	Offset Binary	test		1
Input Capacitance (Note 3)	11.10	reviewnoù raroura		8	Max		pF
POWER REQUIREMENTS	11 (H)	INBEEL MARCHINE					TREMES A
Power Supply Voltage Range		Accuracy is not guaranteed over this range	+5	to +16		-	٧
						1	Mary Commission of the Commiss
		All digital inputs high or low	2.	0/2.5	Max	SAMBI	mA

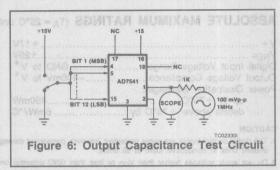
NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, RFEEDBACK.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

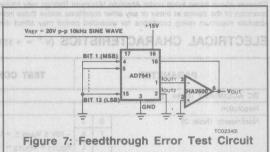
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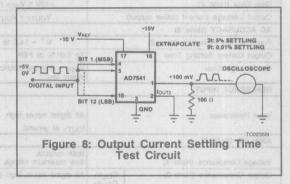












#### **DEFINITION OF TERMS**

**NONLINEARITY:** Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V<sub>REF</sub> range.

**RESOLUTION:** Value of the LSB. For example, a unipolar converter with n bits has a resolution of  $(2^{-n})$  (V<sub>REF</sub>). A bipolar converter of n bits has a resolution of  $[2^{-(n-1)}]$  [V<sub>REF</sub>]. Resolution in no way implies linearity.

**SETTLING TIME:** Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

**FEEDTHROUGH ERROR:** Error caused by capacitive coupling from V<sub>REF</sub> to output with all switches OFF.

6

**BINTERSIL** 

**OUTPUT CAPACITANCE:** Capacity from I<sub>OUT1</sub> and I<sub>OUT2</sub> terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I<sub>OUT1</sub> terminal with all digital inputs LOW or on I<sub>OUT2</sub> terminal when all inputs are HIGH.

#### DETAILED DESCRIPTION OF THE PROPERTY OF THE PR

The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

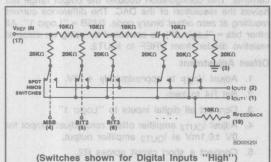
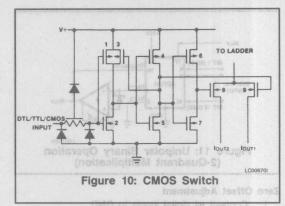


Figure 9: AD7541 Functional Diagram

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 10). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.



#### **APPLICATIONS**

#### **General Recommendations**

Static performance of the AD7541 depends on I<sub>OUT1</sub> and I<sub>OUT2</sub> (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than  $\pm 200\,\mu\text{V}$ ).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V<sup>+</sup> (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or  $V_{\mbox{\scriptsize DD}}$  for proper operation.

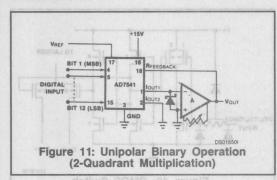
A high value resistor ( $\sim$ 1M $\Omega$ ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

#### UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 11. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents IOUT1 from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

6-19



#### Zero Offset Adjustment

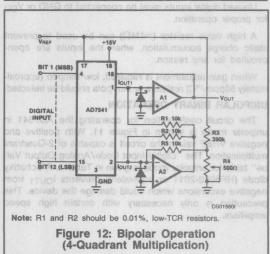
- 1. Connect all digital inputs to GND.
- Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

#### **Gain Adjustment**

- 1. Connect all digital inputs to VDD.
- 2. Monitor VOUT for a -VREF (1-1/212) reading.
- 3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
- To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

Table 1: Code Table — Unipolar Binary
Operation

DIGITAL INPUT	ANALOG OUTPUT
wol e mmmmamam betse	-VREF (1-1/2 <sup>12</sup> ) in primavi
10000000001	-V <sub>REF</sub> (1/2 + 1/2 <sup>12</sup> )
10000000000	-V <sub>REF</sub> /2
01111111111	-V <sub>REF</sub> (1/2 - 1/2 <sup>12</sup> )
00000000001	-V <sub>REF</sub> (1/2 <sup>12</sup> )
00000000000	o eite.



#### BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT2 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

#### Offset Adjustment

- 1. Adjust VRFF to approximately +10V.
- 2. Set R4 to zero.
- 3. Connect all digital inputs to "Logic 1".
- Adjust I<sub>OUT2</sub> amplifier offset zero adjust trimpot for 0V ±0.1mV at I<sub>OUT2</sub> amplifier output.
- 5. Connect a short circuit across R2.
- 6. Connect all digital inputs to "Logic 0".
- Adjust I<sub>OUT2</sub> amplifier offset zero adjust trimpot for 0V ±0.1mV at I<sub>OUT1</sub> amplifier output.
- 8. Remove short circuit across R2.
  - Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
  - 10. Adjust R4 for 0V ±0.2mV at VOUT.

#### Gain Adjustment annual and that are stone to hove to be code.

- 1. Connect all digital inputs to VDD.
- Monitor VOUT for a -VREF (1-1/2<sup>11</sup>) volts reading.
- 3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
- To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

Table 2: Code Table Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	-V <sub>REF</sub> (1-1/2 <sup>11</sup> )
10000000001	
10000000000	O TO TENDE DE TOTAL DE LA COMPANSION DE
also 01111111111111 at a	V <sub>REF</sub> (1/2 <sup>11</sup> )
00000000001	V <sub>REF</sub> (1 - 1/2 <sup>11</sup> )
00000000000	VREF

Figure 13: General DAC Circuit with Compensation Capacitor, CC

#### DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, openloop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.



The output impedance of the AD7541 looking into louT1 varies between 10k $\Omega$  (RFeedback alone) and 5K $\Omega$  (RFeedback) in parallel with the ladder resistance).

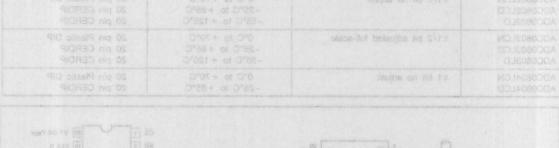
Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

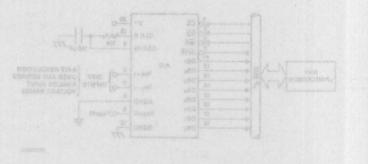
A capacitor in parallel with the feedback resistor (as shown in Figure 13) provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

#### INPUT SIGNAL WARNING

Because of the input protection diodes on the logic inputs, it is important that no voltage greater than 4V outside the logic supply rails be applied to these inputs at any time, including power-up and other transients. To do so could cause destructive SCR latch-up.





(Outline dwg. CD, CN)
Figure 2: Pin
Configuretion

Rouse 1: Typical Application

### ADC0802-ADC0804

### 8-Bit µP-Compatible A/D Converters

#### GENERAL DESCRIPTION

The ADC0802 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

The differential analog voltage input has good commonmode-rejection, and permits offsetting the analog zeroinput-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

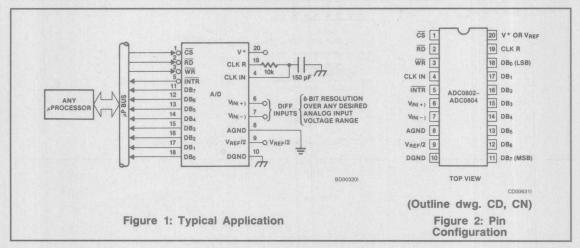


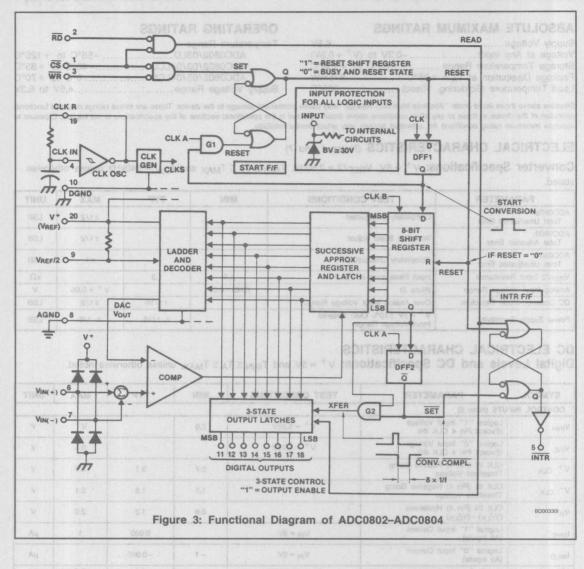
#### **FEATURES**

- 80C48 and 80C80/85 Bus Compatible No Interfacing Logic Required
- Conversion Time  $< 100 \mu s$
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode Differential Analog Voltage Inputs
- Works With Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator • 0V to 5V Analog Voltage Input Range (Single +5V Supply)
- No Zero-Adjust Required

#### ORDERING INFORMATION

PART	questal ROP evi ERROR eviso bluso	TEMPERATURE RANGE	PACKAGE DUOTS TO HIGHE
ADC0802LCN	±1/2 bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0802LCD		-25°C to +85°C	20 pin CERDIP
ADC0802LD		-55°C to +125°C	20 pin CERDIP
ADC0803LCN	±1/2 bit adjusted full-scale	0°C to +70°C	20 pin Plastic DIP
ADC0803LCD		-25°C to +85°C	20 pin CERDIP
ADC0803LD		-55°C to +125°C	20 pin CERDIP
ADC0804LCN	±1 bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0804LCD		-25°C to +85°C	20 pin CERDIP





voltage at Any input0.3V to (V ' +0.3V)	ADC0802/03LD
Storage Temperature Range65°C to +150°C	ADC0802/03/04
Package Dissipation at T <sub>A</sub> = +25°C875mW	ADC0802/03/04
Lead Temperature (Soldering, 10sec) 300°C	Supply Voltage Range

	ADC080	2/03LD	55°C to +125°C
	ADC080	2/03/04LCD	40°C to +85°C
	ADC080	2/03/04LCN	0°C to +70°C
ply	Voltage	Range	4.5V to 6.3V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications:  $V^+ = 5V$ ,  $V_{REF}/2 = 2.500V$ ,  $T_{MIN} \le T_A \le T_{MAX}$  and  $f_{CLK} = 640kHz$  unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC0802: Total Unadjusted Error	Completely Unadjusted			±1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted		ANG ANG	±1 0	LSB
V <sub>REF</sub> /2 Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND - 0.05		V + + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	V <sup>+</sup> = 5V ±10% Over Allowed Input Voltage Range		± 1/16	± 1/8	LSB

## DC ELECTRICAL CHARACTERISTICS Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \le T_A \le T_{MAX}$ , unless otherwise noted.

		The second of th			ARL ARL		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
CONTROL IN	PUTS (Note 6)	HTATES					
VINH &	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V <sup>+</sup> = 5.25V	2.0		V+	V	
VINL 08	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V + = 4.75V	o n		0.8	V	
V <sup>+</sup> CLK	CLK IN (Pin 4) Positive Going Threshold Voltage	SEGNAL OUTPUTS	2.7	3.1	3.5	٧	
V- CLK	CLK IN (Pin 4) Negative Going Threshold Voltage	3 IQARS TUSTUCES	1.5	1.8	2.1	V	
VH	CLK IN (Pin 4) Hysteresis (VCLK) – (VCLK)	DOA to exemple 'scolor	0.6	1.3	2.0	V	
I <sub>INHI</sub>	Logical "1" Input Current (All Inputs)	V <sub>IN</sub> = 5V		0.005	1	μА	
INLO	Logical "0" Input Current (All Inputs)	V <sub>IN</sub> = 0V	-1	-0.005		μΑ	
(*	Supply Current (Includes Ladder Current)	$f_{CLK} = 640 \text{kHz},$ $T_A = +25^{\circ}\text{C} \text{ and } \overline{\text{CS}} = \text{HI}$		1.3	2.5	mA	
DATA OUTPL	JTS AND INTR					T. Blak	
VoL	Logical "0" Output Voltage	I <sub>O</sub> = 1.6mA V + = 4.75V			0.4	V	
VoH	Logical ''1'' Output Voltage	$I_0 = -360 \mu A$ V + = 4.75V	2.4			V	
lLO	3-State Disabled Output Leakage (All Data Buffers)	V <sub>OUT</sub> = 0V V <sub>OUT</sub> = 5V	-3		3	μΑ μΑ	
						-	

6

NOTES: 1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

For  $V_{|N(-)} \ge V_{|N(+)}$  the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the  $V^+$  supply. Be careful, during testing at low  $V^+$  levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog  $V_{|N|}$  does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading. With V+ = 6V, the digital logic interfaces are no longer TTL compatible.

With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

The CS input is assumed to bracket the WR strobe input so that timing is dependent on the WR pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the WR pulse (see Timing Diagrams).

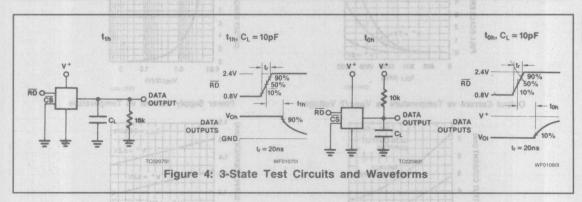
CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.

None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the  $V_{IN(-)}$  input can be adjusted to achieve this. See **Zero** Error on page 10 of this data sheet.

#### AC ELECTRICAL CHARACTERISTICS

Timing Specifications: V + = 5V and TA = +25°C unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fCLK	Clock Frequency	V <sup>+</sup> = 6V (Note 3) V <sup>+</sup> = 5V	100 100	640 640	1280 800	kHz kHz
tconv	Clock Periods per Conversion (Note 4)		62		73	
CR	Conversion Rate In Free-Running Mode	INTR tied to WR with CS = 0V, f <sub>CLK</sub> = 640kHz		, 100	8888	conv/s
tw(WR)I	Width of WR Input (Start Pulse Width)	CS = 0V (Note 5)	100	r S	E 865 S	ns
tacc	Access Time (Delay from Falling Edge of RD to Output Data Valid)	C <sub>L</sub> = 100pF (Use Bus Driver IC for Larger C <sub>L</sub> )	4.50 4.70 9 S	135	200	ns
t <sub>1h</sub> , t <sub>0h</sub>	3-State Control (Delay from Rising Edge of RD to HI-Z State)	C <sub>L</sub> = 10pF, R <sub>L</sub> = 10k (See 3-State Test Circuits)	R also D.I	125	250	ns
twi, t <sub>RI</sub>	Delay from Falling Edge of WR to Reset of INTR			300	450	ns
CIN	Input Capacitance of Logic Control Inputs	A Property of the Park of the		5	7.5	pF
Cour	3-State Output Capacitance (Data Buffers)			5	7.5	pF

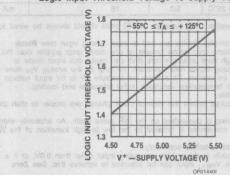


### ADC0802-ADC0804

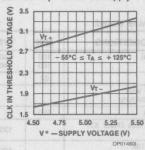
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### TYPICAL PERFORMANCE CHARACTERISTICS (100) SOLTERSTOARAHO JADINTOSUS OC

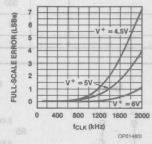
Logic Input Threshold Voltage vs Supply Voltage



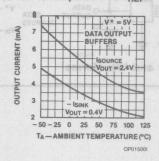
**CLK IN Schmitt Trip Levels vs Supply Voltage** 



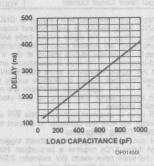
Full-Scale Error vs FCLK



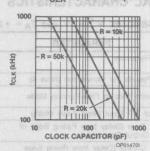
Output Current vs Temperature vs V<sub>REF</sub>/2 Voltage



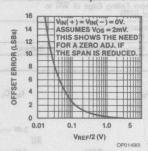
Delay From Falling Edge of RD to Output Data Valid vs Load Capacitance



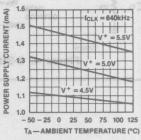
fCLK vs Clock Capacitor

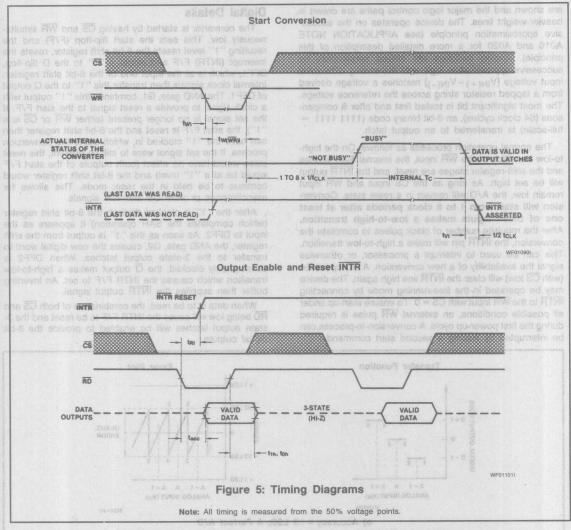


Effect of Unadjusted Offset Error



Power Supply Current vs Temperature





#### UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 6a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1LSB (19.53mV with 2.5V tied to the  $V_{\rm REF}/2$  pin). The digital output codes which correspond to these inputs are shown as D – 1, D, and D + 1. For the perfect A/D, not only will center-value (A – 1,A,A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located  $\pm\,^1\!\!/_2$  LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend  $\pm\,^1\!\!/_2$  LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1LSB wide.

The error curve of Figure 6b shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 6a is + ½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1LSB in magnitude, unless the device has missing codes.

#### **FUNCTIONAL DESCRIPTION**

A functional diagram of the ADC0802 series of A/D converters is shown in Figure 3. All of the package pinouts

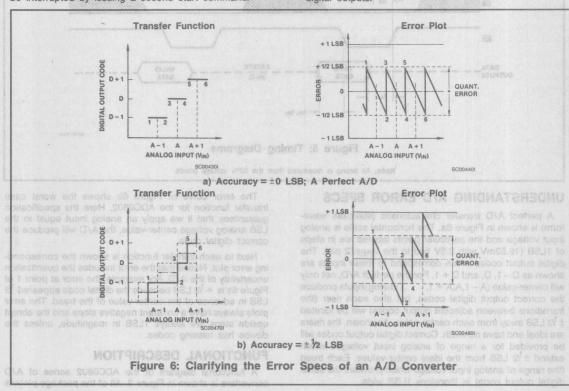
sive approximation principle (see APPLICATION NOTE A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage  $[V_{IN(+)} - V_{IN(-)}]$  matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the highto-low transition of the WR input, the internal SAR latches and the shift-register stages are reset, and the INTR output will be set high. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition. After the requisite number of clock pulses to complete the conversion, the INTR pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A RD operation (with CS low) will clear the INTR line high again. The device may be operated in the free-running mode by connecting INTR to the WR input with CS = 0. To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

neously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either WR or CS is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide CS and WR signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the  $\overline{\rm Q}$  output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the  $\overline{\rm INTR}$  output signal.

When data is to be read, the combination of both  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.



6

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the onchip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the  $V_{IN(+)}$  input and leaving the  $V_{IN(-)}$  input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and **do not inherently cause errors** as the on-chip comparator is strobed at the end of the clock period.

### **Analog Operation**

RD input (pin 2).

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between  $V_{\rm IN}(+)$  and  $V_{\rm IN}(-)$ , while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by 1/2 LSB (see Figure 6a).

The digital control inputs (CS, RD, and WR) meet

standard TTL logic voltage levels. These signals are

essentially equivalent to the standard A/D Start and Output

Enable control signals, and are active low to allow an easy

interface to microprocessor control busses. For non-micro-

processor based applications, the CS input (pin 1) can be

grounded and the standard A/D Start function obtained by

an active low pulse at the WR input (pin 3). The Output

Enable function is achieved by an active low pulse at the

### Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The V<sub>IN(-)</sub> input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA-20mA current loop conversion. In addition, commonmode noise can be reduced by use of the differential input.

The time interval between sampling  $V_{IN(+)}$  and  $V_{IN(-)}$  is  $4^{1/2}$  clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_{\Theta}(MAX) = (V_{p})(2\pi f_{cm}) \left[ \frac{4.5}{f_{CLK}} \right]$$

where:

 $\Delta V_{e}$  is the error voltage due to sampling delay  $V_{P}$  is the peak value of the common-mode voltage  $f_{cm}$  is the common-mode frequency

For example, with a 60Hz common-mode frequency, f<sub>cm</sub>, and a 640kHz A/D clock, f<sub>CLK</sub>, keeping this error to ½ LSB (~5mV) would allow a common-mode voltage, V<sub>P</sub>, given by:

$$V_{p} = \frac{[\Delta V_{e}(MAX)(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_p = \frac{(5 \times 10^{-3}) (640 \times 10^3)}{(6.28) (60) (4.5)} \approx 1.9V$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see Reference Voltage Span Adjust).

#### **Input Bypass Capacitors**

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the VIN(+) input voltage at full-scale. For a 640kHz clock frequency with the VIN(+) input at 5V, this DC current is at a maximum of approximately 5µA. Therefore, bypass capacitors should not be used at the analog inputs or the VRFF/2 pin for high resistance sources ( $> 1 \text{k}\Omega$ ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance. due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

#### Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, will not cause errors since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor ( $\leq 1 \mathrm{k}\Omega$ ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, ( $\leq 1 \mathrm{k}\Omega$ ), a  $0.1 \mu\mathrm{F}$  bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A  $100\Omega$  series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

#### Stray Pickup

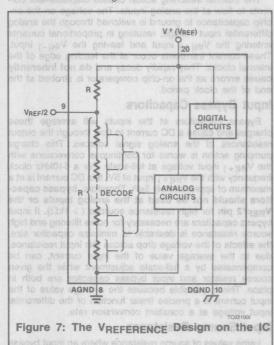
The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below  $5k\Omega$ . Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capcitors will average the transient input switching currents of the A/D (see Analog Input Current). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a fullscale adjustment of the A/D (see Full-Scale Adjustment) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

### Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted

## ADC0802-ADC0804

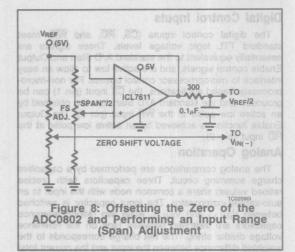
voltage reference. This has been achieved in the design of the IC as shown in Figure 7.

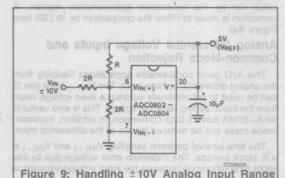


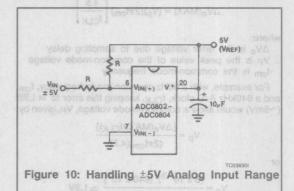
Notice that the reference voltage for the IC is either \$^{1}\!\!/2\$ of the voltage which is applied to the V  $^{+}$  supply pin, or is equal to the voltage which is externally forced at the VREF/2 pin. This allows for a pseudo-ratiometric voltage reference using, for the V  $^{+}$  supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the VREF/2 input. The internal gain to the VREF/2 input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the  $V_{\text{IN}(-)}$  pin to absorb the offset, the reference voltage can be made equal to  $\frac{1}{2}$  of the 3V span or 1.5V. The A/D now will encode the  $V_{\text{IN}(+)}$  signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 8. For expanded scale inputs, the circuits of Figures 9 and 10 can be used.









#### Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the

reference voltage are important accuracy factors in the operation of the A/D converter. For  $V_{\rm REF}/2$  voltages of 2.5V nominal value, initial errors of  $\pm 10 {\rm mV}$  will cause conversion errors of  $\pm 1{\rm LSB}$  due to the gain of 2 of the  $V_{\rm REF}/2$  input. In reduced span applications, the initial value and the stability of the  $V_{\rm REF}/2$  input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1LSB at the  $V_{\rm REF}/2$  input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source,

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

#### Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value,  $V_{IN(MIN)}$ , is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D  $V_{IN(-)}$  input at this  $V_{IN(MIN)}$  value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the  $V_{\rm IN(-)}$  input and applying a small magnitude positive voltage to the  $V_{\rm IN(+)}$  input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for  $V_{\rm REF}/2 = 2.500V$ ).

#### **Full-Scale Adjust**

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting

the magnitude of the V<sub>REF</sub>/2 input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted V<sub>REF</sub>/2 voltage, the full-scale adjustment is made by inputting V<sub>MIN</sub> to the V<sub>IN(-)</sub> input of the A/D and applying a voltage to the V<sub>IN(+)</sub> input which is given by:

$$V_{\text{IN(+)}}\text{fsadj} = V_{\text{MAX}} - 1.5 \left[ \frac{(V_{\text{MAX}} - V_{\text{MIN}})}{256} \right]$$

where:

 $V_{MAX}$  = the high end of the analog input range and

V<sub>MIN</sub> = the low end (the offset zero) of the analog range. (Both are ground referenced.)

#### **Clocking Option**

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 11.

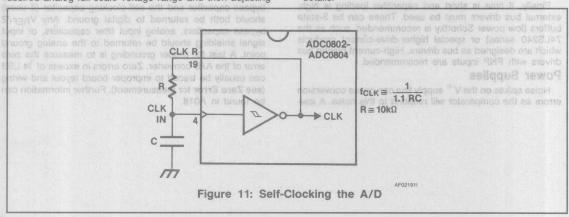
Heavy capacitive or DC loading of the CLock R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

#### Restart During a Conversion of about 18009

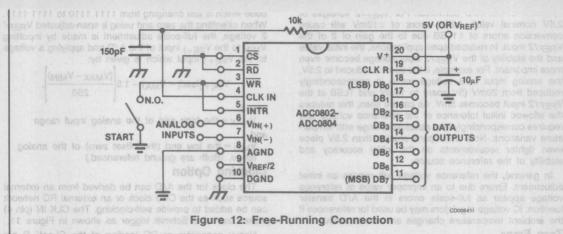
If the A/D is restarted (CS and WR go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

# Continuous Conversions

In this application, the  $\overline{\text{CS}}$  input is grounded and the  $\overline{\text{WR}}$  input is tied to the  $\overline{\text{INTR}}$  output. This  $\overline{\text{WR}}$  and  $\overline{\text{INTR}}$  node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 12 for details.







#### Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see Typical Performance Characteristics).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

#### **Power Supplies**

Noise spikes on the V + supply line can cause conversion errors as the comparator will respond to this noise. A low-

inductance tantalum filter capacitor should be used close to the converter V  $^+$  pin, and values of  $1\mu F$  or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V  $^+$  supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

#### Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any V<sub>REF</sub>/2 bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ½ LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in A018.

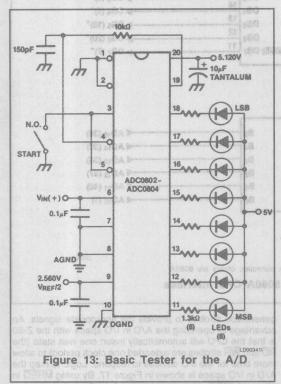
## ADC0802-ADC0804

#### TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 13.

For ease of testing, the V<sub>REF</sub>/2 (pin 9) should be supplied with 2.560V and a V supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V ( $5.120-1^{1/2}$  LSB) should be applied to the  $V_{\rm IN(+)}$  pin with the  $V_{\rm IN(-)}$  pin grounded. The value of the  $V_{\rm REF}/2$  input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of  $V_{\rm REF}/2$  should then be used for all the tests.



The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right) (5.12)V.$$

MODERS IL

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 14 and 15 show more sophisticated test circuits.

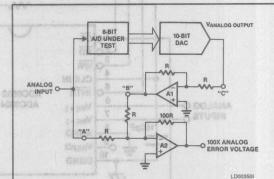
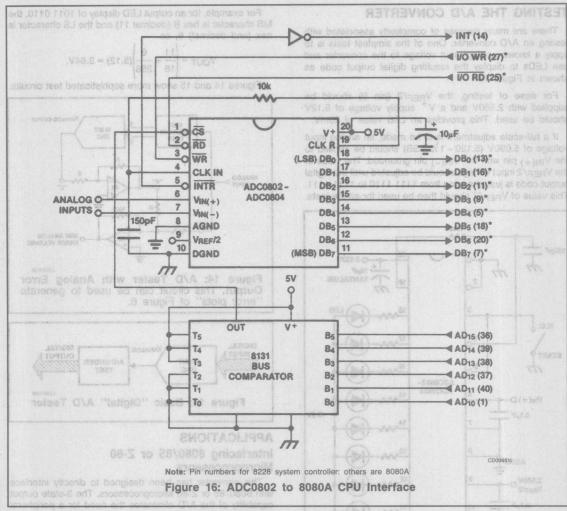


Figure 14: A/D Tester with Analog Error Output. This circuit can be used to generate "error plots" of Figure 6.

# APPLICATIONS Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate CS for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for  $\overline{\text{CS}}$  and the  $\overline{\text{MEMR}}$  and  $\overline{\text{MEMW}}$ strobes) or it can be controlled as an I/O device by using the I/O R and I/O W strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the CS input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 16.



The standard control-bus signals of the 8080 (CS, RD and WR) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs, one for each I/O device. Degam-yoursens to not assuable

#### Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General RD and WR strobes are provided and separate memory request, MREQ, and I/O request, IORQ, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the RD and WR strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 17. By using MREQ in place of IORQ, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized RD and WR strobe, with an IO/M line to distinguish I/O and memory requests. The circuit of Figure 17 can again be used, with IO/M in place of IORQ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide IO/M for an I/O-mapped connection.

# Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  strobe signals. Instead it employs a single  $R/\overline{W}$  line and additional timing, if needed, can be derived from the  $\phi2$  clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 16 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the  $\overline{\text{CS}}$  decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded  $\overline{\text{475}}$  line is brought out to the common bus at pin 21. This can be tied directly to the  $\overline{\text{CS}}$  pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 19 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the  $\overline{CS}$  pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no  $\overline{CS}$  decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D  $\overline{RD}$  pin can be grounded.

#### **APPLICATION NOTES**

Some applications bulletins that may be found useful are

A016 "Selecting A/D Converters," by Dave Fullagar.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed

A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

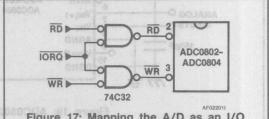
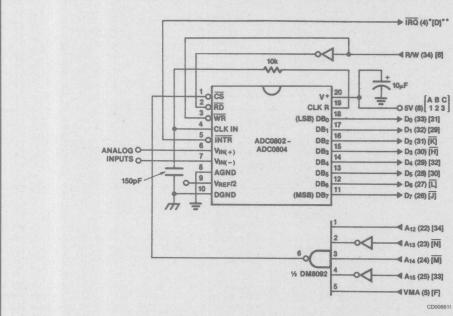


Figure 17: Mapping the A/D as an I/O device for use with the Z-80 CPU

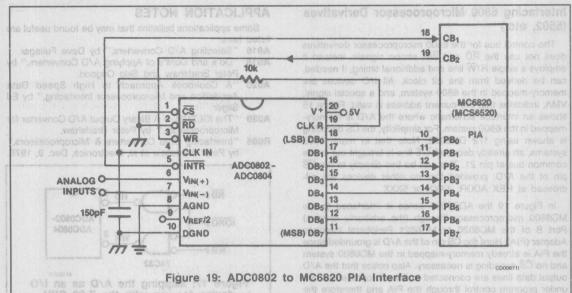


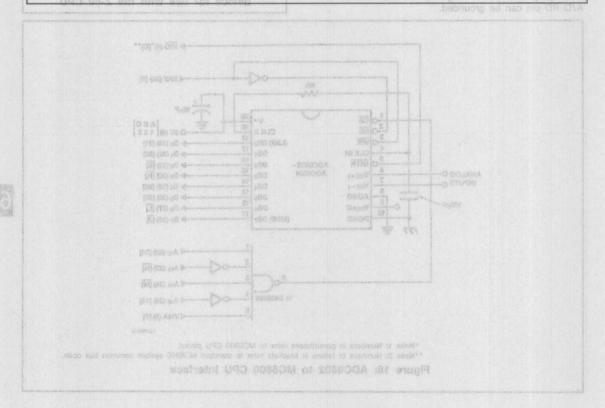
\*Note 1: Numbers in parentheses refer to MC6800 CPU pinout.

\*\*Note 2: Numbers or letters in brackets refer to standard MC6800 system common bus code.

Figure 18: ADC0802 to MC6800 CPU Interface







#### GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3 <sup>1</sup>/<sub>2</sub>-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, a reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

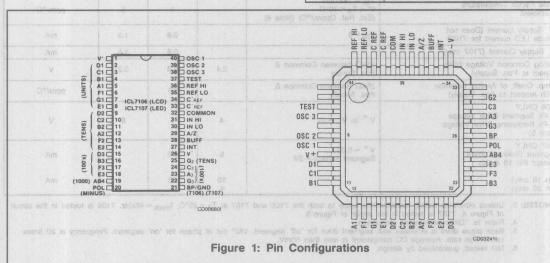
The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than  $10\mu V$ , zero drift of less than  $1\mu V/^{\circ} C$ , input bias current of 10 pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. Finally, the true economy of single power supply operation (7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

#### **FEATURES**

- Guaranteed Zero Reading for 0 Volts Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- 9 True Differential Input and Reference
- Direct Display Drive No External Components
   Required LCD ICL7106
   LED ICL7107
- Low Noise-Less Than 15μV p-p
- On-Chip Clock and Reference
- Low Power Dissipation-Typically Less Than 10mW
- No Additional Active Circuits Required
- New Small Outline Surface Mount Package
   Available
- Evaluation Kit Available

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7106CDL	0°C to +70°C	40 pin ceramic DIP
ICL7106CPL	0°C to +70°C	40 pin plastic DIP
ICL7106CJL	0°C to +70°C	40 pin CERDIP
ICL7106CM44	0°C to +70°C	44 pin Surface Mount
ICL7107CJL	0°C to +70°C	40 pin CERDIP
ICL7107CDL	0°C to +70°C	40 pin ceramic DIP
ICL7107CPL	0°C to +70°C	40 pin plastic DIP
ICL7106EV/Kit ICL7107EV/Kit		tain IC, display, circuit



# ICL7106/ICL7107



#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage
ICL7106, V + to V 15V
ICL7107, V + to GND +6V
ICL7107, V - to GND9V
Analog Input Voltage (either input)(Note 1) V + to V
Reference Input Voltage (either input)V to V
Clock Input Hold estated not creat to withing out?
ICL7106TEST to V +
ICI 7107 GND to V +

Power Dissipation (Note 2)	
Ceramic Package	
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature6	35°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C
n a single CMOS LC. Included are seven-	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100 µA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

#### **ELECTRICAL CHARACTERISTICS** (Note 3)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT IS IN
Zero Input Reading	V <sub>IN</sub> = 0.0V Full Scale = 200.0mV	- 000.0	±000.0	+ 000.0	Digital Reading
Ratiometric Reading MOTAMED 3M	V <sub>IN</sub> = V <sub>REF</sub> V <sub>REF</sub> = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	$-V_{\text{IN}} = +V_{\text{IN}} \simeq 200.0 \text{mV}$	splay. -1	±.2	#1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200.0mV or full scale = 2.000V (Note 6)	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V <sub>CM</sub> = ±1V, V <sub>IN</sub> = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V <sub>IN</sub> = 0V Full Scale = 200.0mV		15		μV
Leakage Current Input	V <sub>IN</sub> = 0 (Note 6)		1	10	pA
Zero Reading Drift Of nichood and nothering	V <sub>IN</sub> = 0 0° < T <sub>A</sub> < 70°C (Note 6)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V <sub>IN</sub> = 199.0mV 0° < T <sub>A</sub> < 70°C (Ext. Ref. Oppm/°C) (Note 6)		1	5	ppm/°C
V <sup>+</sup> Supply Current (Does not include LED current for 7107)	V <sub>IN</sub> = 0		0.8	1.8	mA
V Supply Current (7107 only)	SAT THE RESERVE		0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	٧
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	0.2	80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	V+ to V-=9V	4 6	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19 & 20)	V + = 5.0V Segment voltage = 3V	5	8.0	# 10 H	mA
(Pin 19 only) (Pin 20 only)	少年電	10 4	16 7	#1518 #1518 #1518	s geods mA

NÔTES: 3. Unless otherwise noted, specifications apply to both the 7106 and 7107 at TA = 25°C, f<sub>clock</sub> = 48kHz. 7106 is tested in the circuit of Figure 4. 7107 is tested in the circuit of Figure 5.

Refer to "Differential Input" discussion.

Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
 Not tested, guaranteed by design.

## TEST CIRCUITS as agreed of riguette egist at it terft

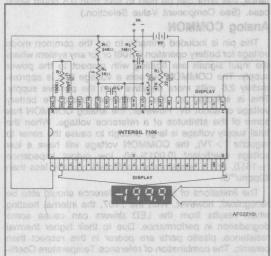
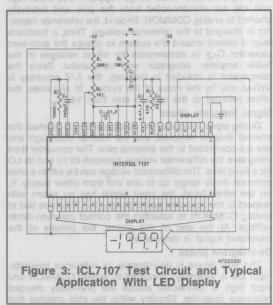
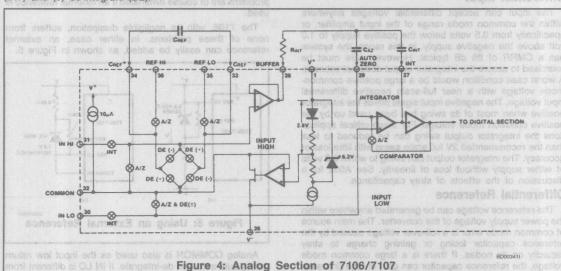


Figure 2: ICL7106 Test Circuit and Typical Application With Liquid Crystal Display

# DETAILED DESCRIPTION A NAW 2801/90 Analog Section

Figure 4 shows the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).





shorred to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor  $c_{AZ}$  to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10\,\mu\text{V}$ .

#### Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to one volt from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

#### De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$1000 \left( \frac{V_{IN}}{V_{REF}} \right)$$

#### **Differential Input**

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range, the system has a CMRR of 86 dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive commonmode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

#### **Differential Reference**

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over

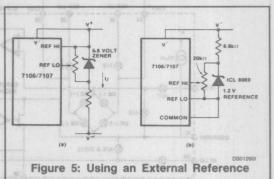
case. (See Component Value Selection.)

#### Analog COMMON

voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance ( $\simeq$ 15 $\Omega$ ), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 µV to 80µVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overrange condition. This is because overrange is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overrange and a nonoverrange count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.



Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for

instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 30mA of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only  $10\mu A$  of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

#### TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a  $500\Omega$  resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 8 and 9 show such an application. No more than a 1mA load should be applied.

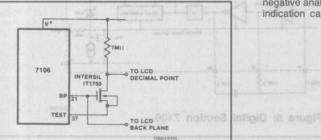
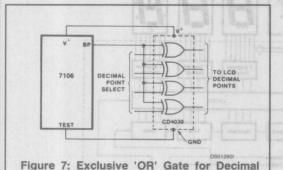


Figure 6: Simple Inverter for Fixed Decimal Point



The second function is a "lamp test". When TEST is pulled high (to V +) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Point Drive

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

#### DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

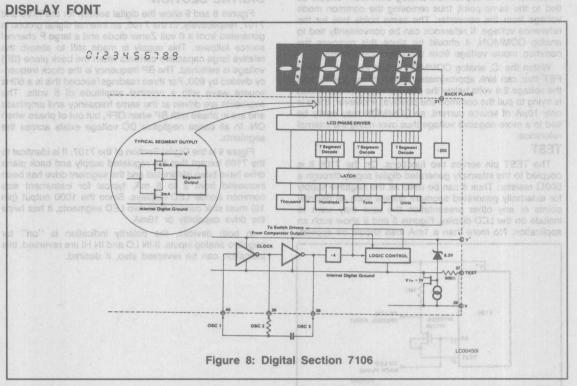
Figure 9 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

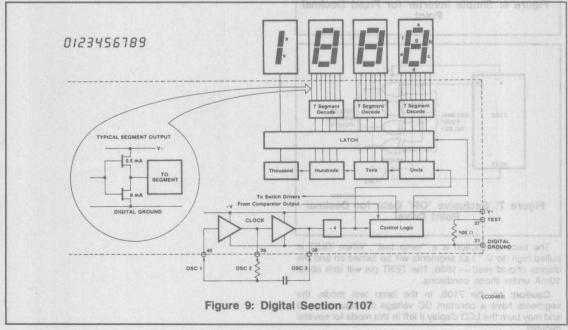
In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

6

# ICL7106/ICL7107

# 

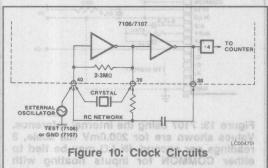




#### System Timing

Figure 10 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

- 1. An external oscillator connected to pin 40.
- 2. A crystal between pins 39 and 40.
- 3. An R-C oscillator using all three pins.



The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 662/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

# COMPONENT VALUE SELECTION Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with  $100\mu A$  of quiescent current. They can supply  $20\mu A$  of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale,  $470k\Omega$  is near optimum and similarly a  $47k\Omega$  for a 200.0 mV scale.

#### Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal  $\pm 2$  volt full scale integrator swing is fine. For the 7107 with  $\pm 5$  volt supplies and analog COMMON tied to supply ground, a  $\pm 3.5$  to  $\pm 4$  volt swing is nominal. For three readings/second (48kHz clock) nominal values for  $C_{\rm INT}$  are  $0.22\mu{\rm F}$  and

0.10 µF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent rollover errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

#### **Auto-Zero Capacitor**

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a  $0.47\mu\text{F}$  capacitor is recommended. On the 2 volt scale, a  $0.047\mu\text{F}$  capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

#### Reference Capacitor solling betoeles in tost in

A  $0.1\mu F$  capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally  $1.0\mu F$  will hold the roll-over error to 0.5 count in this instance.

## Oscillator Components TAOLIGGA LIAOIGYT

For all ranges of frequency a  $100 k\Omega$  resistor is recommended and the capacitor is selected from the equation  $f = \frac{0.45}{RC}$ . For 48kHz clock (3 readings/second), C = 100pF.

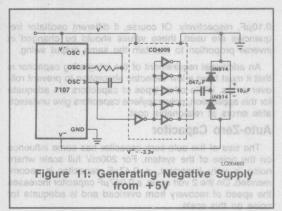
#### Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: VIN = 2VRFF. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select VRFF = 0.341V. Suitable values for integrating resistor and capacitor would be  $120k\Omega$  and 0.22 µF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for VIN = 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

### 7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

# ICL7106/ICL7107



In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the common mode range of the converter.
- 2. The signal is less than ±1.5 volts.
  - 3. An external reference is used.

#### TYPICAL APPLICATIONS TO THE STATE OF THE STA

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

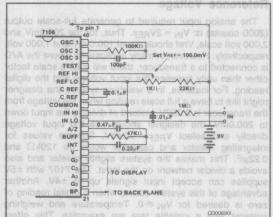


Figure 12: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

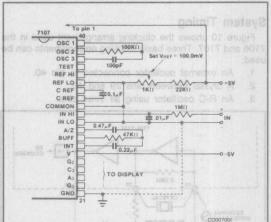


Figure 13: 7107 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

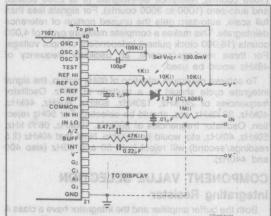


Figure 14: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

scale integrator swing is fine. For the 7107 with ±5 volt

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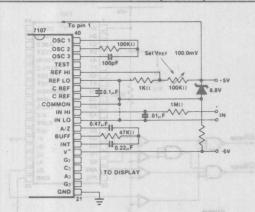


Figure 15: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 15, IN LO may be tied to either COMMON or GND.

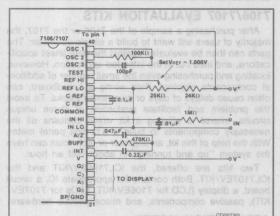


Figure 16: 7106/7107: Recommended component values for 2.000V full scale.

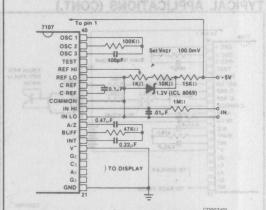


Figure 17: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V<sup>+</sup> and V<sup>-</sup> is insufficient for correct operation of the internal reference.

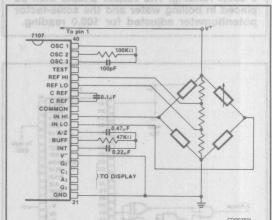


Figure 18: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

Figure 20: Circuit for developing Underrange

# ICL7106/ICL7107

# **BINTERSIL**

#### TYPICAL APPLICATIONS (CONT.)

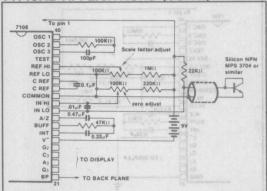


Figure 19: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

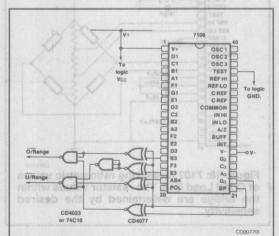


Figure 20: Circuit for developing Underrange and Overrange signals from 7106 outputs.

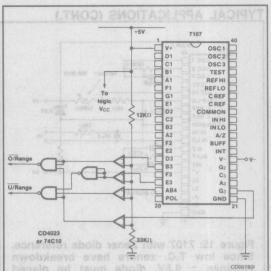


Figure 21: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

#### 7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

#### APPLICATION NOTES

- A016 "Selecting A/D Converters", by David Fullagar.
- A017 "The Integrating A/D Converter", By Lee Evans.
- A018 "Do's and Don'ts of Applying A/D Converters", by
  - Peter Bradshaw and Skip Osgood.
- A019 ''4½-Digit Panel Meter Demonstrator/ Instrumentation Boards'', by Michael Dufort.
- A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
- A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

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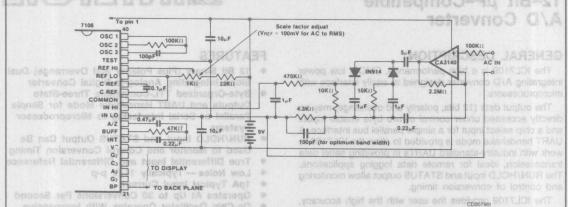


Figure 22: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

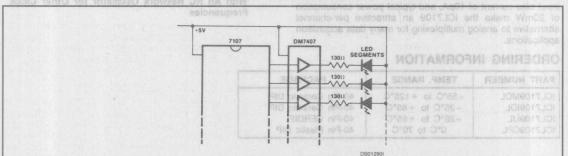
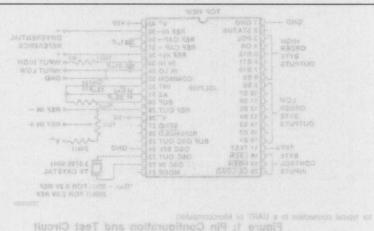


Figure 23: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.



# **ICL7109**12-Bit μP-Compatible A/D Converter



#### GENERAL DESCRIPTION

The ICL7109 is a high performance, CMOS, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

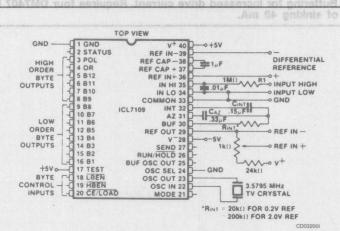
The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1µV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

#### **FEATURES**

- 12 Bit Binary (Plus Polarity and Overrange) Dual Slope Integrating Analog-to-Digital Converter
- Byte-Organized TTL-Compatible Three-State
   Outputs and UART Handshake Mode for Simple
   Parallel or Serial Interfacing to Microprocessor
   Systems
- RUN/HOLD Input and STATUS Output Can Be Used to Monitor and Control Conversion Timing
- True Differential Input and Differential Reference
- Low Noise Typically 15μV p-p
- 1pA Typical Input Current
- Operates At Up to 30 Conversions Per Second
- On-Chip Oscillator Operates With Inexpensive 3.58MHz TV Crystal Giving 7.5 Conversions Per Second for 60Hz Rejection May Also Be Used With An RC Network Oscillator for Other Clock Frequencies

#### ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7109MDL	-55°C to +125°C	40-Pin Ceramic DIP
ICL7109IDL	-25°C to +85°C	40-Pin Ceramic DIP
ICL7109IJL	-25°C to +85°C	40-Pin CERDIP
ICL7109CPL	0°C to 70°C	40-Pin Plastic DIP



(See Figure 2 for typical connection to a UART or Microcomputer)

Figure 1: Pin Configuration and Test Circuit

#### ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V+)		+6.2V
Negative Supply Voltage (GND to V-)		9V
Analog Input Voltage (Lo or Hi) (Note 1).	V+	to V
Reference Input Voltage (Lo or Hi) (Note	1)V+	to V
Digital Input Voltage		+0.31
(Pins 2-27) (Note 2)	GND	-0.3V

Power Dissipation (Note 3)  Ceramic Package	1W @ +85°C
Plastic Package	500mw @ + 70°C
Operating Temperature	
Ceramic Package (MDL)	55°C to +125°C
Ceramic Package (IDL)	25°C to +85°C
Plastic Package (CPL)	0°C to +70°C
Storage Temperature	65°C to +150°C

Lead Temperature (Soldering, 10sec) ......+300°C

ELECTRICAL CHARACTERISTICS (CONT.)

# **ELECTRICAL CHARACTERISTICS** ( $V^+ = +5V$ , $V^- = -5V$ , GND = 0V, $T_A = 25$ °C, unless otherwise indicated.) Test circuit as shown on first page of this data sheet.

#### ANALOG SECTION

SYMBOL	PARAMETER	Rora	TEST CONDITIONS	-Pin	MINE	TYP	MAX	UNIT
	Zero Input Reading	108	V <sub>IN</sub> = 0.0V Full Scale = 409.6mV	котте	Commission Accounts their	±00008	+00008	Octal Reading
(Pm 21) low wto K enable.	Ratiometric Reading	CI/	V <sub>IN</sub> = V <sub>REF</sub> V <sub>REF</sub> = 204.8mV	ntuler limit	37778	3777 <sub>8</sub> 4000 <sub>8</sub>	40008	Octal Reading
and andors	Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 4), (Note 6)	grate and d ed. og seetion is	lata es latol		+1	Counts
nske mode.	Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 2.048V (Note 5), (Note 6)		for Positiv		+1	Counts
CMRR	Common Mode Rejection Ratio		V <sub>CM</sub> ±1V V <sub>IN</sub> = 0V Full Scale = 409.6mV	(HE trus	lost Signific	50		μ\/\
VCMR	Input Common Mode Range		Input Hi, Input Lo, Common (Note	e 4)	V-+1.5	71 100	V + -1.0	V
en stab to h	Noise (p-p value not exceeded 95% of time)		V <sub>IN</sub> = 0V Full Scale = 409.6mV			15 <sub>8 M8</sub>		ggμV g
TILK Details of	Leakage current at Input		$V_{IN} = 0$ All devices at 25°C ICL7109CPL 0°C $\leq$ T <sub>A</sub> $\leq$ +70°C (ICL7109IDL $-25$ °C $\leq$ T <sub>A</sub> $\leq$ +85°C ICL7109MDL $-55$ °C $\leq$ T <sub>A</sub> $\leq$ +125°C	(Note 4)	01/H = 1	1 20 100 2	10 100 250 5	pA pA pA nA
	Zero Reading Drift		$V_{IN} = 0V R_1 = 0\Omega$ (Note 4)	32.00		0.2	1	μV/°C
nilgures	Scale Factor Temperature Coefficient	T	V <sub>IN</sub> = 408.9mV = > 7770 <sub>8</sub> reading Ext. Ref. 0 ppm/°C (Note 4)			1 8 ns	5	ppm/°C
I + bos bestio	Supply Current V <sup>+</sup> to GND		V <sub>IN</sub> = 0, Crystal Osc 3.58MHz test circuit	(NB) free:	ingil tess	700	1500	18µA <sub>8</sub>
ISUPP	Supply Current V to V	5.54	Pins 2-21, 25, 26, 27, 29; open		) Innmolf -	700	1500	μΑ
V <sub>REF</sub>	Ref Out Voltage		Referred to V <sup>+</sup> , 25kΩ between V <sup>+</sup> and REF OUT	d for test or	-2.4	-2.8	-3.2	٧
	Ref Out Temp. Coefficient	44	25kΩ between V + and REF OU	In about a	NV birtes	80		ppm/°C

#### DIGITAL SECTION

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH of ot of	Output High Voltage	I <sub>OUT</sub> = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
VOL	Output Low Voltage	IOUT = 1.6mA wol (15 nig) ebaM ni	W alden	0.2	0.4	BBH V 41
VP = veno	Output Leakage Current	Pins 3-16 high impedance	s. high did	±.01	±1	μΑ
MAS vitánio	Control I/O Pullup Current	Pins 18, 19, 20 V <sub>OUT</sub> = V <sup>+</sup> -3V MODE input at GND	OR.	812 POL		μА
	Control I/O Loading	HBEN Pin 19 LBEN Pin 18	trs near ou	dold a se	50	pF
VIH	Input High Voltage	Pins 18-21, 26, 27 referred to GND	2.5	mode. See		V
VIL	Input Low Voltage	Pins 18-21, 26, 27 referred to GND			1	V

<sup>\*</sup>COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	PARAMETER Input Pull-up Current Input Pull-up Current		TEST CONDITIONS	MIN	TYP	MAX	UNIT
970 - 6: 10			Pins 26, 27 V <sub>OUT</sub> = V + -3V	7 01 G	5	HOV YEAR	μΑ μΑ
POT A B. W			Pins 17, 24 V <sub>OUT</sub> = V + -3V	RADAS VILLE	25		
	Input Pull-down Current	terooms	Pin 21 VOUT = GND +3V	0. (thi to	5	nV tuoni	μА
Оон	Octillator Output	High	V <sub>OUT</sub> = 2.5V		1	ostlov tu	mA
OoL O	Current (JOI) equal	Low	V <sub>OUT</sub> = 2.5V		1.5	S eroW) (	S-SmA
ВООН	Buffered Oscillator	High	V <sub>OUT</sub> = 2.5V		2	H THE R	mA
BOOL	Output Current	Low	V <sub>OUT</sub> = 2.5V		5		mA
tw	MODE Input Pulse Width	enuisi	(Note 4)	50			ns

- NOTES: 1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA

  2. Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V<sup>+</sup> or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

  3. This limit refers to that of the package and will not be obtained during normal operation.

  4. This parameter is not production tested, but is guaranteed by design.

  5. Roll-over error for T<sub>A</sub> = -55°C to +125°C is ±3 counts maximum.

  6. A full scale voltage of 2.048V is used because a full scale voltage of 4.096V exceeds the devices Common Mode Voltage Range.

#### TABLE 1: — Pin Assignment and Function Description

PIN	SYMBOL	-80000s	DESCRIPTION		
1 <sub>ist</sub>	GND		Digital Ground, 0V. Ground return for all digital logic.		
2	STATUS				
3	POL	Polarity -	- HI for Positive input.	V849.S of	
4	OR	Overrange	e — HI if Overranged.		
5	B12	Bit 12	(Most Significant Bit)		
6	B11	Bit 11	8 7 + "W (8 9		
7	B10	Bit 10	10.77	All	
8	B9	Bit 9		three	
9	B8 01	Bit 8		state	
10	B7	Bit 7	HI = true (4 stol4	output	
11	B6	Bit 6	The succession	data	
12	B5	Bit 5		bits	
13	B4	Bit 4		704	
14	B3	Bit 3			
15	B2	Bit 2		(\$ absi	
16	B1 00001	Bit 1	(Least Significant Bit)		
17	TEST 0081	Note: Thi	h — Normal Operation. v — Forces all bit outputs s input is used for test pu high if not used.	high. urposes	
18	LBEN	and CE/L	Enable — With Mode (Pir OAD (Pin 20) low, taking ates low order byte output	this pin	
	IU XAM	as a low	flode (Pin 21) high, this pin byte flag output used in line Figures 8, 9, 10.		
19		and CE/L	Enable — With Mode (Pin OAD (Pin 20) low, taking ates high order byte outpu L, OR.	this pin	
	80	as a high	lode (Pin 21) high, this pin byte flag output used in the Figures 8, 9, 10.	n serves handshake	

PIN	SYMBOL	DESCRIPTION
20	CE/LOAD	Chip Enable Load — With Mode (Pin 21) low. CE/LOAD serves as a master output enable. When high, B1 — B12, POL, OR outputs are disabled.  — With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 8, 9, 10.
	MODE MOV PROPRIETOR M	Input Low — Direct output mode where CE7 LOAD (Pin 20), HBEN (Pin 19) and LBEN (Pin 19) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 10. Input High — Enables CE/LOAD (Pin 20), HBEN (Pin 19), and LBEN (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 8 and 9 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. — Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/HOLD	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to +5V if not used.
28	V=019	Analog Negative Supply — Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V* (Pin 40).
30	BUFFER	Buffer Amplifier Output
11210	AND WARRY TO THE REAL PROPERTY.	The state of the s

PIN	SYMBOL	DESCRIPTION				
31 AUTO-ZERO		Auto-Zero Node — Inside foil of CAZ				
32	INTEGRATOR	Integrator Output - Outside foil of CINT				
33	COMMON	Analog Common — System is Auto-Zeroe to COMMON				
34	INPUT LO	Differential Input Low Side				
35	INPUT HI	Differential Input High Side				

PIN	SYMBOL	DESCRIPTION				
36	REF IN +	Differential Reference Input Positive				
37	REF CAP +	Reference Capacitor Positive				
38	REF CAP	Reference Capacitor Negative				
39	REF IN	Differential Reference Input Negative				
40	40 V + Positive Supply Voltage — Nomin with respect to GND (Pin 1).					

Note: All digital levels are positive true.

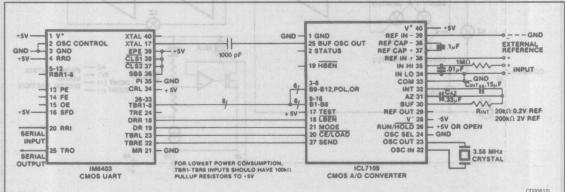
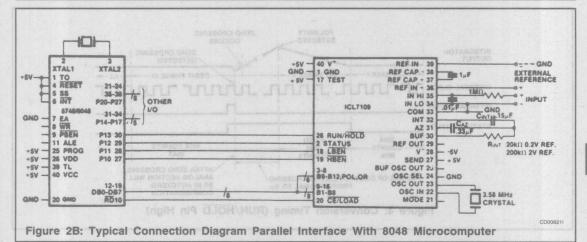


Figure 2A: Typical Connection Diagram UART Interface – To transmit latest result, send any word to UART



## DETAILED DESCRIPTION

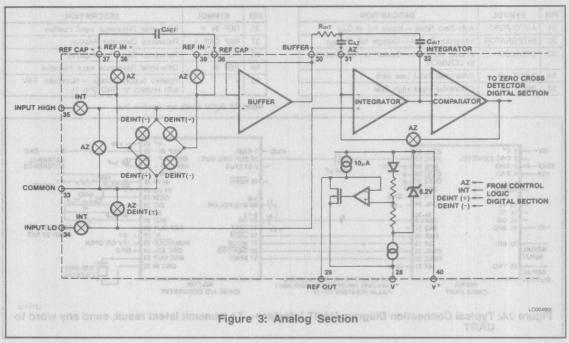
#### Analog Section

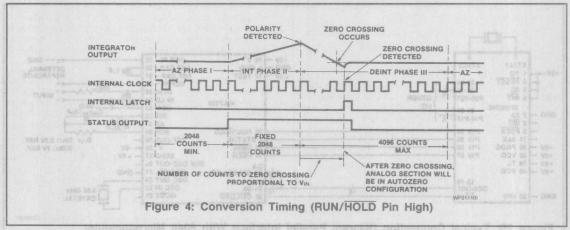
Figure 3 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/HOLD input is left open or connected to V<sup>+</sup>, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 4. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

#### Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor  $C_{AZ}$  to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10\mu V$ .

CL7109





#### Signal Integrate Phase

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

#### De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged

(during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal. The property to of bedsednoon to made

#### Differential Input and ve benimmered size as a social

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and -5V, this allows a 4V full scale integrator swing positive or negative thus maximizing the performance of the analog section.

#### Differential Reference was and make the air hugh

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

#### Component Value Selection Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

#### **Integrating Resistor**

Both the buffer amplifier and the integrator have a class A output stage with 100 µA of quiescent current. They supply 20 µA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small

enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale,  $200k\Omega$  is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, RINT should be chosen by the relation a not beau ad bluods Wma. NOS one solsos lui

$$R_{\text{INT}} = \frac{\text{full scale voltage}}{20\mu\text{A}}$$

# Integrating Capacitor, page and malaya print

The integrating capacitor CINT should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72kHz clock frequency) as provided by the crystal oscillator, nominal values for CINT and CAZ are 0.15 µF and 0.33 µF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of CINT is given by teres carefully observing polarities carefuld

$$C_{INT} = \frac{(2048 \times \text{clock period})(20 \mu \text{A})}{\text{integrator output voltage swing}}$$

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption. not controlled or where high-accu

#### **Auto-Zero Capacitor**

The size of the auto-zero capacitor has some influence on the noise of the system: the smaller the capacitor the lower the overall system noise. However, CAZ cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mV full scale where noise is very important and the integrating resistor small, a value of CAZ twice CINT is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of CAZ equal to half of C<sub>INT</sub> is recommended.

For optimal rejection of stray pickup, the outer foil of CAZ should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of CINT should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

#### Reference Capacitor

A 1µF capacitor gives good results in most applications. However, where a large reference common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10 µF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

#### Reference Voltage menuper epaked subru tent rinuone

The analog input required to generate a full scale output of 4096 counts is VIN = 2VREF. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are  $34k\Omega$  and  $0.15\mu F$ . This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

#### Reference Sources

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external highquality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF- (pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V + should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a  $1k\Omega$  resistor in series with pin 39.

## DETAILED DESCRIPTION AND TOTAL AND ALLE Digital Selection

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in Figure 5. spexisel well wind not 0 68 as

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in the Electrical Characteristics Table. For minimum power consumption, all inputs should swing from GND (low) to V + (high). Inputs driven from TTL gates should have  $3-5k\Omega$ pullup resistors added for maximum noise immunity.

#### MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

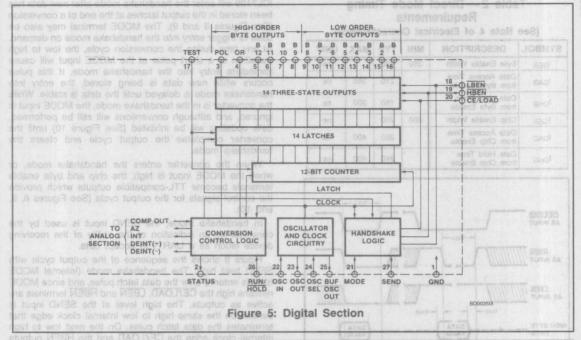
# STATUS Output, seve flore at rome about nominos to

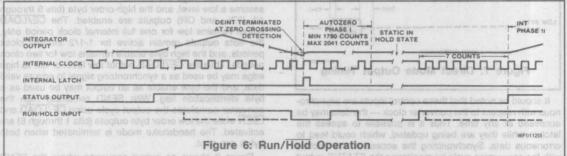
During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 4 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the convert-

# RUN/HOLD Input losgao yells edit of nochsquoo ni

When the RUN/HOLD input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 4). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting

If RUN/HOLD goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/HOLD stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/HOLD input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/HOLD. See Figure 6 for details.





Using the RUN/HOLD input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/HOLD low. When RUN/HOLD goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART — see Handshake Mode). RUN/HOLD may now be taken low which terminates deintegrate and ensures a minimum Auto-Zero time before the next conversion.

Alternately, RUN/HOLD can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/HOLD input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/HOLD to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

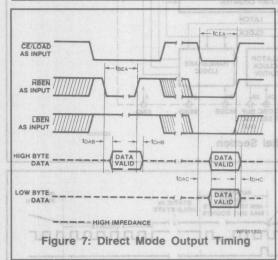
#### Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled 'Interfacing.' The timing requirements for these outputs are shown in Figure 7 and Table 2.

# Table 2 — Direct Mode Timing Requirements

(See Note 4 of Electrical Characteristics)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
†BEA	Byte Enable Width	350	220	K-76-7	ns
tDAB	Data Access Time from Byte Enable		210	350	ns
tDHB	Data Hold Time from Byte Enable		150	300	ns
tCEA	Chip Enable Width	400	260		ns
tDAC	Data Access Time from Chip Enable		260	400	ns
tDHC	Data Hold Time from Chip Enable		240	400	ns



It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the latches while they are being updated, which could lead to erroneous data. Synchronizing the access of the latches with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

## Handshake Mode chavnoo ent it eserts) crex-oluA

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequentially transfer two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the

ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of a conversion (See Figures 8 and 9). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 10) until the converter completes the output cycle and clears the handshake mode.

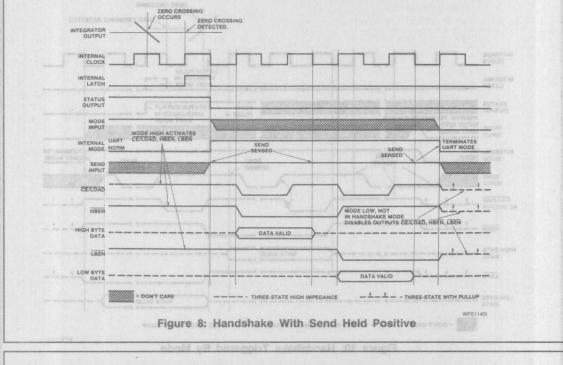
When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 8, 9, and 10).

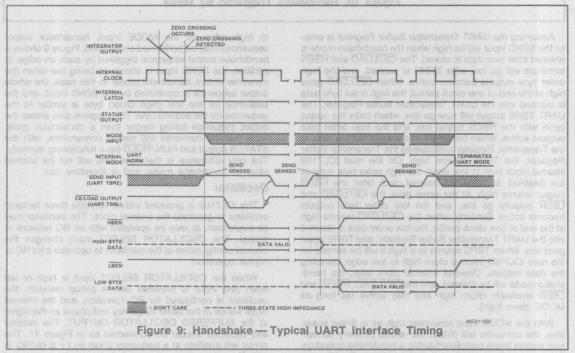
In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

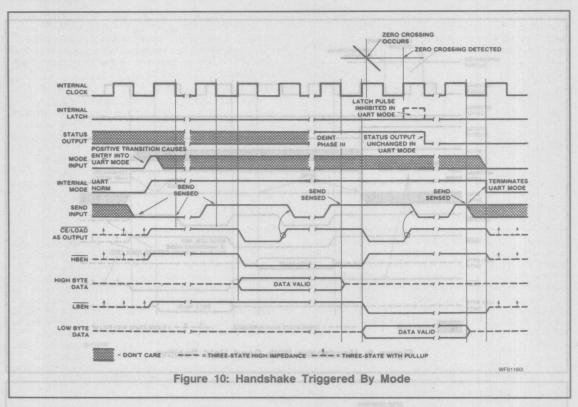
Figure 8 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse, and since MODE remains high the CE/LOAD, LBEN and HBEN terminals are active as outputs. The high level at the SEND input is sensed on the same high to low internal clock edge that terminates the data latch pulse. On the next low to high internal clock edge the CE/LOAD and the HBEN outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The CE/LOAD output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the CE/LOAD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using CE/LOAD and LBEN while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 9 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LOAD terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

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Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The CE/LOAD and HBEN terminals will go low after SEND is sensed, and the high order byte outputs become active. When CE/LOAD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the HBEN output returns high. At the same time, the CE/LOAD and LBEN outputs go low, and the low order byte outputs become active. Similarly, when the CE/LOAD returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the CE/LOAD, HBEN, and LBEN terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low

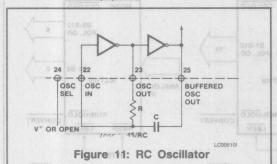
to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/HOLD input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

#### Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated with an RC network or crystal. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 11. The circuit will oscillate at a frequency given by f=0.45/RC. A  $100 \mathrm{k}\Omega$  resistor is recommended for useful ranges of

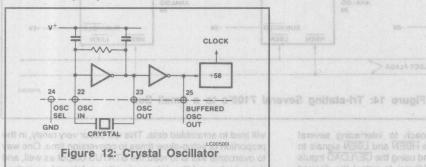
frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but should not be less than 50pF).



When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

T = (2048 clock periods) x 
$$\left[ \frac{58}{3.58 \text{MHz}} \right]$$
 = 33.18ms

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.



If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The

BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive capability, and when driving more than one slave device, external buffering should be used.

#### Test Input

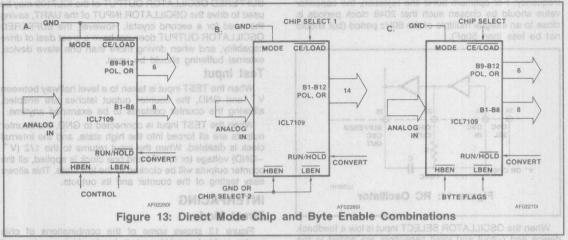
When the TEST input is taken to a level halfway between V<sup>+</sup> and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V $^+$ -GND) voltage (or to V $^+$ ) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

# INTERFACING Direct Mode

Figure 13 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The CE/LOAD input may be tied low, allowing either byte to be controlled by its own enable as in Figure 13A. Figure 13B shows a configuration where the two byte enables are connected together. In this configuration, the CE/LOAD serves as a chip enable, and the HBEN and LBEN may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 13C shows the HBEN and LBEN as flag inputs, and CE/LOAD as a master enable, which could be the READ strobe available from most microprocessors.

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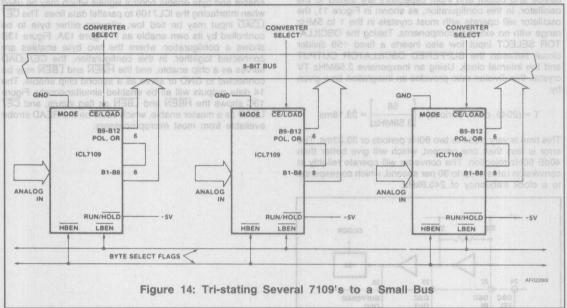
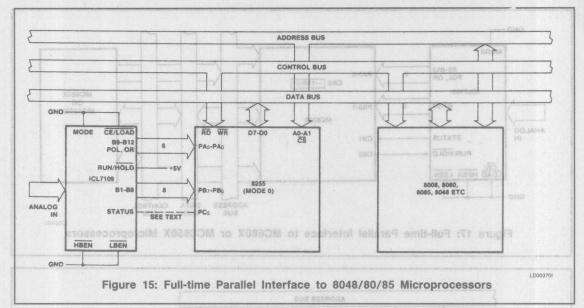
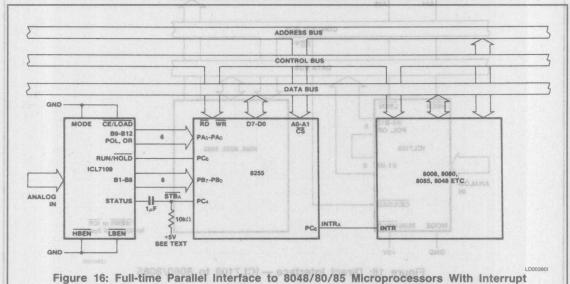


Figure 14 shows an approach to interfacing several ICL7109s to a bus, ganging the HBEN and LBEN signals to several converters together, and using the CE/LOAD inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 15 through 20. Figure 15 shows a straightforward application to the Intel 8048/80/85 microprocessors via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated

will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 16. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data latches. This application also shows the RUN/HOLD input being used to initiate conversions under software control.

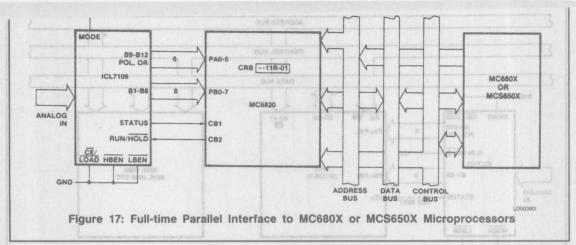


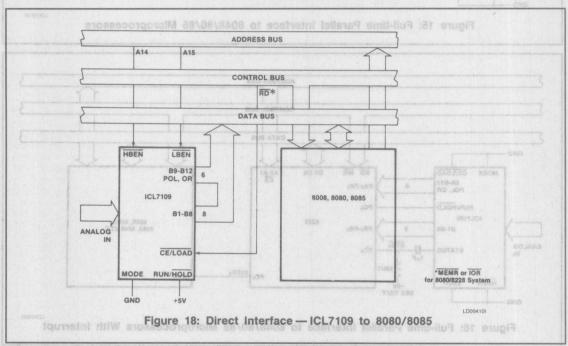


A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 17. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/HOLD pin through Control Register B, allowing software-controlled initiation of conversions in this system as well.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples

of this are shown in Figures 18 and 19. It is necessary to carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long buses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

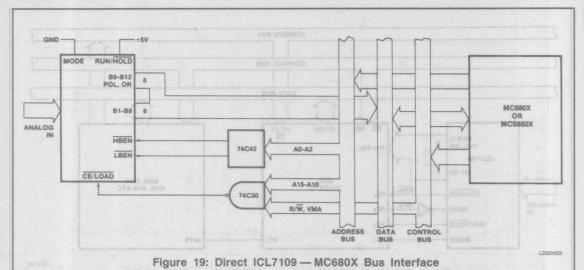




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The three-state output capability of the ICL7199 allows firect intertacing to most microprocessor busses. Examples



#### Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of CE/LOAD, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the CE/LOAD to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/HOLD input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command

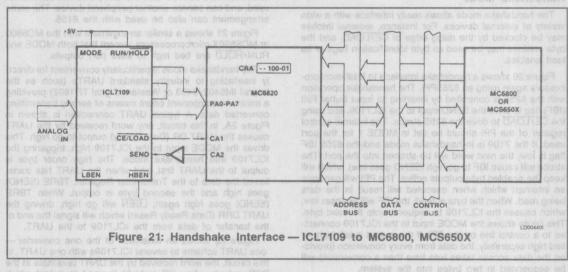
under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

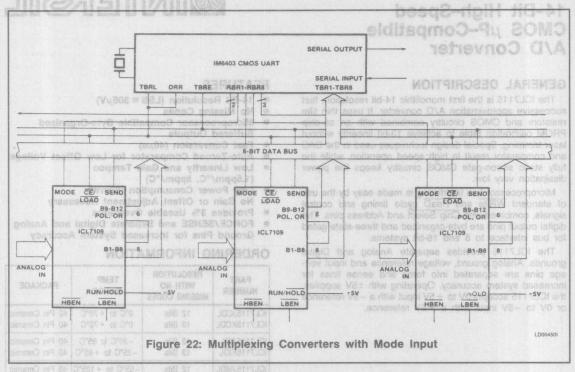
Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/HOLD are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown in Figure 2A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high again, LBEN will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter—one UART scheme to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

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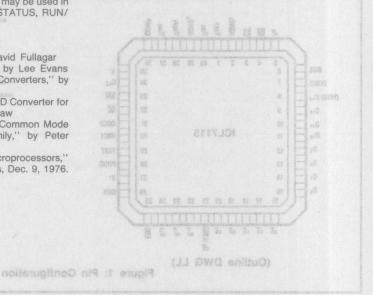


The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/HOLD, and MODE signals may be mixed.

#### APPLICATION NOTES

- A016 "Selecting A/D Converters," by David Fullagar
- A017 "The Integrating A/D Converters," by Lee Evans
- A018 "'Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A030 "The ICL7104 A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw
- R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

(Outline DWG DL)



S00-888108

### ICL7115

# 14-Bit High-Speed CMOS μP-Compatible A/D Converter



#### **GENERAL DESCRIPTION**

The ICL7115 is the first monolithic 14-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 13-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8 and 16-bit systems.

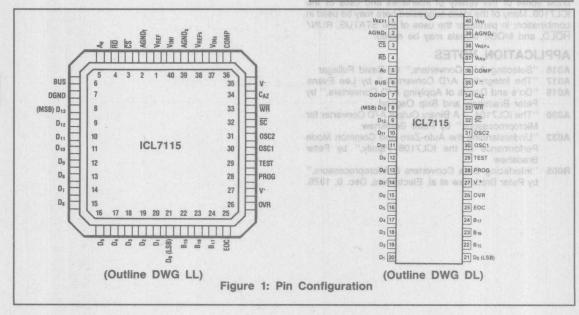
The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +5V input with a -5V reference or 0V to -5V input with a ±5V reference.

#### FEATURES

- 14-Bit Resolution (LSB = 305μV)
- No Missing Codes
- Microprocessor Compatible Byte-Organized Buffered Outputs
- Fast Conversion (40μs)
- Auto-Zeroed Comparator for Low Offset Voltage
- Low Linearity and Gain Tempco (1.5ppm/°C, 5ppm/°C)
- Low Power Consumption (60mW)
- No Gain or Offset Adjustment Necessary
- Provides 3% Useable Overrange
- FORCE/SENSE and Separate Digital and Analog
   Ground Pins for Increased System Accuracy

#### ORDERING INFORMATION

PART NUMBER	RESOLUTION WITH NO MISSING CODES	TEMP. RANGE	PACKAGE
ICL7115JCDL	12 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115KCDL	13 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115JIDL	12 Bits	-25°C to 85°C	40 Pin Ceramic
ICL7115KIDL	13 Bits	-25°C to +85°C	40 Pin Ceramic
ICL7115JMDL ICL7115KMDL ICL7115JMLL ICL7115KMLL	12 Bits 13 Bits 12 Bits 13 Bits	-55°C to +125°C -55°C to +125°C -55°C to +125°C -55°C to +125°C	40 Pin Ceramic 40 Pin LCC



ELECTRICAL CHARACTERISTICS

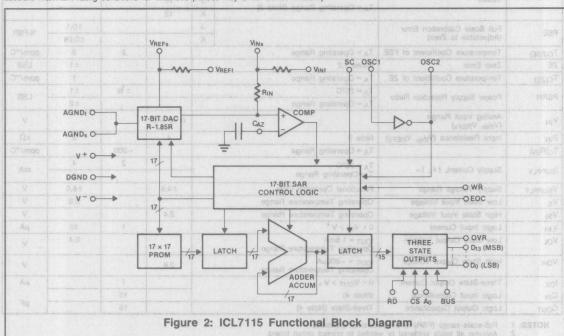
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#### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V+ to DGND0.3V to +6.5V	Operating Temperature Range
Supply Voltage V <sup>-</sup> to DGND+0.3V to -6.5V	ICL7115XCXX0°C to +70°C
VREFs, VREFf, VINS, VINf to DGND +25V to -25V	ICL7115XIXX25°C to +85°C
AGNDs, AGNDf to DGND + 1V to -1V	ICL7115XMXX55°C to +125°C
Current in FORCE and SENSE Lines	Storage Temperature Range65°C to +150°C
Digital I/O Pin Voltages0.3V to V <sup>+</sup> +0.3V	Power Dissipation500mW
PROG to DGND VoltageV- to V+ +0.3V	derate above 70°C @ 100mW/°C
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Lead Temperature (Soldering, 10sec)300°C

NOTE 1: All voltages with respect to DGND, unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



### ICL7115



### ELECTRICAL CHARACTERISTICS (F STOM) COMITAR MUMIXAM ETUJORSA

DC ELECTRICAL CHARACTERISTICS V+ = +5.0V, V- = -5.0V, V<sub>REFs</sub> = -5.0V, T<sub>A</sub> = +25°C, f<sub>CLK</sub> = 500kHz unless

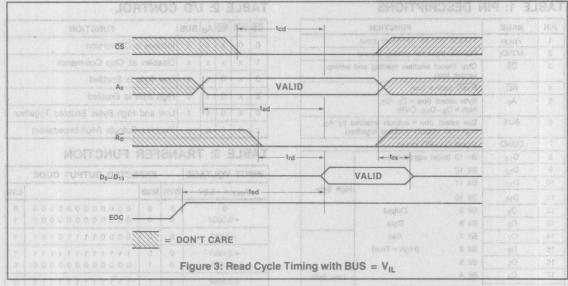
SYMBOL	PARAMETER	TEST CONDITIONS	2+	MIN	TYP	MAX	UNIT
to + 150°	Resolution Space and	SC = VIH		14	IRMRE N	E BOROS	Bits
		SC = VILID TANKS	of V	12	201	Pin Volta	AL letipi
ILE <sub>OC</sub>	Integral Linearity Error	Note 1	K K	V	908	±0.018 (	%FSR
T <sub>C</sub> (ILE)	Temperature Coefficient of ILE	TA = Operating Range	en ou	day maria		1.5	ppm/°C
y and function	Min Resolution with No Missing	TA = 25°C ob moramed eauth vem- and	J	12	mus to exact	stell excits av	o notesso
RES(NMC)	Codes	T <sub>A</sub> = Operating Range (Note 2)	J	11	enombrio	gridet murner	Bits
	Full Scale Calibration Error		J			±0.1	
FSE	(Adjustable to Zero)	staN.	K	Vegas		±0.08	%FSR
T <sub>C</sub> (FSE)	Temperature Coefficient of FSE	T <sub>A</sub> = Operating Range		9	2	5	ppm/°C
ZE	Zero Error	Notes 1,2		AAA .		±1	LSB
T <sub>C(ZE)</sub>	Temperature Coefficient of ZE	T <sub>A</sub> = Operating Range				1	ppm/°C
PSRR	Power Supply Rejection Ratio	T <sub>A</sub> = 25°C			± 1/2	±1	LSB
VIN	Analog Input Range (VINs, VREFs)	1 1000		0 to +5		- CHINDA	V
RIN	Input Resistance (VINs, VREFs)	Note 3		4		9	kΩ
T <sub>C</sub> (R <sub>IN</sub> )		T <sub>A</sub> = Operating Range			-300	un 4 m	ppm/°C
ISUPPLY	Supply Current, I+, I-	T <sub>A</sub> = 25°C T <sub>A</sub> =Operating Range		1 1/18	2	4	, mA
VSUPPLY	Supply Voltage Range	Functional Operation Only		±4.5		±6.0	V
VIL	Low State Input Voltage	Operating Temperature Range	-		4-	0.8	V
VIH	High State Input Voltage	Operating Temperature Range		2.4			V
ILIH	Logic Input Current	0 < VIN > V +			1	10	μΑ
Vol	Low State Output Voltage	I <sub>OUT</sub> = 1.6mA Operating Temperature Range	d	17 × 17		0.4	V
Vон	High State Output Voltage	I <sub>OUT</sub> = -200μA Operating Temperature Range		2.8			٧
lox	Three-State Output Current	0 < V <sub>OUT</sub> > V + MUDDA			1		μΑ
CIN	Logic Input Capacitance	(Note 4)			15		25
COUT	Logic Output Capacitance	Three-State (Note 4)			15	NAME OF THE PARTY	pF

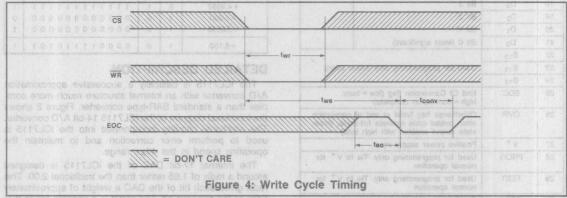
NOTES: 1. Full-scale range (FSR) is 5V (reference adjusted).

2. Assume all leads soldered or welded to printed circuit board.

3. Assume all leads soldered or welded to printed circuit board.

6





AC ELECTRICAL CHARACTERISTICS V<sup>+</sup> = +5.0V, V<sup>-</sup> = -5.0V, T<sub>A</sub> = +25°C, f<sub>clk</sub> = 500kHz unles otherwise noted. Data derived from extensive characterization testing. Parameters are not 100% production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
READ CYCLI	TIMING	Market View	Notion	ninos tenesejas	May Ollie	3/12
t <sub>cd</sub>	Prop. Delay CS to Data	RD Low, Ao Valid	Tug	or Aiddra Janesco	200	N N N N
tad	Prop. Delay Ao to Data	CS Low, RD Low		V OU DU 1000	200	MGO   8
alid trd hivib	Prop. Delay RD to Data	CS Low, Ao Valid		Box tridul sos es	200	ns .
to tox	Prop. Delay Data to Three State	amom ers	nichii	sonoretet tot on	100	a taky 6
ted	Prop. Delay EDC High to Data	CONVERSION	DEADE	o polena for en	200	BREA 9
WRITE CYCL	E TIMING	TO PHOOM	(2009)	10V JASKI 101 SITE	FORCE	MAIN D
twr	WR Low Time	TO DEBOTO	100			ns
t <sub>we</sub>	Prop. Delay WR Low to EDC Low	Wait Mode	1		2	
teo	EOC High Time	Free-Run Mode	0.5		1.5	
abas-ilui nd	Conversion Time	SC = V <sub>IH</sub>			20	1/fclk
tconv	Conversion Time	SC = VIL		BITALL SERIES	18	



#### TABLE 1: PIN DESCRIPTIONS

PIN	NAME	FUNCTION	
1	V <sub>REFf</sub>	FORCE line for reference input.	
2	AGNDf	FORCE input for analog ground	
3	CS	Chip Select enables reading and writing (active low)	
4	RD	ReaD (active low)	
5	A <sub>0</sub>	Byte select (low = $D_0-D_7$ , high = $D_8-D_{13}$ , OVR)	
6	BUS	Bus select (low = outputs enabled by A <sub>0</sub> , high = all outputs enabled together)	
7	DGND	Digital GrouND return	
8	D <sub>13</sub>	Bit 13 (most significant)	
9	D <sub>12</sub>	Bit 12	
10	D <sub>11</sub>	Bit 11	
11	D <sub>10</sub>	Bit 10	
12	D <sub>9</sub>	Bit 9 Output	
13	D <sub>8</sub>	Bit 8 Data	
14	D <sub>7</sub>	Bit 7 Bits	
15	D <sub>6</sub>	Bit 6 (High = True)	
16	D <sub>5</sub>	Dit 6	
17	D <sub>4</sub>	Bit 4 Low Byte	
18	D <sub>3</sub>	Bit 3	
19	D <sub>3</sub>	Bit 2	
20	D <sub>2</sub>	Bit 1	
21	D <sub>0</sub>	Bit 0 (least significant)	
22	B <sub>15</sub>	Bit 0 (least significant)	
23		Used for programming only (leave open)	
24	B <sub>16</sub>	Osed for programming only (leave open)	
25	B <sub>17</sub> EOC	End Of Conversion flag (low = busy,	
20	EOC	high = conversion complete)	
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)	
27	٧+	Positive power supply input	
28	PROG	Used for programming only. Tie to V + for normal operation	
29	TEST	Used for programming only. Tie to V + for normal operation	
30	OSC1	Oscillator inverter input	
31	OSC2	Oscillator inverter output	
32	SC	Short cycle input (high = 14-bit, low = 12-bit operation)	
33	WR	WRite pulse input (low starts new conversion	
34	CAZ	Auto-zero capacitor connection	
35	V-	Negative power supply input	
36	COMP	Used in test, tie to V	
37	V <sub>INs</sub>	SENSE line for input voltage	
38	VREFS	SENSE line for reference input	
39	AGNDs	SENSE line for analog ground	
40	VINf	FORCE line for input voltage	

#### TABLE 2: I/O CONTROL

CS	WR	RD	A <sub>0</sub>	BUS	FUNCTION
0	0	Х	X	X	Initiates a Conversion
1	X	X	X	X	Disables all Chip Commands
0	X	0	0	0	Low Byte is Enabled
0	Х	0	1	0	High Byte is Enabled
0	X	0	Х	1	Low and High Bytes Enabled Together
X	×	1	X	×	Disables Outputs (High-Impedance)

#### **TABLE 3: TRANSFER FUNCTION**

INPUT VOLTAGE	-	EXP	ECTED OUTPUT CODE	
V <sub>REF</sub> = -5.0V	OVR	MSB	MARKET BEING	LSB
0	0	0	000000000000	0
+ 0.0003	0	0	000000000000	1
+0.150	0	0	000011110101	1
+ 2.4997	0	0	111111111111	1
+2.500	0	1	000000000000	0
+4.9994	0	1	11111111111	0
+ 4.9997	0	1	111111111111	1
+5.000	1	0	000000000000	0
+5.0003	1	0	000000000000	1
+5.150	1	0	000011110101	1

#### **DETAILED DESCRIPTION**

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 2 shows the functional diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the  $40\mu s$  range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the onchip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (B16) and the MSB-4 bit (B12). The sequence continues for each bit pair, B<sub>X</sub> and B<sub>X-4</sub>, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the

final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion. When the Short Cycle (SC) input is low, 18 clock cycles are required to complete a 12-bit conversion.

The overflow output of the 17-bit full-adder is also the OVerRange (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

#### **OPTIMIZING SYSTEM PERFORMANCE**

The FORCE and SENSE inputs for  $V_{IN}$  and  $V_{REF}$  are also shown driven by external op-amps. This technique eliminates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than  $300 \text{m}\Omega$  of total series resistance, the result can be a voltage error equivalent to 1LSB. If no op-amps are used for  $V_{IN}$  and  $V_{REF}$ , connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the  $V_{IN}$  and  $V_{REF}$  pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

When using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115 as shown in Figures 5 and 6. In Figure 5 the FORCE line is the only point that is connected to system analog ground. In Figure 6, the op-amp A<sub>3</sub> forces the voltage at AGND to be equal to analog system ground. The addition of this op-amp overcomes the main deficiency of the arrangement in Figure 5: the V<sub>IN</sub> and V<sub>REF</sub> sources are not referenced to true analog system ground.

The clamp diodes in Figure 6 are required because spurious op-amp output on AGNDf during power-on can exceed the absolute max rating of ±1.0V between AGDf and DGND. The two inverse-parallel diodes clamp the voltage between AGNDs and DGND to ±0.7V.

#### INPUT WARNING

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7115 until the  $\pm 5V$  power supplies have stabilized.

#### INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers,  $\overline{\text{CS}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ , and bus select inputs (A<sub>0</sub> and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A<sub>0</sub> lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a  $\overline{\text{WR}}$  pulse (pin 33) when  $\overline{\text{CS}}$  (pin 3) is low. Data is enabled on the bus when the chip is selected and  $\overline{\text{RD}}$  (pin 4) is low.

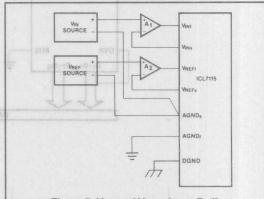


Figure 5: VIN and VREF Input Buffers

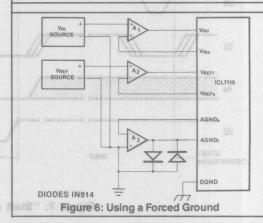
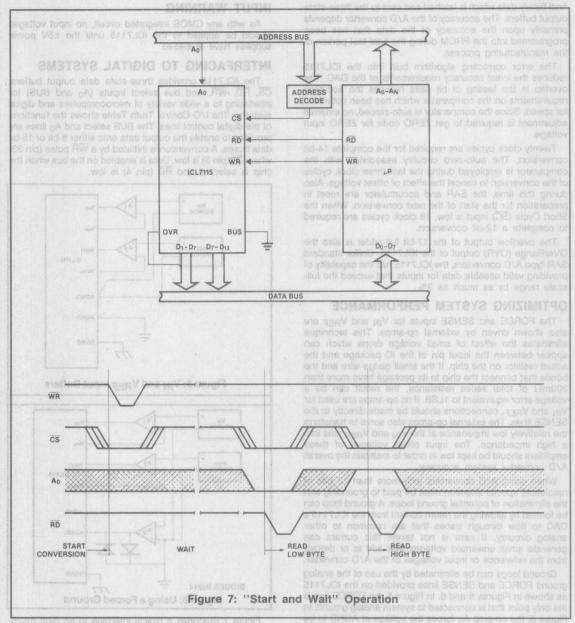


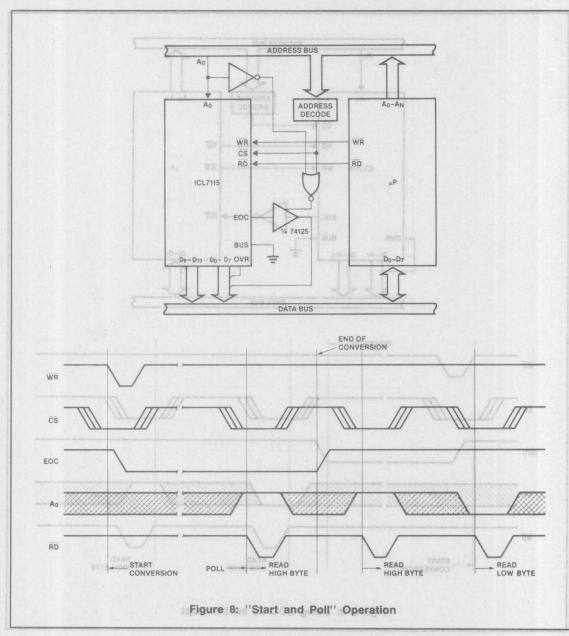
Figure 7 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the WR input to the ICL7115 after the I/O or memory-mapped address decoder has brought the CS input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A<sub>0</sub> enables the LSBs and a high level enables the MSBs.

V



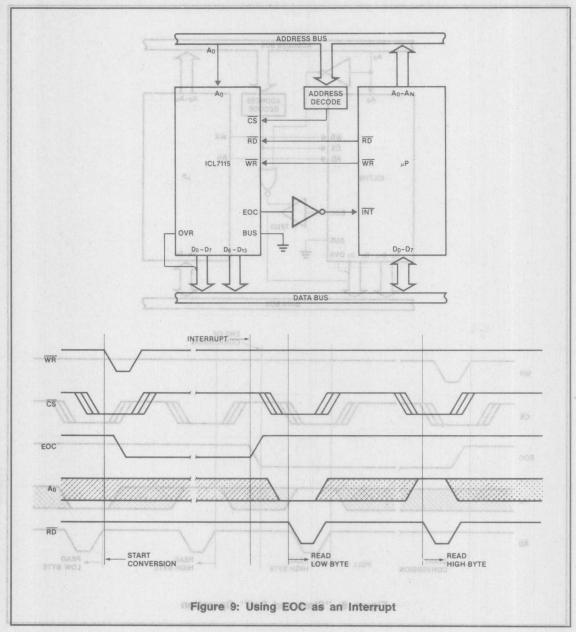
By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a ''Start and Poll'' interface (Figure 8). In this mode, the  $A_0$  and  $\overline{\text{CS}}$  lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the  $\overline{\text{WR}}$  line to initiate a conversion, the microprocessor continually

reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.



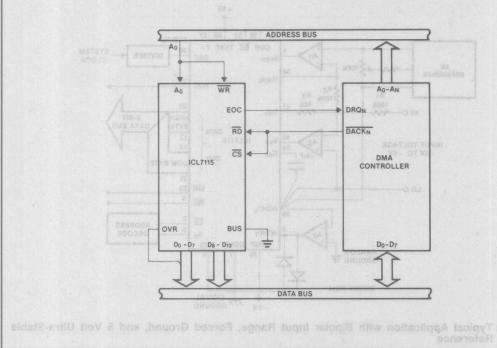
Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 9. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D

converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 9.



a Direct Memory Access (DMA) controller as shown in

6



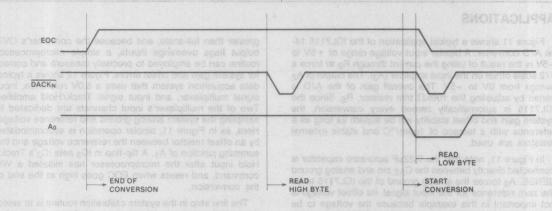


Figure 10: Data to Memory via DMA Controller

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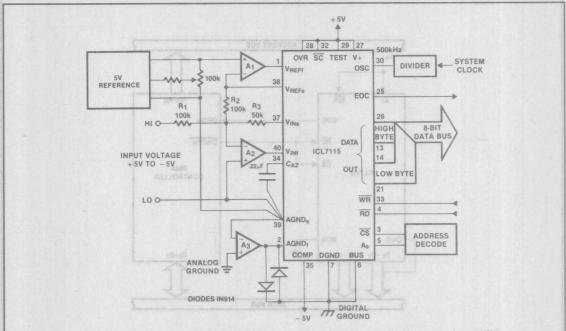


Figure 11: Typical Application with Bipolar Input Range, Forced Ground, and 5 Volt Ultra-Stable Reference

#### **APPLICATIONS**

Figure 11 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of  $\pm$ 5V to  $\pm$ 5V is the result of using the current through  $R_2$  to force a 1/2 scale offset on the input amplifier (A2). The output of A2 swings from 0V to  $\pm$ 5V. The overall gain of the A/D is varied by adjusting the  $\pm$ 100k $\pm$ 1 trim resistor, R5. Since the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/°C and stable external resistors are used.

In Figure 11, note that the  $0.22\mu\text{F}$  auto-zero capacitor is connected directly between the  $C_{AZ}$  pin and analog ground SENSE.  $A_3$  forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground. It is important to note that since the 7115's DAC current flows in  $A_1$ ,  $A_2$  and  $A_3$  these amplifiers should be wideband (GBW > 20MHz) types to minimize errors.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for a conversion time of 40 $\mu s$ . Output data is controlled by the BUS and  $A_0$  inputs. Here they are set for 8-bit bus operation with BUS grounded and  $A_0$  under the control of the address decode section of the external system.

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3%

greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 12 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 11, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A<sub>1</sub>. A flip-flop in IC<sub>3</sub> sets IC<sub>2</sub>'s Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from IC1, IC2, and A1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

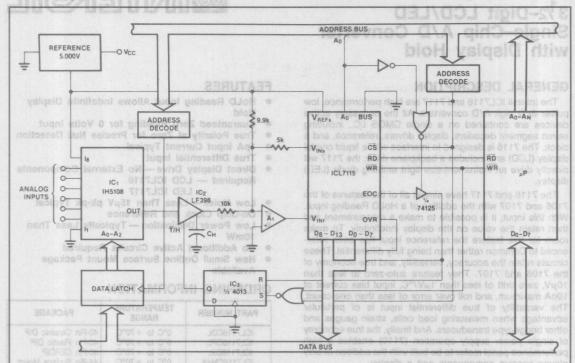


Figure 12: Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

The ICL7115 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}}$$
 for 14-bit operation

and

$$f_{CLK} = \frac{18}{t_{CODY}}$$
 for 12-bit operation

Figure 1: Pin Configurations

### ICL7116/7117

### 3½-Digit LCD/LED Single-Chip A/D Converter with Display Hold



#### GENERAL DESCRIPTION

The Intersil ICL7116 and 7117 are high performance, low power 3-½ digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal-display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HoLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. They feature auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display. tem with Zero and Reference Lines Brought to

#### **FEATURES**

- HoLD Reading Input Allows Indefinite Display Hold
- Guaranteed Zero Reading for 0 Volts Input
- True Polarity at Zero for Precise Null Detection
- 1pA Input Current Typical
- True Differential Input
- Low Noise Less Than 15μV pk-pk Typical
- On-Chip Clock and Reference
- Low Power Dissipation Typically Less Than
   10mW
- No Additional Active Circuits Required
- New Small Outline Surface Mount Package
   Available

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7116CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7116CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7116CJL	0°C to +70°C	40-Pin CERDIP
ICL7116CM44	0°C to +70°C	44-Pin Surface Mount
ICL7117CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7117CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7117CJL	0°C to +70°C	40-Pin CERDIP

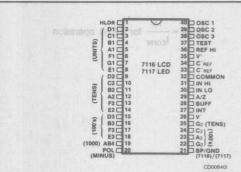
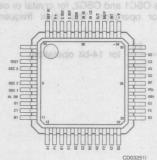


Figure 1: Pin Configurations



### ICL7116/7117

### **BINITERSIL**

#### ABSOLUTE MAXIMUM RATINGS

	XAICL7116 9YT			ICL7117 TEMARAS
Analog Inpu Reference HLDR, Cloo Power Diss Cera Plas	age (V + to V -)	1) . V + to V V + to V Test to V + 1000mW 800mW	Analog Input Voltage Reference Input Volt HLDR, Clock Input Power Dissipation ( Ceramic Pack	+ 6V -9V e (either input) (Note 1)V+ to V- tage (either input)
Storage Te	erature65 erature (Soldering, 10sec)	s°C to +150°C 300°C	Operating Temperature Storage Temperature	ge

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to  $\pm 100 \mu A$ .

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS** (Note 3)

PARAMETER CONT.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V <sub>IN</sub> = 0.0V Full Scale = 200.0mV	- 000.0	±000.0	+ 000.0	Digital Reading
Ratiometric Reading	V <sub>IN</sub> = V <sub>REF</sub> V <sub>REF</sub> = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	IV <sub>IN</sub> I ≈ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V (Note 7)	-1	±0.2	variat 1	Counts
Common Mode Rejection Ratio (Note 4)	V <sub>CM</sub> = ±1V, V <sub>IN</sub> = 0V, Full Scale = 200.0mV		50	1 10 10 10 10 10 10 10 10 10 10 10 10 10	μV/V
Noise (Pk — Pk value not exceeded 195% of time)	V <sub>IN</sub> = 0V Full Scale = 200.0mV	consens fernious T. fore	15	ST DEFE	μV
Leakage Current @ Input	V <sub>IN</sub> = 0V (Note 7)	wetowk?	tiet Coretes	10	pA
Zero Reading Drift	V <sub>IN</sub> = 0 0°C < T <sub>A</sub> < 70°C (Note 7)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V <sub>IN</sub> = 199.0mV 0°C < T <sub>A</sub> < 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V + Supply Current (Does not include LED current for 7117)	VIN = 0 and de tro and		0.8	1.8	mA
V Supply Current (7117 only)	to the converter po		0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between COMMON & pos. Supply	2.4	2.8	3.2	Y
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between COMMON & pos. Supply		80	Notation 1	ppm/°C
nput Resistance, Pin 1 (Note 6)	Q 91aggrate p	30	70	BBBBBBB	kΩ
V <sub>IL</sub> , Pin 1 (7116 only)	easily land ariT			TEST + 1.5	V
V <sub>IL</sub> , Pin 1 (7117 only)	amount at wol mont			GND + 1.5	V
/IH, Pin 1 (Both)	nnoo si rloid tunni	V <sup>+</sup> - 1.5	310	NATIONAL PARTIES AND ADDRESS OF THE PARTIES AND	V
7116 ONLY Rk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage Note 5)	V <sup>+</sup> - V <sup>-</sup> = 9V	4 4	5	6	V

\_

Floure 3: ICL7117 Test Circuit and Typical

### ICL7116/7117



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

PARAMETER	TEST CONDITIONS	MIN	TYP 81	MAX	UNIT
7117 ONLY Segment Sinking Current	V <sup>+</sup> = 5.0V	(87		("Y of "Y	Supply Voltage (
(Except Pin 19 and 20)	Segment Voltage = 3V	0 5 V. (1	8.0	rentie) aga	lov arent golani
(Pin 19 only)	allov Jugni polseA	0 10	16	voltage (eith	MAIN MAIN
(Pin 20 only)	Reference Input V	Way Aga	7	71	distribution of the

NOTES: 3. Unless otherwise noted, specifications apply to both the 7116 and 7117 at TA = 25°C, f<sub>clock</sub> = 48kHz. 7116 is tested in the circuit of

- Figure 4. 7117 is tested in the circuit of Figure 5.

  4. Refer to "Differential Input" discussion.

  5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
- 6. The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

7. Not tested, guaranteed by design.

#### **TEST CIRCUITS**

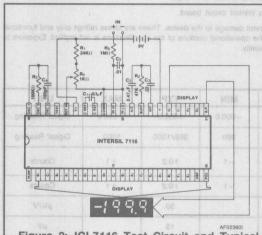
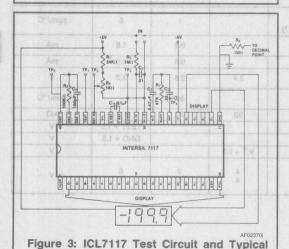


Figure 2: ICL7116 Test Circuit and Typical Application With Liquid Crystal Display



Application With LED Display

**DETAILED DESCRIPTION** 

#### Analog Section

Figure 4 shows the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

#### Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10\mu V$ .

#### Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

#### De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000

#### Differential Input in attit and of very segren Titl

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of typically 86dB. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive commonmode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See A032 for a discussion of the effects of stray capacitance.

#### Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

#### Analog COMMON sannos to nego itel ed ras fugnit

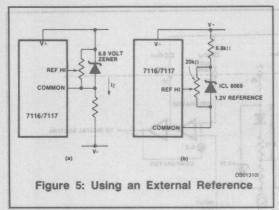
This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts less than the positive supply. This is selected to provide proper operation with a minimum endof-life battery voltage of about 6V. However, the analog COMMON does have some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ( > 7V), the COMMON voltage will have a low voltage coefficient (.001%/V), low output

impedance ( $\simeq$ 15 $\Omega$ ), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 µV to 80μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

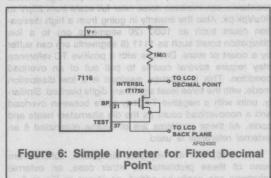
Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

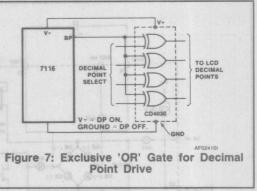


Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only  $10\mu A$  of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

#### TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a  $500\Omega$  resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.





The second function is a "lamp test". When TEST is pulled to high (to V $^+$ ) all segments will be turned on and the display should read – 1888. [Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]

#### DIGITAL SECTION

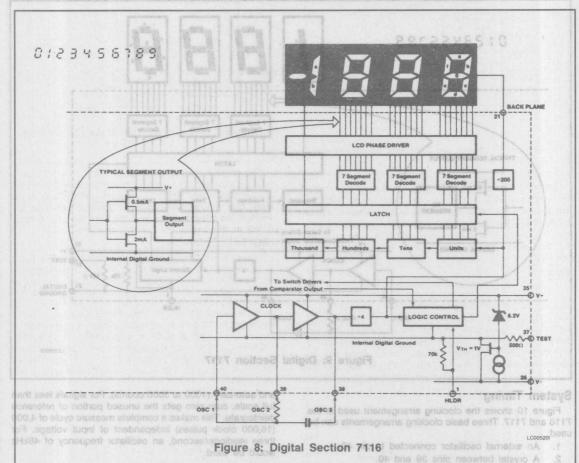
Figures 8 and 9 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7117. It is identical to that of the 7116 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

#### **HOLD** Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a  $70\mathrm{k}\Omega$  typical resistance to either TEST (7116) or GROUND (7117).



COCCEON ACTIONS ACTION

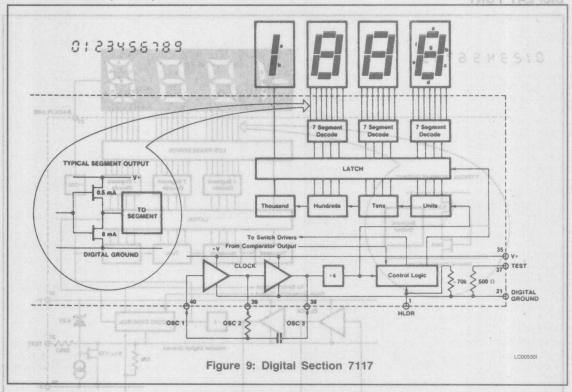
The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts).

Integrate cycle should be a multiple of 60Hz Oscillator frequencies of 240kHz, 120kHz, 60kHz, 60kHz, 60kHz, 48kHz, 48kHz, 132 MkHz, 132 MkHz, 152 Shutz, 1

# COMPONENT VALUE SELECTION

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 20µA of drive current with negligible non-linearity, The integrating resistor should be large shough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volta full scale,  $470k\Omega$  is graded on the PC board. For 2 volta full scale,  $470k\Omega$  is near optimum and similarly a  $47k\Omega$  resistor is optimum for a 200.0mV scale.

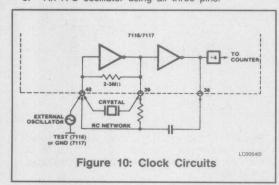
**DISPLAY FONT (CONT.)** 



#### System Timing

Figure 10 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

- 1. An external oscillator connected to pin 40. Hope land
- 2. A crystal between pins 39 and 40.
- 3. An R-C oscillator using all three pins.



The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts)

and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33½kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

# COMPONENT VALUE SELECTION Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with  $100\mu A$  of quiescent current. They can supply  $20\mu A$  of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volts full scale,  $470k\Omega$  is near optimum and similarly a  $47k\Omega$  resistor is optimum for a 200.0mV scale.

#### Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal  $\pm 2$  volt full scale integrator swing is fine. For the 7117 with  $\pm 5$  volt supplies and analog common tied to supply ground, a  $\pm 3.5$  to  $\pm 4$  volt swing is nominal. For three readings/second (48kHz clock), nominal values for  $C_{\rm INT}$  are  $0.22\mu{\rm F}$  and  $0.10\mu{\rm F}$ , respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

#### Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a  $0.47\mu\text{F}$  capacitor is recommended. On the 2 volt scale, a  $0.047\mu\text{F}$  capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

#### **Reference Capacitor**

A  $0.1\mu F$  capacitor gives good results in most applications. If rollover errors occur a larger value, up to  $1.0\mu F$  may be required.

#### **Oscillator Components**

For all ranges of frequency a 100k $\Omega$  resistor is recommended and the capacitor is selected from the equation f  $\simeq \frac{0.45}{100}$ . For 48kHz clock (3 readings/second), C = 100pF.

#### Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: VIN = 2VREF. Thus, for the 200.0mV and 2.000 volt scale, VREF should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V<sub>BFF</sub> = 0.341V. Suitable values for integrating resistor and capacitor would be  $120k\Omega$  and  $0.22\mu$ F. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for V<sub>IN</sub> ≠ 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

#### 7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors,

and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

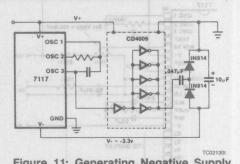


Figure 11: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the common mode range of the converter.
- 2. The signal is less than ±1.5 volts in magnitude.
- 3. An external reference is used.

#### TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

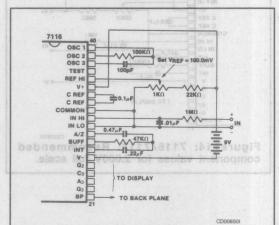


Figure 12: 7116 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

6

TYPICAL APPLICATIONS (CONT.)

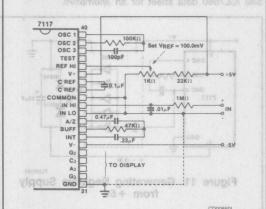


Figure 13: 7117 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)

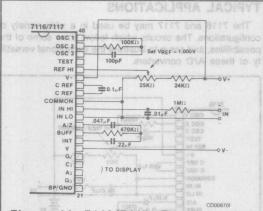


Figure 14: 7116/7117: Recommended component values for 2.000V full scale.

Figure 12: 7116 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (3V bettern).

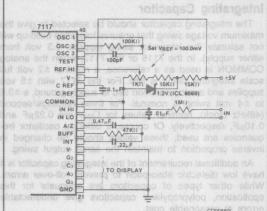


Figure 15: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V<sup>+</sup> and V<sup>-</sup> is insufficient for correct operation of the internal reference.

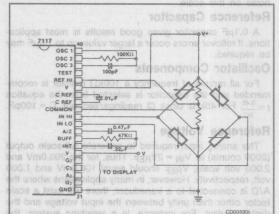


Figure 16: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

 $120k\Omega$  and  $0.22\mu\mathrm{F}$ . This makes the system slightly quieter and also evoids a divider network on the input. The 7117 with  $\pm$ 5 volts supplies can accept input signals up to  $\pm$ 4 with  $\pm$ 6 volts supplies can accept input signals up to  $\pm$ 6 digital reading of zero is desired for  $\forall_{\mathrm{IN}} \neq 0$ . Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the vanishe (or fixed) offset voltage between COMMON and IN U.O.

The 7117 is designed to work from ±5 volt supplies.

However, if a negative supply is not available, it can be generated from the clock output with 2 diodes. 2 occapions.

#### TYPICAL APPLICATIONS (CONT.)

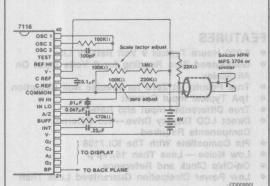


Figure 17: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

#### **APPLICATION NOTES**

- A016 "Selecting A/D Converters," by David Fullagar.
- A017 "The Integrating A/D Converter," by Lee Evans. A018 "Do's and Don'ts of Applying A/D Converters," by
- Peter Bradshaw and Skip Osgood.
- "41/2-Digit Panel Meter Demonstrator/ Instrumentation Boards," by Michael Dufort.
- A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
- A052 "Tips for Using Single-Chip 31/2-Digit A/D

Converters," by Dan Watson.

### 3<sup>1</sup>/<sub>2</sub>-Digit Low-Power Single-Chip A/D Converter

#### **GENERAL DESCRIPTION**

The Intersil ICL7126 is a high performance, very low power  $3^{1/2}$ -digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is  $100\mu\text{A}$ , ideally suited for 9V battery operation.

The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than  $10\mu V$ , zero drift of less than  $1\mu V/^{\circ}C$ , input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

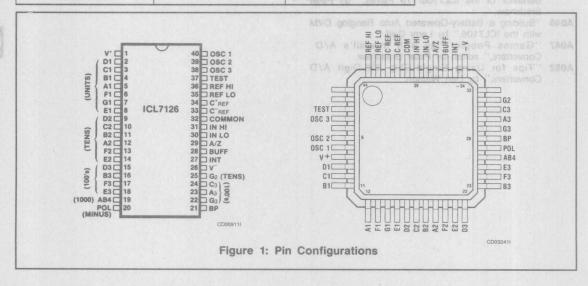


#### **FEATURES**

- 8,000 Hours Typical 9 Volt Battery Life
- Guaranteed Zero Reading for 0 Volts Input On All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LCD Display Drive No External Components Required
- Pin Compatible With The ICL7106
- Low Noise Less Than 15μVp-p
- On-Chip Clock and Reference
- Low Power Dissipation Guaranteed Less Than 1mW
- No Additional Active Circuits Required
- Evaluation Kit Available (ICL7126EV/KIT)

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7126CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7126CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7126CM44	0°C to +70°C	40-Pin Surface Mount
ICL7126RCPL	0°C to +70°C	40-Pin Plastic DIP
ICL7126CJL	0°C to +70°C	CERDIP
ICL7126EV/KIT		EVALUATION KIT



#### ABSOLUTE MAXIMUM RATINGS

Reference Input Voltage (Either Input) ....... V+ to V-Clock Input ......TEST to V+

Power Dissipation (Note 2)	
Ceramic Package	1000mV
Plastic Package	800mV
Operating Temperature	
Storage Temperature	65°C to +150°C
Lead Temperature (Soldering,	10sec)300°C

NOTE 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.

NOTE 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

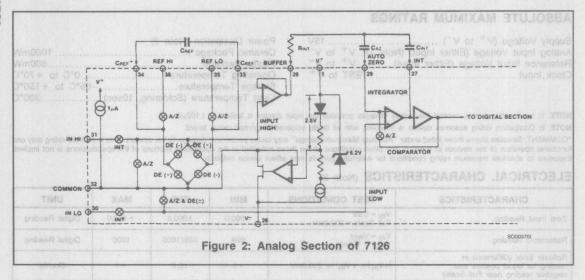
#### **ELECTRICAL CHARACTERISTICS** (Note 3)

CHARACTERISTICS	TEST CONDITIONS	MIN	CONTYP.	MAX	UNIT
Zero Input Reading	V <sub>IN</sub> = 0.0V Full Scale = 200.0mV	=000.0	±000.0	+ 000.0	Digital Reading
Ratiometric Reading	V <sub>IN</sub> = V <sub>REF</sub> V <sub>REF</sub> = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$ -V_{1N}  = +V_{1N} \simeq 200.0 \text{mV}$		±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	-1	±0.2	+1 87	Counts
Common Mode Rejection Ratio (Note 4)	V <sub>CM</sub> = ±1V, V <sub>IN</sub> = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V <sub>IN</sub> = 0V Full Scale = 200.0mV		15	- O O +	μV
Leakage Current @ Input	V <sub>IN</sub> = 0V		1 1	10	pA
Zero Reading Drift	V <sub>IN</sub> = 0 0°C < T <sub>A</sub> < 70°C		0.2	S 1	μV/°C
Scale Factor Temperature Coefficient	V <sub>IN</sub> = 199.0mV 0°C < T <sub>A</sub> < 70°C (Ext. Ref. 0 ppm/°C)	In	198	5 OMBI	ppm/°C
Supply Current (Does not include COMMON current)	V <sub>IN</sub> = 0 (Note 6)	YALIFE	70	100	μΑ
Analog COMMON Voltage (With respect to pos. supply)	250kΩ between Common & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250kΩ between Common & pos. Supply		150	INTERBIL TH	ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V <sup>+</sup> to V <sup>-</sup> = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V <sup>+</sup> to V <sup>-</sup> = 9V	4 6	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.	The state of	40	SUPPRIOR TO STREET	pF

NOTES: 3. Unless otherwise noted, specifications apply at TA = 25°C, f<sub>clock</sub> = 16kHz and are tested in the circuit of Figure 4.

4. Refer to "Differential Input" discussion.

Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times 5. Back plate differs in phase with segment and the following conversion rate. Average DC component is less than 50mV.
6. During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 5, increases current by 8μA (typ).
7. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).



#### TEST CIRCUITS

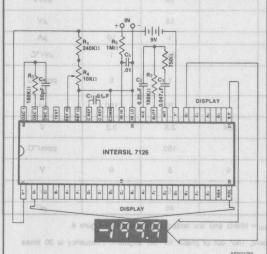
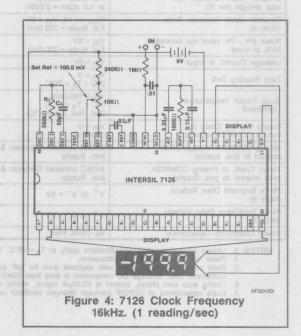
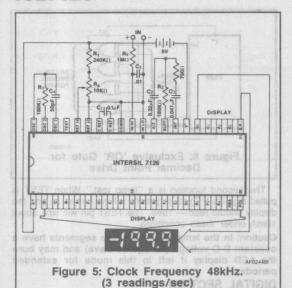


Figure 3: ICL7126 with Liquid Crystal Display



6-90



# DETAILED DESCRIPTION Annual language la

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

#### Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor  $C_{AZ}$  to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less then  $10\mu V$ .

#### Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter the integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

#### De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the

input signal. Specifically the digital reading displayed is  $1000 \left( \frac{V_{IN}}{V_{REF}} \right)$ .

#### **Differential Input**

The input can accept differential voltages anywhere within the common mode rante of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive commonmode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracv. The integrator output can swing within 0.3 Volts of either supply without loss of linearity. The model at the me ave

#### **Differential Reference**

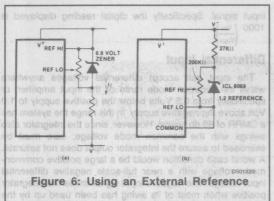
The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

#### **Analog COMMON**

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (< 7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ( $\simeq$ 15 $\Omega$ ), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate ( < 7V). These problems are eliminated if an external reference is used, as shown in Figure 6.



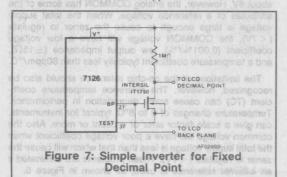


Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage, If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 3mA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only  $1\mu A$  of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

#### TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a  $500\Omega$  resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.



7126

DECIMAL POINT SELECT

TO LCD. DECIMAL POINTS

GROUND = dp OFF. C04030

GROUND = dp OFF. C04030

GROUND = dp OFF. C04030

GND

AF02460I

Figure 8: Exclusive 'OR' Gate for Decimal Point Drive

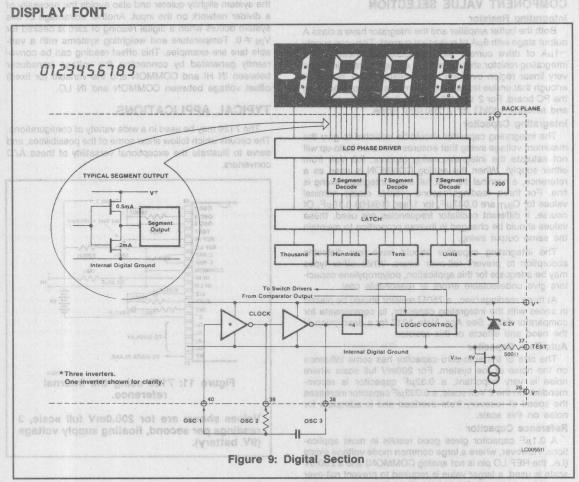
The second function is a "lamp test." When TEST is pulled high (to V +) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

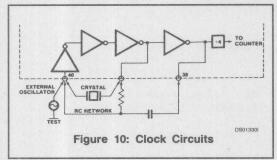
Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

#### DIGITAL SECTION equibes ()

Figure 9 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

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#### **System Timing**

Figure 10 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

- 1. An external oscillator connected to pin 40.
- A crystal between pins 39 and 40.
- An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-2/3kHz. 50kHz. 40kHz. etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

#### COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6µA of guiescent current. They can supply ~1 µA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale,  $1.8m\Omega$  is near optimum and similarly  $180k\Omega$  for a 200.0mV scale.

#### Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C<sub>INT</sub> are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a  $750\Omega$  resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

#### **Auto-Zero Capacitor**

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32 µF capacitor is recommended. On the 2 Volt scale, a 0.033 µF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

#### Reference Capacitor

A 0.1 µF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 µF will hold the roll-over error to 0.5 count in this instance. Oscillator Components dell'ai il anatorico abanan arti

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate 0.45

equation f . For 48kHz clock (3 readings/second),  $R = 180k\Omega$ .

#### Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: VIN = 2VREF. Thus, for the 200.0mV and 2.000 Volt scale, VREF should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V<sub>RFF</sub> = 0.341V. A suitable value for integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for V<sub>IN</sub> ≠ 0. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

#### TYPICAL APPLICATIONS

The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

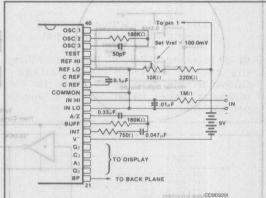
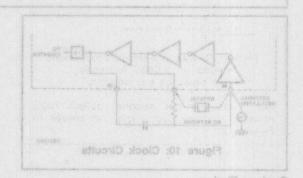


Figure 11: 7126 using the internal reference.

Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).



Floure 10 shows the clocking arrangement used in the An R-C pacificator using all three pins.

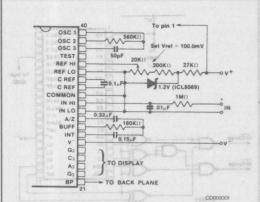


Figure 12: 7126 with an external band-gap reference (1.2V type).

IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.

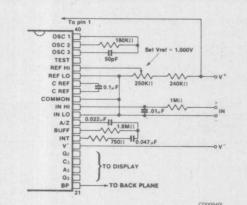


Figure 13: Recommended component values for 2.000V full scale,
3 readings per second.

For 1 reading per second, delete 750  $\!\Omega$  resistor, change C\_INT, ROSC to values of Figure 12.

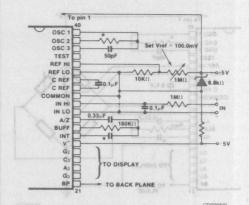


Figure 14: 7126 with Zener diode

Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.

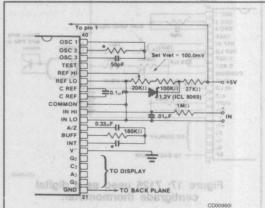


Figure 15: 7126 operated from single +5V supply.

An external reference must be used in this application, since the voltage between V <sup>+</sup> and V <sup>-</sup> is insufficient for correct operation of the internal reference.

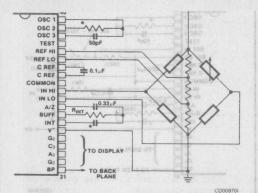


Figure 16: 7126 measuring ratiometric values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.

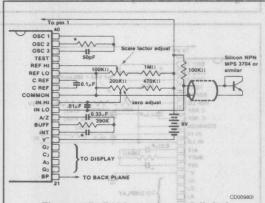
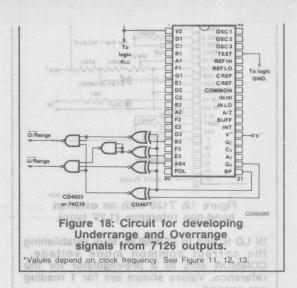
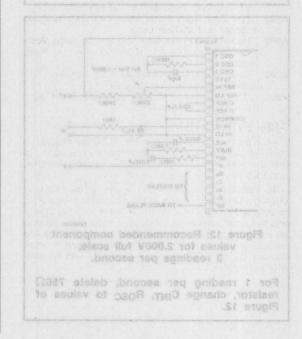
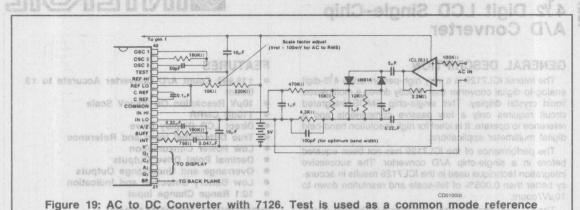


Figure 17: 7126 used as a digital centigrade thermometer.

A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.







level to ensure compatibility with most op-amps.

#### **APPLICATION NOTES**

- A016 "Selecting A/D Converters", by David Fullagar.
- A017 "The Integrating A/D Converter", by Lee Evans.
- A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
- A019 ''41/2-Digit Panel Meter Demonstrator/ Instrumentation Boards'', by Michael Dufort.
- A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
- A052 "Tips for Using Single-Chip 31/2-Digit A/D Converters", by Dan Watson.

#### 7126 EVALUATION KIT

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

Figure 2: Pin Configuration (outline dwg PL)

SOCLEBBLOC

### ICL7129

### 4<sup>1</sup>/<sub>2</sub> Digit LCD Single-Chip A/D Converter



#### GENERAL DESCRIPTION

The Intersil ICL7129 is a very high-performance 4 ½-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high-resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to  $10\mu V/count$ .

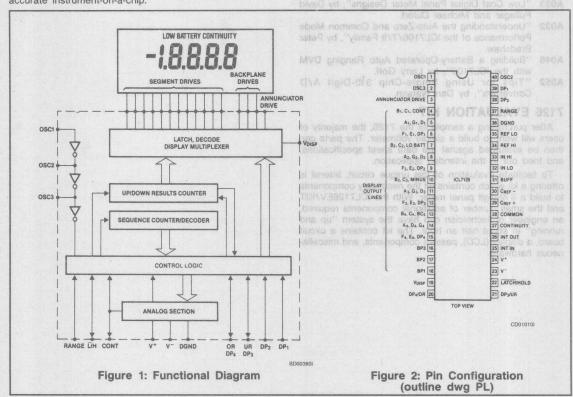
The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

#### **FEATURES**

- ±19,999 Count A/D Converter Accurate to ±3
  Count
- 10μV Resolution On 200mV Scale
- 110dB CMRR
- Direct LCD Display Drive
- True Differential Input and Reference
- Low Power Consumption
- Decimal Point Drive Outputs
- Overrange and Underrange Outputs
- Low Battery Detection and Indication
- 10:1 Range Change Input

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE	PACKAGE	
ICL7129CPL	0°C to +70°C	40-Pin Plastic	



#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltages (V <sup>+</sup> to V <sup>-</sup> )	Power Dissipation (Note 2)
Reference Voltage (REF HI or REF LO) V + to V-	Plastic package
Input Voltage (Note 1)	Operating Temperature 0°C to +70°C
(IN HI or IN LO)V <sup>+</sup> to V <sup>-</sup>	Storage Temperature65°C to +150°C
VDISP	Lead Temperature (Soldering, 10sec)300°C
Digital Input Pins	
1, 2, 19, 20, 21, 22, 27,	
37, 38, 39, 40DGND to V <sup>+</sup> /	TITITITI

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400 µÅ. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1mA. Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS  $V^-$  to  $V^+ = 9V$ ,  $V_{REF} = 1.00V$ .  $T_A = +25$ °C,  $f_{CLK} = 120$ kHz, unless otherwise noted.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V <sub>IN</sub> = 0V 200mV Scale	- 0000	0000	+ 0000	Counts
Zero Reading Drift	V <sub>IN</sub> = 0V 0°C < T <sub>A</sub> < +70°C	U40/	±0.5		μV/°C
Ratiometric Reading	V <sub>IN</sub> = V <sub>REF</sub> = 1000mV RANGE = 2V	9996	9999	10000	Counts
Range Change Accuracy	V <sub>IN</sub> = 0.10000V on Low Range ÷ V <sub>IN</sub> = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN} = +V_{IN} = 199 \text{mV}$	中 电通路管线点	1.5	3.0	
Linearity Error	200mV Scale	and the same of the same of the same	1.0	Carting passage of the Princip	Counts
Input Common-Mode Rejection Ratio	V <sub>CM</sub> = 1.0V, V <sub>IN</sub> = 0V 200mV Scale	r elust	110		dB
Input Common-Mode Voltage Range	V <sub>IN</sub> = 0V 200mV Scale	# N T - 1 T	(V <sup>-</sup> ) + 1.5 (V <sup>+</sup> ) - 1.0	a series promo	V
Noise (p-p Value not Exceeding 95% of Time)	V <sub>IN</sub> = 0V 200mV Scale	. W	m toward 14 mever sooks te	I of tugel	μV
Input Leakage Current	V <sub>IN</sub> = 0V, Pin 32, 33	weder	second alocale	to teat10)	pA) s
Scale Factor Tempco	V <sub>IN</sub> = 199mV 0°C < T <sub>A</sub> < + 70°C External V <sub>REF</sub> = Oppm/°C	gravino not augu	o eveweraups 2 an	ensig/ce8 AC	ppm/°C
COMMON Voltage calls test ant the bedge	V <sup>+</sup> to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V		0.6	er southe	mA
COMMON Source Current	$\Delta$ Common = $-0.1$ V		10	00 100100	μΑ
DGND Voltage prior evilage TU9700	V <sup>+</sup> to Pin 36 V <sup>+</sup> to V <sup>-</sup> = 9V	4.5	5.3	5.8	TVa
DGND Sink Current noc not been ed mad	ΔDGND = +0.5V		1.2	CR JUDIOCA	mA
Supply Voltage Range	V <sup>+</sup> to V <sup>-</sup> (Note 1)	6	9	12	V
Supply Current Excluding COMMON Current	V <sup>+</sup> to V <sup>-</sup> = 9V		1.0	3001.5	EG EG MA
Clock Frequency	(Note 1)	at at	120	of hu360	kHz S
VDISP Resistance	V <sub>DISP</sub> to V <sup>+</sup>	- al	omge 50 algeb	Output to	200 a0 kΩ   E
Low Battery Flag Activation Voltage Total Park TURN	V+ to V-	6.3	7.2	of such 7.7	A Ay Da, Ga
CONTINUITY Comparator Threshold Voltages	V <sub>OUT</sub> Pin 27 = HI V <sub>OUT</sub> Pin 27 = LO	100 Velgaio	of 200 200	400	mV 0
Pull-Down Current Vaccos + next seel at	Pins 37, 38, 39	yalgaic	01 10020 5	10	μΑ
"Weak Output" Current	Pin 20, 21 Sink/Source	daplay.	3/3	Backplane	μA
nk/Source	Pin 27 Sink/Source	,Exercit	3/9	Negativo	serov e
Pin 22 Source Current Pin 22 Sink Current		TEST STREET S	1000 3 mines		POASO 0

NOTES: 1. Device functionality is guaranteed at the stated Min/Max limits. However, accuracy can degrade under these conditions.

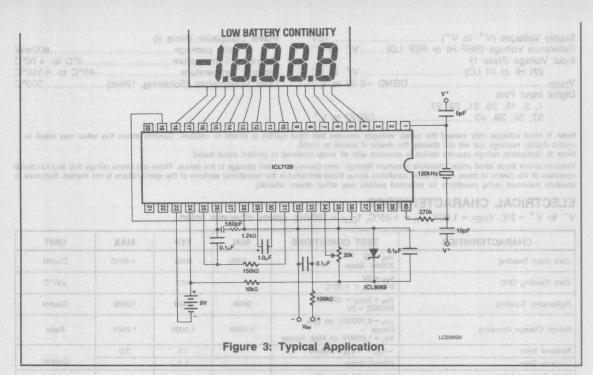


Table 1. Pin Descriptions

PIN	NAME	FUNCTION		
1	OSC1	Input to first clock inverter.		
2	OSC3	Output of second clock inverter.		
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.		
4	B <sub>1</sub> , C <sub>1</sub> , CONT	Output to display segments.		
5	A <sub>1</sub> , G <sub>1</sub> , D <sub>1</sub>	Output to display segments.		
6	F <sub>1</sub> , E <sub>1</sub> , DP <sub>1</sub>	Output to display segments.		
7	B <sub>2</sub> , C <sub>2</sub> , LO BATT	Output to display segments.		
8	A2, G2, D2	Output to display segments.		
9	F2, E2, DP2	Output to display segments.		
10	B <sub>3</sub> , C <sub>3</sub> , MINUS	Output to display segments.		
11	A <sub>3</sub> , G <sub>3</sub> , D <sub>3</sub>	Output to display segments.		
12	F <sub>3</sub> , E <sub>3</sub> , DP <sub>3</sub>	Output to display segments.		
13	B <sub>4</sub> , C <sub>4</sub> , BC <sub>5</sub>	Output to display segments.		
14	A <sub>4</sub> , D <sub>4</sub> , G <sub>4</sub>	Output to display segments.		
15	F4, E4, DP4	Output to display segments.		
16	BP3	Backplane #3 output to display.		
17	BP2	Backplane #2 output to display.		
18	BP1	Backplane #1 output to display.		
19	VDISP	Negative rail for display drivers.		
20	DP <sub>4</sub> /OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.		

PIN	NAME	FUNCTION	
		FUNCTION	
21	DP3/UR	INPUT: Second most significant	
	VIN = OV, Pin 2	decimal point on when HI. OUTPUT: Pulled HI when result count	
	Vm991 = 191V	is less than ±1,000.	
22	LATCH/HOLD	INPUT: When floating, A/D converter	
	V to Pin 28	operates in the free-run mode. When pulled HI, the last displayed reading is	
	△Common = +	held. When pulled LO, the result	
	and the second second	counter contents are shown incrementing	
	_ = GORBRODE = _	during the de-integrate phase of	
	V to Pin 36	cycle. OUTPUT: Negative going edge occurs	
	ADGNO - ON	when the data latches are updated.  Can be used for converter status	
	SUN THE PROPERTY	signal.	
23	V-	Negative power supply terminal.	
24	V+	Positive power supply terminal, and	
	(Note 1)	positive rail for display drivers.	
25	INT IN	Input to integrator amplifier.	
26	INT OUT	Output of integrator amplifier.	
27	CONTINUITY	INPUT: When LO, continuity flag on the	
	Vous Pin 27 =	display is off. When HI, continuity flag	
	YOUT PID 27 H	is on. OUTPUT: HI when voltage between inputs	
	Pins 37, 38, 3	is less than +200mV. LO when	
	Pin 20, 21 Sin	voltage between inputs is more than + 200mV.	

Table 1. Pin Descriptions (Cont.)

PIN	NAME	FUNCTION		
28	COMMON	Sets common-mode voltage of 3.2V below V + for DE, 10X, etc. Can be used as pre-regulator for external reference.		
29	C <sub>REF</sub> +	Positive side of external reference capacitor.		
30	CREF	Negative side of external reference capacitor.		
31	BUFFER	Output of buffer amplifier.		
32	IN LO	Negative input voltage terminal.		
33	IN HI	Positive input voltage terminal.		
34	REF HI	Positive reference voltage input terminal		
35	REF LO	Negative reference voltage input terminal.		
36	DGND	Ground reference for digital section.		
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.		
38	DP <sub>2</sub>	Internal 3µA pull-down. When HI, decimal point 2 will be on.		
39	DP <sub>1</sub>	Internal 3µA pull-down. When HI, decimal point 1 will be on.		
40	OSC2	Output of first clock inverter. Input of second clock inverter.		

#### **DETAILED DESCRIPTION**

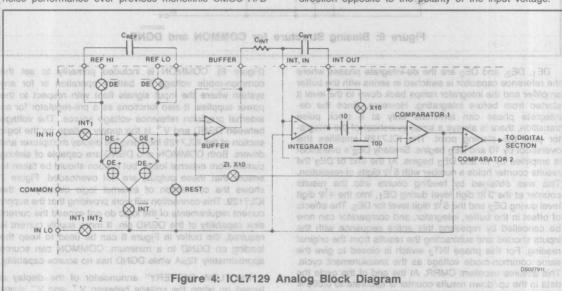
Intersil's ICL7129 is a uniquely designed single-chip A/D converter. It features a new "successive integration" technique to achieve 10 µV resolution on a 200 mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D

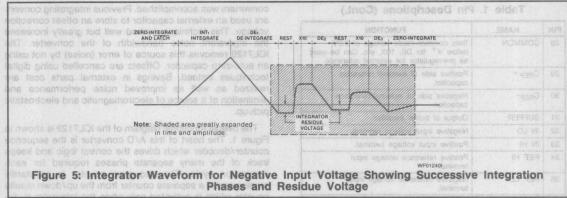
converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are cancelled using digital techniques instead. Savings in external parts cost are realized as well as improved noise performance and elimination of a source of electromagnetic and electrostatic pick-up.

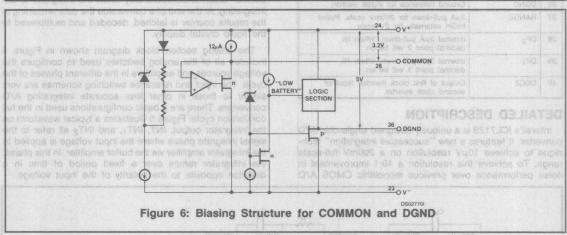
The overall functional diagram of the ICL7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is deintegrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 4 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 5 illustrates a typical waveform on the integrator output. INT, INT1, and INT2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

COMMON. DGND. AND "LOW BATTERY"







DE1, DE2, and DE3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the deintegrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE2 begins. Similarly DE2's overshoot is amplified by 10 and DE3 begins. At the end of DE3 the results counter holds a number with 51/2 digits of resolution. This was obtained by feeding counts into the results counter at the 31/2 digit level during DE1, into the 41/2 digit level during DE2 and the 51/2 digit level for DE3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.005% of full-scale and is sent to the display driver for decoding and multiplexing.

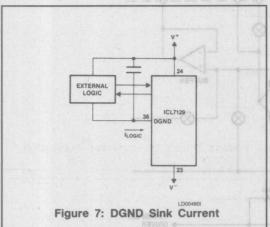
#### COMMON, DGND, AND "LOW BATTERY"

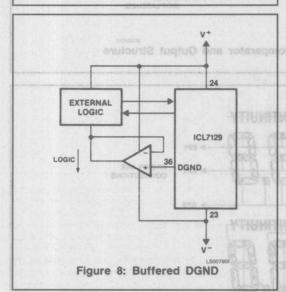
The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes

(Figure 6). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V + is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 7 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 8 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12µA while DGND has no source capability.

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V<sup>+</sup> and V<sup>-</sup> drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V<sup>-</sup> rail in Figure 6. As the supply voltage decreases, the n-channel transistor connected to the V-rail eventually turns off and

the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

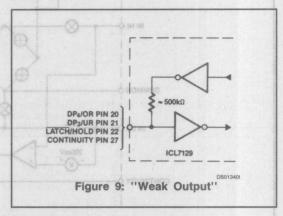




## I/O PORTS

Four pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described in the Pin Description table (Table 1). If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V $^+$  (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 9. Since there is approximately  $500 k\Omega$  in series with

the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to  $3\mu\rm A$ , nominally, and the input switching threshold is typically DGND  $^+2\rm V$ .

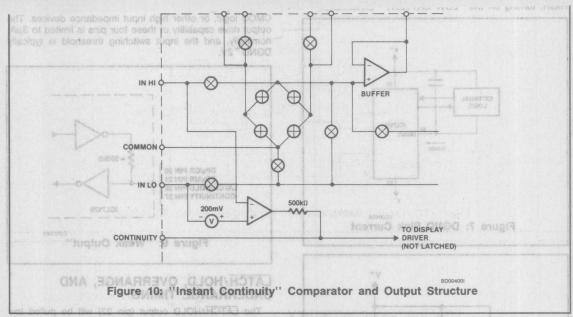


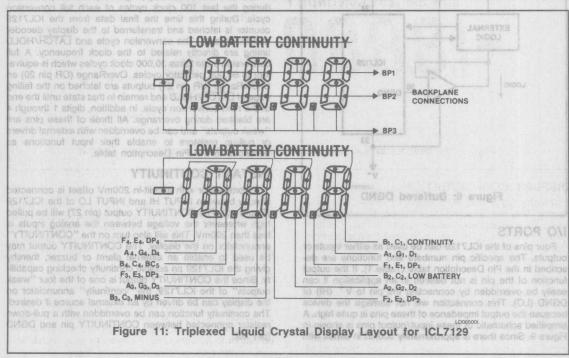
# LATCH/HOLD, OVERRANGE, AND UNDERRANGE TIMING

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) an UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Description table.

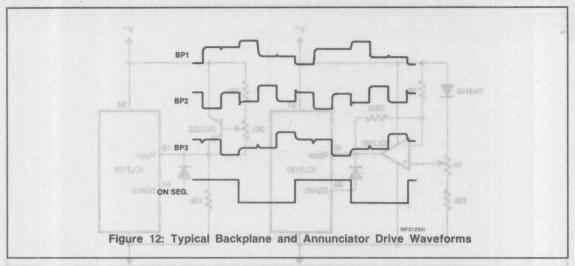
#### **INSTANT CONTINUITY**

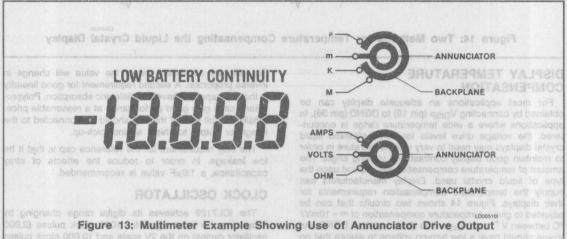
A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 10). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability. Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).





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## DISPLAY CONFIGURATION OF A SOLAR PROPERTY OF THE PROPERTY OF T

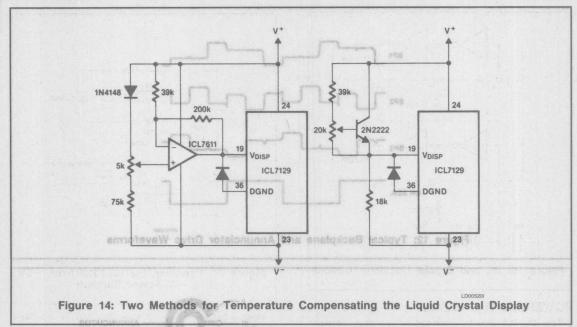
The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 11. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

#### ANNUNCIATOR DRIVE

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from VDISP to V<sup>+</sup> and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 12 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 13.

swing of A2.5V at full-scale. For a 150kQ integrating



## **DISPLAY TEMPERATURE** COMPENSATION

For most applications an adequate display can be obtained by connecting VDISP (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 14 shows two circuits that can be adjusted to give a temperature compensation of ≈+10mV/ °C between V + and Voisp. The diode between DGND and V<sub>DISP</sub> should have a low turn-on voltage to assure that no forward current is injected into the chip if VDISP is more negative than DGND.

### COMPONENT SELECTION

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is no auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected to be high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of  $150k\Omega$  should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail (≈0,7V). This gives an optimum swing of ≈2.5V at full-scale. For a 150kΩ integrating resistor and 2 conversions per second the value is 0.10μF.

For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0 µF value is recommended.

#### CLOCK OSCILLATOR

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2.000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

In low resolution applications, where the converter uses only 3 1/2 digits and 100 μV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from fosc = 0.45/RC. However, when the converter is used to its full potential (4½ digits and 10μV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 15. Its earl CR segments, BPC has all O ent to its

umns) are connected in groups of three bringing all



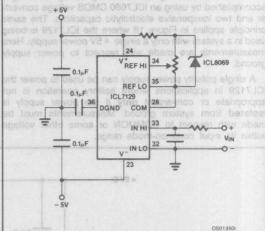


Figure 16: Powering the ICL7129 from +5V and -5V Power Supplies

**POWERING THE ICL7129** 

5pF

120kHz

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 16, 17, and 18 show various powering modes that may be used with the ICL7129.

Figure 15: RC and Crystal Oscillator Circuits

₹75k 51pF

≤ 270kΩ

10nF

ICL7129

ICI 7129

The standard supply connection using a 9V battery is shown in Figure 3.

The power connection for systems with +5V and -5V supplies available is shown in Figure 16. Notice that measurements are with respect to ground. COMMON is not connected to INPUT LO but is used only as a pre-regulator for the external voltage reference.

It is important to notice that in Figure 16, digital ground of the ICL7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V <sup>+</sup> terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 7 and 8. In Figure 7, DGND is used as the negative supply rail for external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 8. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND lew. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

When a battery voltage between 3.8V and 7V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 17.

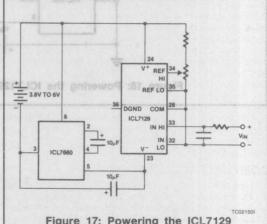
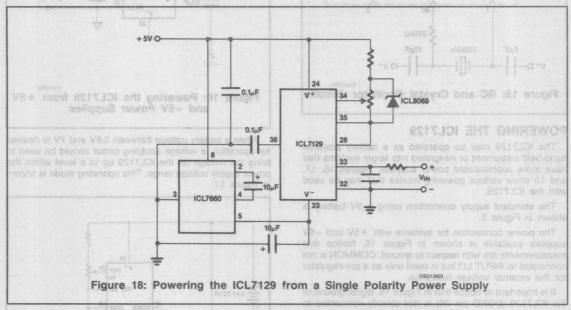


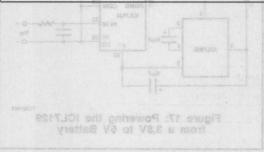
Figure 17: Powering the ICL7129 from a 3.8V to 6V Battery

accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 18 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

The COMMON output of the ICL7129 has a temperature coefficient of  $\pm 80 \text{ppm/}^{\circ}\text{C}$  typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram in Figures 3 and 18 show the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129, and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.





rower supply ground. DGND is set internally to approxinately 5V less than the V\* terminal and is not intended to
be used as a power input pin. It may be used as the ground
elerence for external logic, as shown in Figure 7 and 8. In
subject 8. DGND is used as the negative supply rail for
systemal logic provided that the supply current to the
systemal logic does not cause excessive loading on DGND.
The DGND output can be buffered as shown in Figure 8.
GC7128 keeping the load on DGND lew. This treatment of
the oxternal logic used to make compatibility when
the external logic used to the UC7129.

# GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistor and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming da vissend attend

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent.

The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The VREF input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

## FEATURES GUIDO OF BAR WAR MARY LINE

- 14-Bit Linearity (0.003% FSR)
   No Gain Adjustment Necessary
- Microprocessor-Compatible With Double Buffered
- Bipolar Application Requires No Extra Adjustments or External Resistors
- Low Linearity and Gain Temperature Coefficients
- Low Power Dissipation
- **Full Four-Quadrant Multiplication**

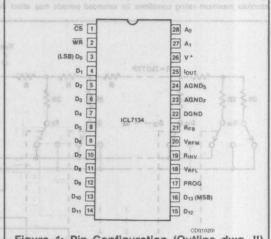


Figure 1: Pin Configuration (Outline dwg JI)

### ORDERING INFORMATION

NON LINEADITY	E(0 + ∞ T	TEMPERATURE RANGE								
NON-LINEARITY	0°C to +70°C	-25°C to +85°C	-55°C to +125°C							
Bipolar Versions										
0.01% (12-bit) 0.006% (13-bit) 0.003% (14-bit)	ICL7134BJCJI ICL7134BKCJI ICL7134BLCJI	ICL7134BJIJI ICL7134BKIJI ICL7134BLIJI	ICL7134BJMJI ICL7134BKMJI ICL7134BLMJI							
Unipolar Versions										
0.01% (12-bit) 0.006% (13-bit) 0.003% (14-bit)	ICL7134UJCJI ICL7134UKCJI ICL7134ULCJI	ICL7134UJIJI ICL7134UKIJI ICL7134ULIJI	ICL7134UJMJI ICL7134UKMJI ICL7134ULMJI							

PACKAGE: 28-pin CERDIP only

## **ABSOLUTE MAXIMUM RATINGS (Note 1)**

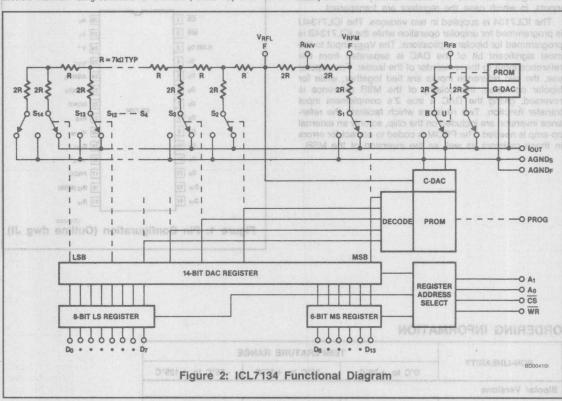
Supply Voltage (V + to DGND)	0.3V	to 7.5V
VRFL, VRFM, RINV, RFB to DGND		±15V
IOUT, AGNDF, AGNDS	0.1\	to V+
Current in AGNDs, AGNDF	toers.J. N	25mA
An, Dn, WR, CS, PROG0.	3V to V	++0.3V

Operating Temperature Range
ICL7134XXC 0°C to +70°C
ICL7134XXI25°C to +85°C
ICL7134XXM55°C to +125°C
Storage Temperature Range65°C to +150°C
Power Dissipation (Note 2)500mW
Derate Linearly Above 70°C @ 10mW/°C
Lead Temperature (Soldering 10sec) 300°C

Note 1: All voltages with respect to DGND.

Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## ELECTRICAL CHARACTERISTICS (V+ = 5V, V<sub>REF</sub> = 10V, T<sub>A</sub> = 25°C unless otherwise specified.)

OVMDOL	DATE	AMETER	TEST SOURIES		LIMITS	Unipolar Ver		
SYMBOL	PAH	AMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
	Resolution	NAME OF STREET STREET	RANCHOT COMPROT	14	1-180	11 - 14	Bits	
	Non-Linearity	J	Test Figure 4	-	1	0.012	% FSR	
		K	(Notes 1 and 2)	yle.	a 910A	0.006	% FSR	
		L				0.003	% FSR	
	Non-Linearity Tempe	rature Coefficient (Note 3)	Operating Temperature Range		1	2	ppm/°C	

6

FEEDTHROUGH ERROR: Error caused by capacitive cou-

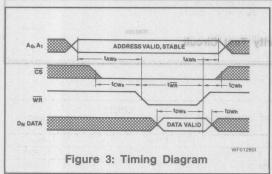
## **ELECTRICAL CHARACTERISTICS (CONT.)**

			LIMITS	HA MINE MAN			
SYMBOL	PARAMETE	R enoligh	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain Error	J	Test Figure 4	and the same		0.024	% FSR
	DESCRIPTIO	-K-EMIE   3	(Notes 1 and 2)	0.3903		0.012	% FSR
tot VG + ni all	Used for programming only.	L DORG	low).	d (active	ing Selec	0.006	% FSR
	Gain Error Temperature Coeff	icient (Note 3)	3	W testerity	2	8	ppm/°C
	Monotonicity	J	taleiges in register	12	And Leading		Bits
investing	Summing node for reference amplifier.	K VINIA	Insulinois -	13	0.4		Bits
	(Note 3)	L	madrage	14		1	Bits
lork of the s	IOUT Leakage Current	Pep	T <sub>A</sub> = +25°C			10	
nuqueo e	resolvator replant for votage	940	Operating Temperature Range	FM. 123	50		nA
PSRR	Power Supply Rejection	CMBC	$T_A = +25$ °C, $\Delta V^+ = \pm 10$ %	10 3 12 13	10	100	
Use to carry	Analog Ground torce lines.	AGNO:	Operating Temperature Range			150-	ppm/V
GNuoriD	Output Current Settling Time		The state of the s		1		μs
South o	Feedthrough Error	ICL7134U	V <sub>REF</sub> = ±10V, 2kHz Sinewave		250		353
Reference point	Analog Ground sense line, if the she	ICL7134B	S ena		500		μVp-p
ZREF	Reference Input Resistance		V <sub>RFL</sub> = V <sub>RFM</sub> (Unipolar Mode)	4.0	6.31	10	kΩ
Cour	Output Capacitance	ruoi	DAC Register = All 0's		160		801 8
	Positive voltage:		DAC Register = All 1's	e de la constante	235		oPF 8
	Output Noise	;A	Equivalent Johnson Res.	1	7		kΩ
VINL	Low State Input o assubbA	bA .	Operating Temperature Range		11.72	0.8	2.V
VINH	High State Input	THE RESERVE THE PARTY OF THE PA	Operating Temperature Range	2.4	87 H		N O
lin	Logic Input Current		0 ≤ V <sub>IN</sub> ≤ V +		LANGUET DE POUTUR	1.0	μΑ
C <sub>lin</sub>	Logic Input Capacitance		(Note 3)		15		pF
V+	Supply Voltage Range (Note	4)	Functional Operation	3.5		6.0	V
1 <sup>±</sup> 3	Supply Current		(Excluding Ladder)		1.0	2.5	mA
	Long Term Stability	BEN YEAR MALE	1000 Hours, +125°C (Note 3)		10		ppm/month

NOTES: 1. Full-Scale Range (FSR) is 10V for unipolar mode, 20V (±10V) for bipolar mode, 2. Using internal feedback and reference inverting resistors.
3. Guaranteed by design, not production tested.
4. Full scale tested to 0.040% FSR.

## AC CHARACTERISTICS (V + = 5V, see Timing Diagram)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>AWs</sub>	Address-WRite Set-Up Time (Min)				100	
tAWh	Address-WRite Hold Time (Min)	(Note 3)	13030		0	
tcws	Chip Select-WRite Set-Up Time (Min)	(Note 3)			0	
tcwh	Chip Select-WRite Hold Time (Min)	(Note 3)			0	ns
twR	WRite Pulse Width Low (Min)	(889)	Lebs Com		200	
t <sub>DWs</sub>	Data-WRite Set-Up Time (Min)	30 H26 T36 S) T18	1921	NO GO	200	
tpWh	Data-WRite Hold Time (Min)	(Note 3)	TY -	1 5 DET 1 THE	0	E TH



#### **DEFINITION OF TERMS**

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a straight line function between endpoints. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V<sub>REF</sub> range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2-n) (VRFF). A bipolar converter of n bits has a resolution of  $[2^{-(n-1)}]$ [VREF]. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

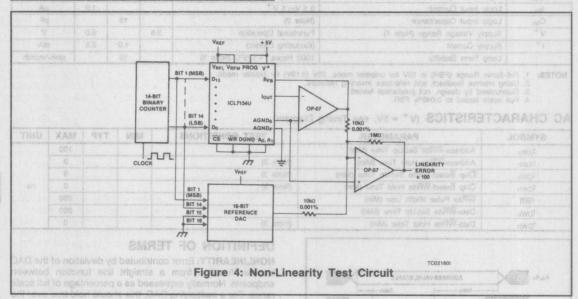
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Table 1: Pin Descriptions

s I sal

PIN	SYMBOL		DESCRIPTION				
1	CS and add	Chip Select (active low). Enables register write.					
2	WR	WRite, (active low). Writes in register. Equivalent to CS.					
3	D <sub>0</sub>	Bit 0	Least significant				
4	D <sub>1</sub>	Bit 1	PE STATE OF THE ST				
5	D <sub>2</sub>	Bit 2					
6	D <sub>3</sub>	Bit 3	emperature Range				
7	D <sub>4</sub>	Bit 4	#01± = *VA				
8	D <sub>5</sub>	Bit 5	Input				
9	D <sub>6</sub>	Bit 6	Data Data				
10	D <sub>7</sub>	Bit 7	Bits				
11	D <sub>8</sub>	Bit 8	(High = True)				
12	D <sub>9</sub>	Bit 9	F All O's				
13	D <sub>10</sub>	Bit 10	0 T BA = 1				
14	D <sub>11</sub>	Bit 11	streen Res.				
15	D <sub>12</sub>	Bit 12	eprefil enuisagem				
16	D <sub>13</sub>	Bit 13	Most significant.				

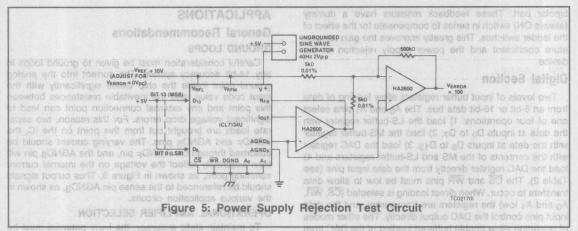
PIN	SYMBOL	DESCRIPTION					
17	PROG	Used for programming only. Tie to +5V for normal operation.					
18	VRFL	VREF for lower bits.					
19	RINV	Summing node for reference inverting amplifier.					
20	VRFM	VREF for MSB only (bipolar).					
21	RFB	Feedback resistor for voltage output applications.					
22	DGND	Digital GrouND return.					
23	AGNDF	Analog GrouND force lines. Use to carry current from internal Analog GrouND connections. Tied internally to AGNDs.					
24	AGNDS	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to AGNDF.					
25	lour	Current output pin. 1/2/20					
26	V+	Positive voltage.					
27	A <sub>1</sub>	Address 1					
28	Ao	Address 0 Control register lines					

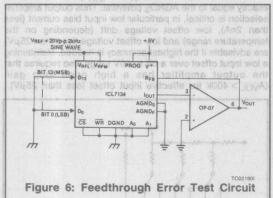


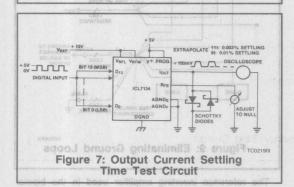
RESOLUTION: Value of the LSB. For example, a unipolar convertor with n bits has a resolution of (2<sup>-n</sup>) (Vacc). A bigolar converter of n bits has a resolution of [2<sup>-(n-1)</sup>] [Vacc). Fasolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input strinulus, i.e., 0 to full-scale.

Figure 3: Timing Diagram







## DETAILED DESCRIPTION

The ICL7134 consists of a 14-bit primary DAC, two PROM controlled correction DACs, input buffer registers, and microprocessor interface logic (Figure 2). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC, or G-DAC, diverts up to 2% of the feedback resistor's current to Analog GounND and reduces the gain error to less than 1 LSB, or 0.006%. The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12bit linearity correction DAC, or C-DAC. For every combination of the primary DAC's 5 most significant bits, a different C-DAC code is selected. This allows correction of superposition errors, caused by bit interaction on the primary resistor ladder's current output bus and by voltage nonlinearity in the feedback resistor. Superposition errors cannot be corrected by any method which corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging. These packaging shifts limit the accuracy that can be achieved using wafer level correction methods such as laser trimming, which has also been found to degrade the time stability of thin film resistors at the 14-bit level.

#### **Analog Section**

The ICL7134 inherently provides both unipolar and bipolar operation. The bipolar application circuit (Figure 8) requires one additional op-amp but no external resistors. The two on-chip resistors, Ri<sub>INV1</sub> and R<sub>INV2</sub>, together with the op-amp, form a voltage inverter which drives the MSB reference terminal, V<sub>RFM</sub>, to -V<sub>REF</sub>, where V<sub>REF</sub> is the voltage applied at the less significant bits' reference terminal, V<sub>RFL</sub>. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V<sub>RFM</sub> and V<sub>RFL</sub> can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V<sub>RFM</sub> and V<sub>RFL</sub> terminals are both tied to V<sub>REF</sub>, and the R<sub>INV</sub> pin is left unconnected.

Since the PROM correction codes required are different for bipolar and unipolar operation, the ICL7134 is available in two different versions; the ICL7134U, which is corrected for unipolar operation, and the ICL7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from 'R' in the unipolar device to '2R' in the

bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

## **Digital Section**

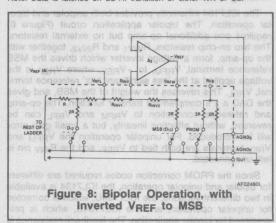
Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The  $A_0$  and  $A_1$  pins select one of four operations: 1) load the LS-buffer register with the data at inputs  $D_0$  to  $D_7;\,2)$  load the MS-buffer register with the data at inputs  $D_8$  to  $D_{13};\,3)$  load the DAC register with the contents of the MS and LS-buffer registers and 4) load the DAC register directly from the data input pins (see Table 2). The  $\overline{CS}$  and  $\overline{WR}$  pins must be low to allow data transfers to occur. When direct loading is selected  $\overline{(CS},\overline{WR},A_0$  and  $A_1$  low) the registers are transparent, and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to  $V^+$  (+5V).

Table 2: Data Loading Controls

C	ONTR	ROLI		on of the primary DAC's 5 most sig			
A <sub>0</sub>	A <sub>1</sub>	CS	10000	ewells ICL7134 OPERATION DATE			
X	X	X	Sopra	No operation, device not selected			
X	X	910	X	borltam vns yd beloe noo ad tonn			
0	0	0	0	Load all registers from data bus.			
0	alolag	0	0	Load LS register from data bus.			
111	0	0	0	Load MS register from data bus.			
dh ei	equal t lev	0	0	Load DAC register from MS and LS register.			

Note: Data is latched on LO-HI transition of either WR or CS.



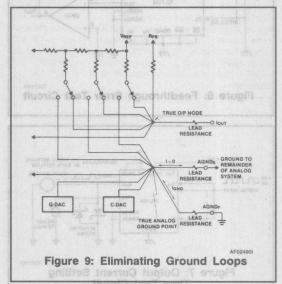
#### **APPLICATIONS**

# General Recommendations GROUND LOOPS

Careful consideration must be given to ground loops in any 14-bit accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, the AGNDF and AGNDS pins. The varying current should be absorbed through the AGNDF pin, and the AGNDS pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 9. Thus output signals should be referenced to the sense pin AGNDS, as shown in the various application circuits.

#### **OPERATIONAL AMPLIFIER SELECTION**

To maintain static accuracy, the I<sub>OUT</sub> potential must be exactly equal to the AGNDs potential. Thus output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than  $25\mu V$ ) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10V range also requires that the output amplifier has a high open loop gain (AVOL > 400k for effective input offset less than  $25\mu V$ ).



The reference inverting amplifier used in the bipolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than  $50\mu V$ ), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the Analog GrouND line (op-amp A2 in Figure 11). This opamp should be selected for low bias current (less than 2nA) and low offset voltage (less than  $50\mu V$ ).

The op-amp requirements can be readily met by use of an ICL7650 chopper stabilized device. For faster settling time, an HA26XX can be used with an ICL7650 providing automatic offset null (see A053 for details).

The output amplifier's non-inverting input should be tied directly to AGNDs. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

### POWER SUPPLIES

The V<sup>+</sup> (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V<sup>+</sup>, which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V<sup>+</sup> for proper operation.

## Unipolar Binary Operation (ICL7134U)

The circuit configuration for unipolar mode operation (ICL7134U) is shown in Figure 10. With positive and negative V<sub>RFF</sub> values the circuit is capable of two-quadrant multiplication. The "digital input code/analog output value" table for unipolar mode is given in Table 3. The Schottky diode (HP5082-2811 or equivalent) protects lour from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers. For applications where the output reference ground point is established somewhere other than at the DAC, the circuit of Figure 10 can be used. Here, op-amp A2. removes the slight error due to IR voltage drop between the internal Analog GrouND node and the external ground connection. For 13bit or lower accuracy, omit A2 and connect AGNDF and AGNDs directly to ground through as low a resistance as possible.

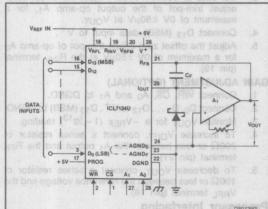
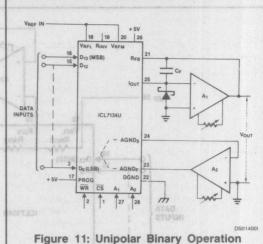


Figure 10: Unipolar Binary, Two-Quadrant Multiplying Circuit



with Forced Ground

Table 3: Code Table — Unipolar Binary Operation

	DIGITAL INPUT													ANALOG OUTPUT
					1									-VREF(1-1/2 <sup>14</sup> )
1	0	0	0	0	0	0	0	0	0	0	0	0	191	-VREF(1/2 + 1/2 <sup>14</sup> )
1	0	0	0	0	0	0	0	0	0	0	0	0	0	-VREF/2
					1									-VREF(1/2-1/2 <sup>14</sup> )
0	0	0	0	0	0	0	0	0	0	0	0	0	nei	-VREF(1/2 <sup>14</sup> )
0	0	0	0	0	0	0	0	0	0	0	0	0	0	CL7134B) 0

## ZERO OFFSET ADJUSTMENT TO THE PROPERTY OF THE

- 1. Connect all data inputs and  $\overline{WR}$ ,  $\overline{CS}$ ,  $A_0$  and  $A_1$  to DGND.
- Adjust offset zero-adjust trim-pot of the operational amplifier A<sub>2</sub>, if used, for a maximum of  $0V \pm 50 \mu V$  at AGNDs.
- Adjust the offset zero-adjust trim-pot of the output op-amp, A<sub>1</sub>, for a maximum of 0V ±50µV at V<sub>OUT</sub>.

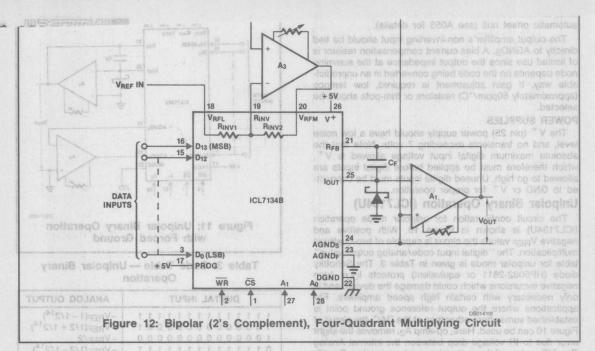
#### GAIN ADJUSTMENT (OPTIONAL)

- Connect all data inputs to V<sup>+</sup>, connect WR, CS, A<sub>0</sub> and A<sub>1</sub> to DGND.
- 2. Monitor VOUT for a -VREF (1-1/214) reading.
- To decrease V<sub>OUT</sub>, connect a series resistor of 100Ω or less between the reference voltage and the V<sub>RFM</sub> and V<sub>RFL</sub> terminals (pins 20 and 18).
- 4. To increase  $V_{OUT}$ , connect a series resistor of  $100\Omega$  or less between A<sub>1</sub> output and the RFB terminal (pin 21).

DEFECT ADJUSTIMENT

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# Bipolar (2's Complement) Operation (ICL7134B)

The circuit configuration for bipolar mode operation (ICL7134B) is shown in Figure 12. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. The 'digital input code/analog output value' table for bipolar mode is given in Table 4. Amplifier A3, together with internal resistors RINV1 and RINV2, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately –VREF, so the MSB's weight is reversed from the polarity of the other bits. In addition, the ICL7134B's feedback resistance is switched to 2R under PROM control, so that the bipolar output range is +VREF to –VREF (1 – ½13). Again, the grounding arrangement of Figure 11 can be used, if necessary.

Table 4: Code Table — Bipolar (2's Complement) Operation

			D	IG	IT	Al	. 1	NI	U	pl				ANALOG OUTPUT
0	d	84	1	1	1	1	1	9	p	ep:	9	19	1TU	-VREF(1-1/2 <sup>13</sup> )
0	0	0	0	0	0	0	0	0	0	0	0	0	4 dec	-VREF(1/2 <sup>13</sup> )
0	0	0	0	0	0	0	0	0	0	0	0	0		(pin 0)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	V <sub>REF</sub> (1/2 <sup>13</sup> )
1	0	0	0	0	0	0	0	0	0	0	0	0		VREF(1-1/2 <sup>13</sup> )
1	0	0	0	0	0	0	0	0	0	0	0	0	0	VREF

#### OFFSET ADJUSTMENT

 Connect all data inputs and WR, CS, A<sub>0</sub> and A<sub>1</sub> to DGND.

- Adjust the offset zero-adjust trim-pot of the operational amplifier A<sub>2</sub>, if used, for a maximum of 0V ±50µV at AGNDs.
- 3. Set data to 00000....00. Adjust the offset zero-adjust trim-pot of the output op-amp  $A_1$ , for a maximum of  $0V \pm 50 \mu V$  at  $V_{OUT}$ .
- 4. Connect D<sub>13</sub> (MSB) data input to V+
- Adjust the offset zero-adjust trim-pot of op-amp Ag for a maximum of 0V ±50μV at the R<sub>INV</sub> terminal (pin 19).

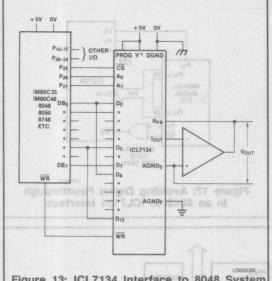
### GAIN ADJUSTMENT (OPTIONAL)

- 1. Connect WR, CS, Ao and A1 to DGND.
- Connect D<sub>0</sub>, D<sub>1</sub>... D<sub>12</sub> to V<sup>+</sup>, D<sub>13</sub> (MSB) to DGND.
- 3. Monitor VOUT for a -VBFF (1 1/213) reading.
- 4. To increase  $V_{OUT}$ , connect a series resistor of  $200\Omega$  or less between the  $A_1$  output and the RFB terminal (pin 21).
- 5. To decrease  $V_{OUT}$ , connect a series resistor of  $100\Omega$  or less between the reference voltage and the  $V_{RFL}$  terminal (pin 18).

### **Processor Interfacing**

The ease of interfacing to a processor can be seen from Figure 14, which shows the ICL7134 connected to an 8035 or any other processor such as an 8049. The data bus feeds into both register inputs; three port lines, in combination with the  $\overline{\rm WR}$  line, control the byte-wide loading into these registers and then the DAC register. A complete DAC set-up requires 4 write instructions to the port, to set up the address and  $\overline{\rm CS}$  lines, and 3 external data transfers, one a dummy for the final transfer to the DAC register.





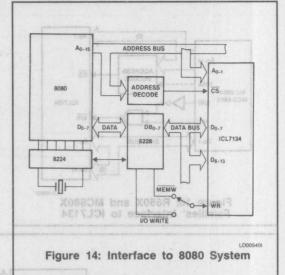
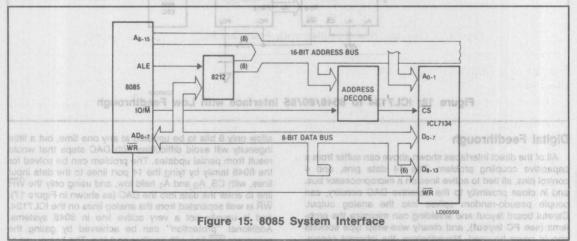
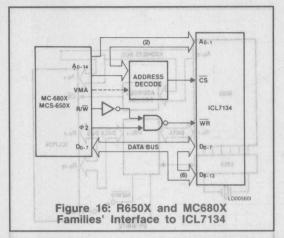


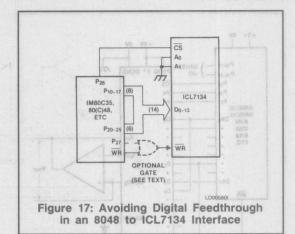
Figure 13: ICL7134 Interface to 8048 System

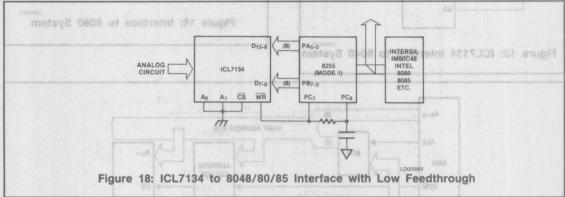


A similar arrangement can be used with an 8080A, 8228, and 8224 chip set. Figure 14 shows the circuit, which can be arranged as a memory-mapped interface (using MEMW) or as an I/O-mapped interface (using I/O WRITE). See A020 and R005 for discussions of the relative merits of memory-mapped versus I/O-mapped interfacing, as well as some other ideas on interfacing with 8080 processors. The 8085 processor has a very similar interface, except that the control lines available are slightly different, as shown in

Figure 15. The decoding of the IO/M line, which controls memory-mapped or I/O-mapped operation, is arbitrary, and can be omitted if not necessary. Neither the MC680X nor R650X processor families offer specific I/O operations. Figure 16 shows a suitable interface to either of these systems, using a direct connection. Several other decoding options can be used, depending on the other control signals generated in the system. Note that the R650X family does not require VMA to be decoded with the address lines.







## Digital Feedthrough

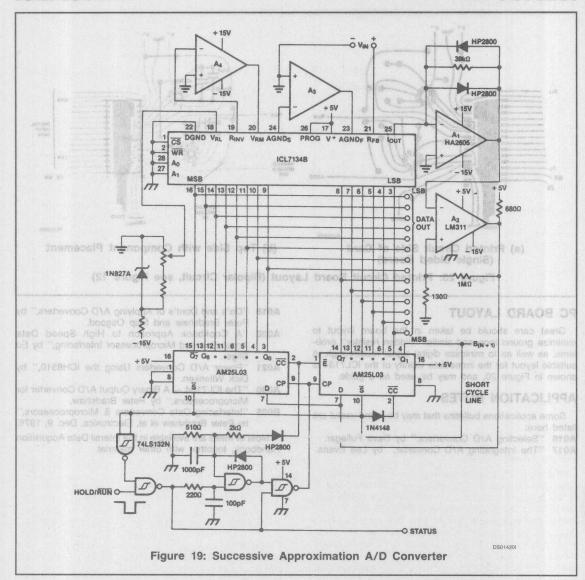
All of the direct interfaces shown above can suffer from a capacitive coupling problem. The 14 data pins, and 4 control pins, all tied to active lines on a microprocessor bus, and in close proximity to the sensitive DAC circuitry, can couple pseudo-random spikes into the analog output. Careful board layout and shielding can minimize the problems (see PC layout), and clearly wire-wrap type sockets should never be used. Nevertheless, the inherent capacitance of the package alone can lead to unacceptable digital feedthrough in many cases. The only solution is to keep the digital input lines as inactive as possible. One easy way to do this is to use the peripheral interface circuitry available with all the systems previously discussed. These generally

result from partial updates. The problem can be solved for the 8048 family by tying the 14 port lines to the data input lines, with CS,  $A_0$  and  $A_1$  held low, and using only the  $\overline{WR}$  line to enter the data into the DAC (as shown in Figure 17).  $\overline{WR}$  is well separated from the analog lines on the ICL7134, and is usually not a very active line in 8048 systems. Additional "protection" can be achieved by gating the processor  $\overline{WR}$  line with another port line. The heavy use of port lines can be alleviated by use of the IM82C43 port expander. The same type of technique can be employed in the 8080/85 systems by using an 8255 PIA (peripheral Interface adapter) (Figure 18) and in the MC680X and R650X systems by using an MC6820 (R6520) PIA.

allow only 8 bits to be updated at any one time, but a little

ingenuity will avoid difficulties with DAC steps that would

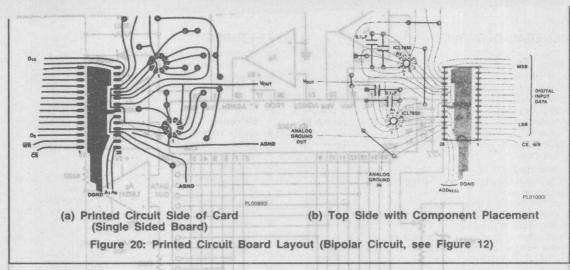
some other ideas on interfacing with 8080 processors. The 8086 processor has a very smiler interface, except that the control tines available are stigntly different, as shown in



## Successive Approximation A/D Converters

Figure 19 shows an ICL7134B-based circuit for a bipolar input high speed A/D converter, using two AM25L03s to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2605 front-end amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7650 is probably advisable (see A053). The clock, using two Schmitt trigger TTL gates, runs at a slower rate for the first 8

bits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; if fewer bits are required, it can be moved up accordingly. The circuit will free-run if the  $HOLD/\overline{RUN}$  input is held low, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS output indicates when the device is operating, and the falling edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D<sub>13</sub>) on an ICL7134U to pin 14 on the first AM25L03, deleting the reference inversion amplifier A<sub>4</sub>, and tying  $V_{REM}$  to  $V_{REL}$ .



#### PC BOARD LAYOUT

Great care should be taken in the board layout to minimize ground loop and similar "hidden resistor" problems, as well as to minimize digital signal feedthrough. A suitable layout for the immediate vicinity of the ICL7134 is shown in Figure 20, and may be used as a guide.

#### APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters," by Dave Fullagar.
A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

A021 "Power A/D Converters Using the ICH8510," by Dick Wilenken.

A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Most of these are available in the Intersil Data Acquisition Handbook, together with other material.

Igure 19: Successive Approximation A/D Converte

eits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; it fewer bits are required, it can be moved up accordingly. The circuit will tree-run if the HOLD/RUN input is held tow, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS that time. A low-going pulse will restart it. The STATUS talking edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D12) on an iCLT13AU to pin 14 on the first AM25LO3, deleting the reference inversion amplifier As, and what Versu.

Figure 19 shows an ICL7134B-based circuit for a bipolar imput high speed A/D converter, using two AM25L039 to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2805 front-and amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7860 is probably advisable (see A053). The clock, using two Schnittt inger ITL gates, runs at a slower rate for the first 5.

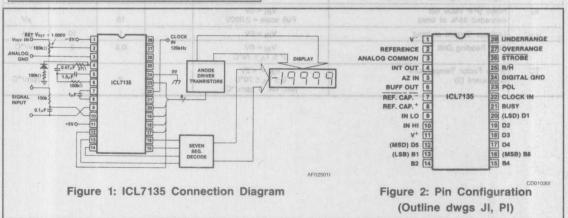
The intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10 µV, zero drift of less than 1µV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDER-RANGE, RUN/HOLD and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

### ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7135CJI	0°C to +70°C	28-Pin CERDIP
ICL7135CPI	0°C to +70°C	28-Pin Plastic DIP
ICL7135EV/KIT		ation Kit passive components)

## FEATURES Slott) (Jugai redile) spettov tugal polenA

- Accuracy Guaranteed to ±1 Count Over Entire ±20,000 Counts (2.0000 Volts Full Scale)
- Guaranteed Zero Reading for 0 Volts Input
- 1pA Typical Input Current way as asset or hard of short
- True Differential Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Over-Range and Under-Range Signals Available for Auto-Range Capability AND JACISTORIE
- All Outputs TTL Compatible
- . Blinking Outputs Gives Visual Indication of Over-
- Six Auxiliary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other
- Multiplexed BCD Outputs



# ICL7135



## **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage V <sup>+</sup>	+6V
V	
Analog Input Voltage (either input) (Note 1) V +	to V-
Reference Input Voltage (either input)V+	to V-
Clock Input Gnd to	0 V+

Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100 µA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS** (Note 1)

 $(V^+ = +5V, V^- = -5V, T_A = 25^{\circ}C, Clock Frequency Set for 3 Reading/Sec)$ 

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
ANALOG (N	ote 1) (Note 2)	ania lesevez to	notibbs er	ff verbess	no ream se Its is incre	reflue. Cit
	Zero Input Reading	V <sub>IN</sub> = 0.0V Full Scale = 2.000V	-0.0000	±0.0000	+0.0000	Digital Reading
	Ratiometric Reading (2)	V <sub>IN</sub> ≡ V <sub>REF</sub> Full Scale = 2.000V	+0.9998	+ 0.9999	+1.0000	Digital Reading
	Linearity over ± Full Scale (error of reading from best straight line)	$-2V \le V_{IN} \le +2V$	MO	0.5	BMI 10M	Digital Count Error
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \le V_{\text{IN}} \le +2V$		+ 0.01	LOSS NOR	LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)	-V <sub>IN</sub> ≡ +V <sub>IN</sub> ≈ 2V	Evaluation active, passi	0.5	7 <b>1</b> (\V3)	Digital Count Error
en	Noise (P-P value not exceeded 95% of time)	V <sub>IN</sub> = 0V Full scale = 2.000V	7000	15		μV
lilk	Leakage Current at Input	V <sub>IN</sub> = 0V	100.10 A	1	10	рА
BONGANTS SEC.	Zero Reading Drift	$V_{IN} = 0V$ $0^{\circ} \le T_{A} \le 70^{\circ}C$	1896) [5]	0.5	2	μV/°C
TC	Scale Factor Temperature Coefficient (3)	V <sub>IN</sub> = +2V 0 ≤ T <sub>A</sub> ≤ 70°C (ext. ref. 0 ppm/°C)	4.4	2 0	5	ppm/°C

6

## **ELECTRICAL CHARACTERISTICS (CONT.)**

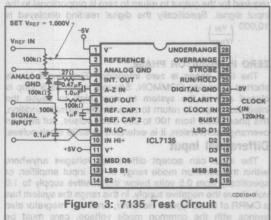
SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL	parameter in the parame	Andrew Comment				
INPUTS		\$ tieff	1966	9/1		
VINH	THE OTHER CONTRACT	Const - Buryting Van	2.8	2.2	0.8	٧
INL	Clock in, Run/Hold, See Figure 4	$V_{IN} = 0$ $V_{IN} = +5V$		0.02	0.1	mA μA
OUTPUTS	POTABLE					
Vol Voh Voh	All Outputs B <sub>1</sub> , B <sub>2</sub> , B <sub>4</sub> , B <sub>8</sub> D <sub>1</sub> , D <sub>2</sub> , D <sub>3</sub> , D <sub>4</sub> , D <sub>5</sub> BUSY, STROBE, OVER-RANGE, UNDER-RANGE POLARITY	$I_{OL} = 1.6 \text{mA}$ $I_{OH} = -1 \text{mA}$ $I_{OH} = -10 \mu \text{A}$	2.4	0.25 4.2 4.99	0.40	V V
SUPPLY	A.1074	SHE SHE SHE SHE SHE	W 1807	sall	TUIT	
٧+	+5V Supply Range	F-0	+4	+5	+6	V
٧-	-5V Supply Range	ATT A PARTY OF THE	HO -3	25	-8	V
1+	+5V Supply Current	$f_C = 0$		1.1	3.0	mA
17	-5V Supply Current	$f_C = 0$	EX (1)30 -	0.8	3.0	C1 1 100
C <sub>PD</sub>	Power Dissipation Capacitance	vs. Clock Freq		40	ON I	pF
CLOCK			TO HER DIE TO THE TO		Marchine and and and	
TENNESSEE H	Clock Freq. (Note 4)	e enimos solona is on	DC DC	2000	1200	kHz

NOTES: 1. Tested in 4-1/2 digit (20,000 count) circuit shown in Figure 3, clock frequency 120kHz.

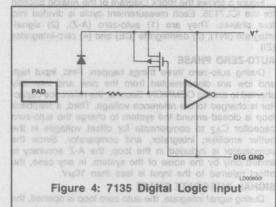
2. Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

3. The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

4. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

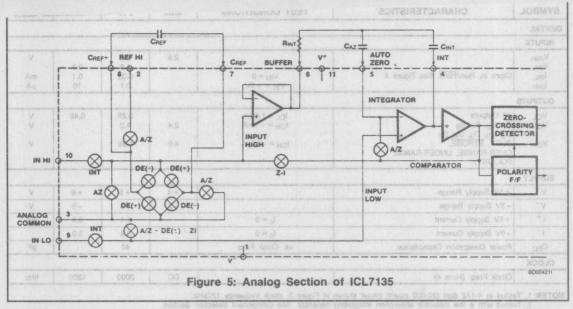


evercased to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative most signed drives the integrator positive when most of its swing has been used up by the noetive common mode voltage. For these offices applications the integrator swing can be reduced to less than the recommended 4V full scale swing within some toss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.



an appropriate the differential voltage between IN FII and IN LO or a fixed time. This differential voltage can be writin a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply. If LO can be field to analog COMMON to establish the connect common-mode voltage. At the end of this phase, the polarity of the infegrated signal is introduction to the polarity of the infegrated signal as introduction to the polarity of the selection.

The Third phase is de-integrate, or reference integrate, lopus LOW is internelly connected to analog COMMON and arout high is connected across the previously charged.



# DETAILED DESCRIPTION on Great the state of the profit of t

Figure 5 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal-integrate (INT), (3) deintegrate (DE) and (4) zero-integrator (ZI).

#### **AUTO-ZERO PHASE**

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor  $C_{AZ}$  to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10\mu V$ .

## SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

#### **DE-INTEGRATE PHASE**

The Third phase is de-integrate, or reference integrate. Input LOW is internally connected to analog COMMON and input high is connected across the previously charged

reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is  $10,000 \ / \ V_{IN} \ 1$ .

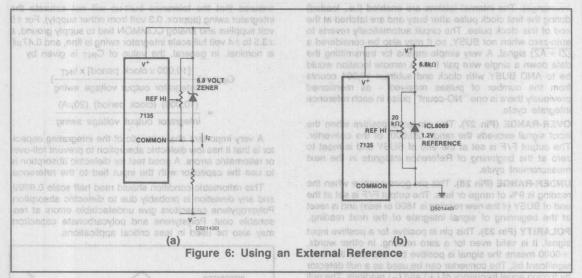
## ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

## Differential Input

VREE

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive commonmode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.



## **Analog Common**

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

#### Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 6.

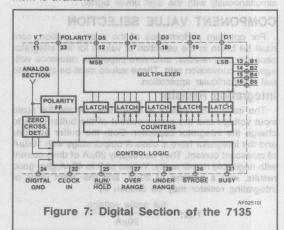
# DETAILED DESCRIPTION Digital Section

Figure 7 shows the Digital Section of the 7135. The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

Run/HOLD (Pin 25). When high (or open) the A/D will freerun with equally spaced measurement cycles every 40,002 clock pulses. It taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/H is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/HOLD is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

STROBE (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches,

UARTs or microprocessors. There are 5 negative going STROBE pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first STROBE pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the STROBE goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last STROBE pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional STROBE pulses will be sent until a new measurement is available.



BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an

6

overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a  $(\overline{Z}I + A\overline{Z})$  signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

**OVER-RANGE** (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F/F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

**UNDER-RANGE** (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F/F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

**POLARITY (Pin 23).** This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (-) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is  $D_5$  (MSD),  $D_4$ ,  $D_3$ ,  $D_2$  and  $D_1$  (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when  $D_5$  will start the scan again. This can give a blinking display as a visual indication of overrange.

**BCD** (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B<sub>8</sub>, B<sub>4</sub>, B<sub>2</sub> and B<sub>1</sub> are positive logic signals that go on simultaneously with the digit driver signal.

#### COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

#### Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with  $100\mu A$  of quiescent current. They can supply  $20\mu A$  of drive current with negligible non-linearity. Values of 5 to  $40\mu A$  give good results, with a nominal of  $20\mu A$ , and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu\text{A}}$$

## Integrating Capacitor

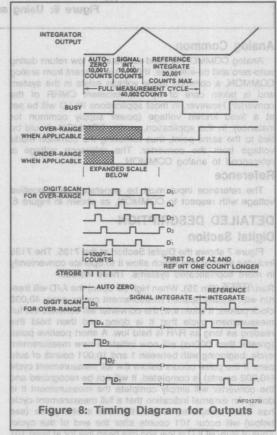
The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance built-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For  $\pm 5$  volt supplies and analog COMMON tied to supply ground, a  $\pm 3.5$  to  $\pm 4$  volt full scale integrator swing is fine, and  $0.47 \mu F$  is nominal. In general, the value of  $C_{\rm INT}$  is given by

$$C_{INT} = (\frac{[10,000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}}$$

$$= \frac{(10,000) \text{ (clock period) } (20\mu\text{A})}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.



## **Auto-Zero and Reference Capacitor**

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough

**WINTERSIL** 

such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and autozero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

## Reference Voltage Say GMA SanT abinoid vd abism

The analog input required to generate a full-scale output is V<sub>IN</sub> = 2 V<sub>REF</sub>, and a second of the s

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

## Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified, adjustment may be needed. The diode can be any silicon diode, such as 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

#### Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 $\mu$ s delay, and at a clock frequency of 160kHz (6 $\mu$ s period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 $\mu$ V input, 1 to 2 with 150 $\mu$ V, 2 to 3 at 250 $\mu$ V, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash ''1'' on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166 2/3kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

## Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

### **EVALUATING THE ERROR SOURCES**

Errors from the "ideal" cycle are caused by:

- 1. Capacitor droop due to leakage.
- Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
- 3. Non-linearity of buffer and integrator.
- High-frequency limitations of buffer, integrator and comparator.
- 5. Integrating capacitor non-linearity (dielectric absorption.)
- 6. Charge lost by CREF in charging Cstrav.
- 7. Charge lost by CAZ and CINT to charge Cstray.

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

## NOISE

The peak-to-peak noise around zero is approximately  $15\mu V$  (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately  $30\mu V$ . Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

#### ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

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The 7135 is designed to work from  $\pm 5V$  supplies. However, in selected applications no negative supply is required. The conditions to use a single  $\pm 5V$  supply are:

- 1.0 The input signal can be referenced to the center of the common mode range of the converter.
- 2. The signal is less than ±1.5 volts.

See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

#### TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 9 shows the complete circuit for a  $4-\frac{1}{2}$  digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to  $50\mu$ A. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The  $\frac{1}{2}$  digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

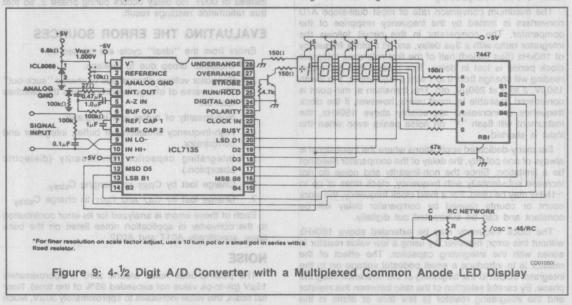
Figure 10 is similar except the output drives a multiplexed common cathode LED Display with the 7-Common Emitter

lower component count possible. Both versions of the complete circuit will give a blinking display as a visual indication of overrange. A clock oscillator circuit using the ICM7555 CMOS timer is shown.

A suitable circuit for driving a plasma-type display is shown in Figure 11. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'Bl' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5k $\Omega$  & 3k $\Omega$  resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

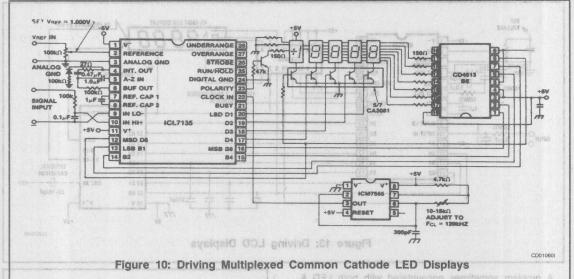
The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 13. A standard CMOS 4030 QUAD XOR gate is used for displaying the ½ digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-½ digit (±2,000V) A/D.

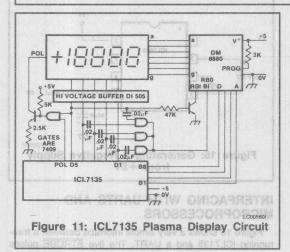
Figure 12 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the STROBE signal and 'Overrange' is indicated by blanking the 4 full digits.

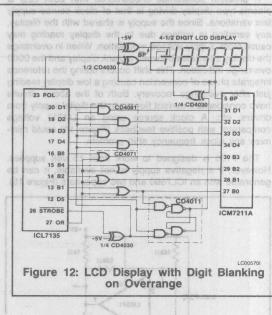


6-128

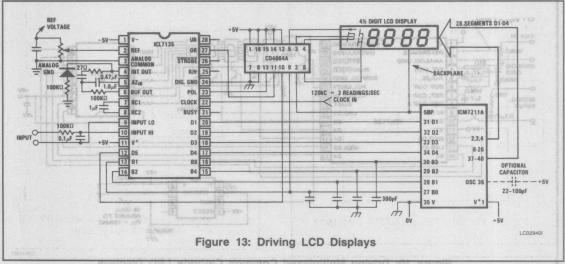
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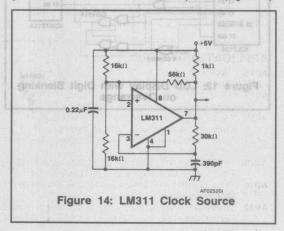


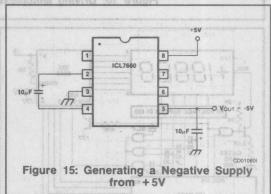
using it to drive the Even Parity Enable Pin (EZE) if EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 17. Here the UART can instruct the AZD to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again STADGE starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the Dg word since in this instance it is known that Rd = Rd = Rd = 0.



A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using an LM311 voltage comparator with positive feedback (Figure 14) could minimize any clock frequency shift problem.

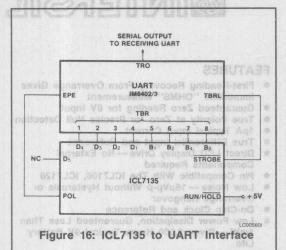
The 7135 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated with an ICL7660 and two capacitors (Figure 15).

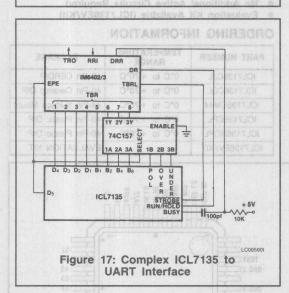




# INTERFACING WITH UARTS AND MICROPROCESSORS

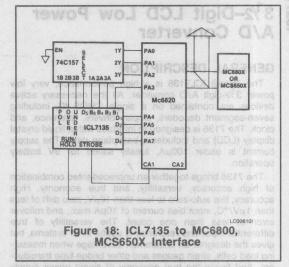
Figure 16 shows a very simple interface between a freerunning ICL7135 and a UART. The five STROBE pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 17. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again STROBE starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D<sub>5</sub> word since in this instance it is known that  $B_2 = B_4 = B_8 = 0.$ 

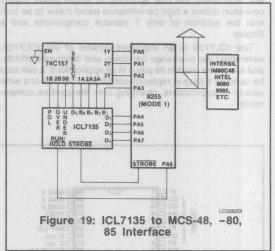




For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 18 and 19. The 8080/8048 and the MC6800 groups with 8 bit buses need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.





## APPLICATION NOTES

- A016 "Selecting A/D Converters," by David Fullagar
- A017 "The Integrating A/D Converters," by Lee Evans
- A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A019 "4-1/2 Digit Plan Meter Demonstrator/
- Instrumentation Boards," by Michael Dufort

  A023 "Low Cost Digital Panel Meter Designs," by David
  Fullager and Michael Dufort
- A028 "Building an Auto-Ranging DMM Using the 8052A/ 7103A A/D Converter Pair," by Larry Goff
- A030 "The ICL7104 A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
- R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

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## A/D Converter

## GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power  $3^{1/2}$ -digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under  $100\mu\text{A}$ , ideally suited for 9V battery operation.

The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than  $10\mu V$ , zero drift of less than  $1\mu V/^{\circ} C$ , input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

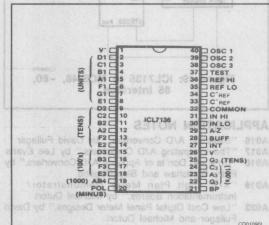
The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

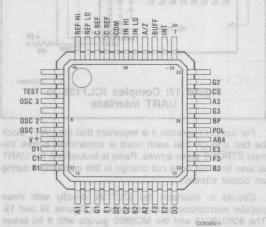
#### **FEATURES**

- First-Reading Recovery From Overrange Gives Immediate "OHMS" Measurement
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LCD Display Drive No External Components Required
- Pin Compatible With The ICL7106, ICL7126
- Low Noise 15μVp-p Without Hysteresis or Overrange Hangover
- On-Chip Clock and Reference
- Low Power Dissipation, Guaranteed Less Than 1mW — Gives 8,000 Hours Typical 9V Battery Life
- No Additional Active Circuits Required
- Evaluation Kit Available (ICL7136EV/Kit)

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE		
ICL7136CJL	0°C to +70°C	40-Pin CERDIP		
ICL7136CDL	0°C to +70°C	40-Pin Ceramic DIP		
ICL7136CM44	0°C to +70°C	44-Pin Surface Mount		
ICL7136CPL	0°C to +70°C	40-Pin Plastic DIP		
ICL7136RCPL	0°C to +70°C	40-Pin Plastic DIP		
ICL7136EV/KIT	THE RE ME B AS AS AS AS	EVALUATION KIT		





need to have polarity over-range and unanotations in the UART organization of the ICLX104 — A Binary Output AXD Converted and the Day Output AXD Converted and the UART organization of the UART organization of the UART or

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### **ABSOLUTE MAXIMUM RATINGS**

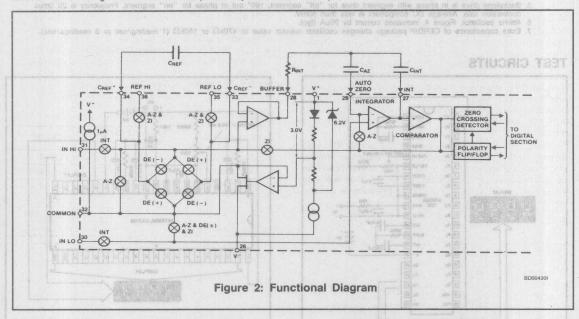
Supply Voltage (V + to V -)	. 15V
Analog Input Voltage (either input)(Note 1) V + 1	to V
Reference Input Voltage (either input)V+	to V-
Clock InputTEST to	o V+

Power Dissipation (Note 2)	Market Commercial Control of the Commercial Control
Ceramic Package	
Plastic Package	800mW
Operating Temperature	
Storage Temperature	65°C to +150°C
Lead Temperature (Soldering, 10	

ELECTRICAL CHARACTERISTICS (CONT.)

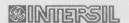
Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to  $\pm 100 \mu A$ . Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## **ELECTRICAL CHARACTERISTICS** (Notes 3, 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V <sub>IN</sub> = 0.0V Full-Scale = 200.0mV	-000.0	±000.0	+ 000.0	Digital Reading
Ratiometric Reading	V <sub>IN</sub> = V <sub>REF</sub> , V <sub>REF</sub> = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN}$ = + $V_{IN}$ $\simeq$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	-1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V <sub>CM</sub> = ±1V, V <sub>IN</sub> = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V <sub>IN</sub> = 0V, Fuil Scale = 200.0mV		15		μV
Leakage Current @ Input	V <sub>IN</sub> = 0V		1	10	pA
Zero Reading Drift	V <sub>IN</sub> = 0V, 0°C < T <sub>A</sub> < +70°C		0.2	. 1	μV/°C
Scale Factor Temperature Coefficient	V <sub>IN</sub> = 199.0mV, 0°C < T <sub>A</sub> < +70°C (Ext. Ref. Oppm/°C)		-1	5	ppm/°C
Supply Current (Does not include COMMON current)	V <sub>IN</sub> = 0V (Note 6)		70	100	μΑ



## **ELECTRICAL CHARACTERISTICS (CONT.)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	NoV Jugar polanA
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply	II	150	a) offeron	ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	$V^+$ to $V^- = 9V$	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V <sup>+</sup> <sub>1</sub> to V <sup>-</sup> <sub>2</sub> = 9V at the rue food and behind	Hacknov	aqque <sup>5</sup> ont b	may 6 xcee	Note 1: In Vit voltages
Power Dissipation Capacitance	vs Clock Frequency		40		pF

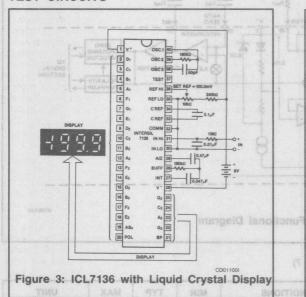
NOTES: 3. Unless otherwise noted, specifications apply at TA = 25°C, fclock = 16kHz and are tested in the circuit of Figure 3.

4. Refer to "Differential Input" discussion.

5. Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV

6. 48kHz oscillator, Figure 4, increases current by  $20\mu$ A (typ). 7. Extra capacitance of CERDIP package changes oscillator resistor value to  $470k\Omega$  or  $150k\Omega$  (1 reading/sec or 3 readings/sec).

#### **TEST CIRCUITS**



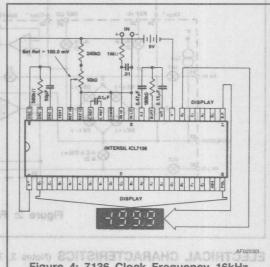
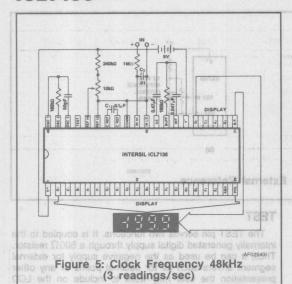


Figure 4: 7136 Clock Frequency 16kHz (1 reading/sec)

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## DETAILED DESCRIPTION bloods be Amt a ment (Analog Section) qual" a si notorut broose sit

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

#### AUTO-ZERO PHASE I benistriam II votasio GOU ont

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor,  $C_{AZ}$ , to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10\mu V$ .

#### SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

#### DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that

the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V<sub>IN</sub>/V<sub>REF</sub>).

#### ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

## **Differential Input**

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive commonmode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

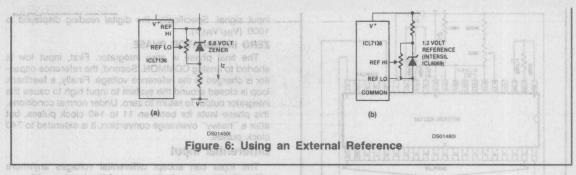
## Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

### **Analog Common**

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ( > 7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ( $\simeq 35\Omega$ ), and a temperature coefficient typically less than 80ppm/°C.

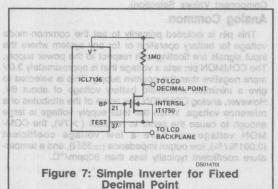
Figure 7: Simple Inverter for Fixed Decimal Point



The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate ( < 7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 3mA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only  $1\mu\text{A}$  of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

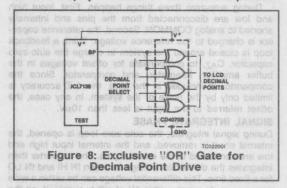


#### TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a  $500\Omega$  resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

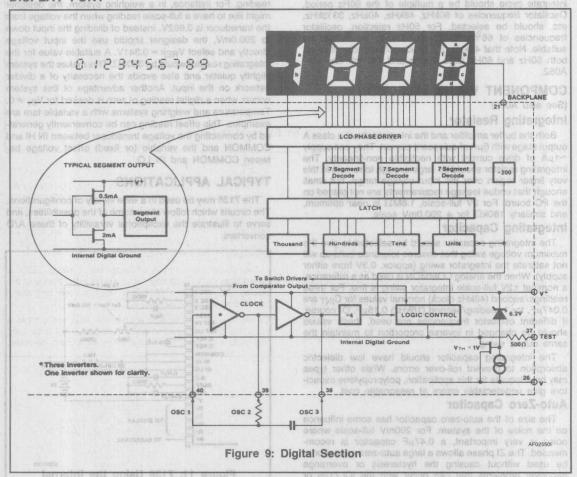
The second function is a "lamp test." When TEST is pulled high (to V +) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10mA under these conditions.

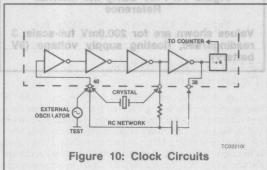
Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.



# DETAILED DESCRIPTION Business before red to (Digital Section)

Figure 9 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower, This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for





### **System Timing**

Figure 10 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

- 1. An external oscillator connected to pin 40.
  - 2. A crystal between pins 39 and 40.
- 3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts\*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-

integrate and zero integrator. This makes a complete

\*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33 /3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66<sup>2</sup>/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

## COMPONENT VALUE SELECTION

(See also A052)

## **Integrating Resistor**

Both the buffer amplifier and the integrator have a class A output stage with  $6\mu A$  of quiescent current. They can supply  ${\sim}1\mu A$  of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale,  $1.8M\Omega$  is near optimum, and similarly  $180k\Omega$  for a 200.0mV scale.

## **Integrating Capacitor**

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal  $\pm 2V$  full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for  $C_{\rm INT}$  are 0.047  $\mu F$ , for 1 reading/second (16kHz) 0.15  $\mu F$ . Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

#### **Auto-Zero Capacitor**

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a  $0.47\mu F$  capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

## Reference Capacitor

A  $0.1\mu F$  capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally,  $1.0\mu F$  will hold the roll-over error to 0.5 count in this instance.

## Oscillator Components at the anatomic observed and

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation f $\sim$ 0.45/RC. For 48kHz clock (3 readings/second), R = 180k $\Omega$ , for 16kHz, R = 560k $\Omega$ .

#### Reference Voltage

The analog input required to generate full-scale output (2000 counts) is  $V_{\rm IN} = 2V_{\rm REF}$ . Thus, for the 200.0mV and 2.000V scale,  $V_{\rm REF}$  should equal 100.0mV and 1.000V,

respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V<sub>REF</sub> = 0.341V. A suitable value for the integrating resistor would be  $330k\Omega$ . This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for  $V_{IN} \neq 0$ . Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

## TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

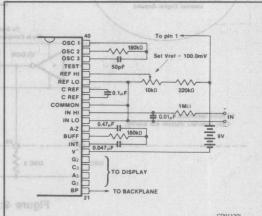


Figure 11: 7136 Using the Internal Reference

Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

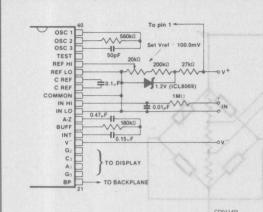


Figure 12: 7136 with an External Band-Gap Reference (1.2V Type)

IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

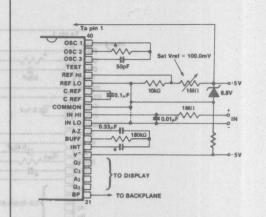


Figure 14: 7136 with Zener Diode Reference

Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.

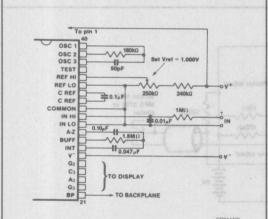


Figure 13: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec

For 1 reading/sec, change C<sub>INT</sub>, R<sub>OSC</sub> to values of Figure 12.

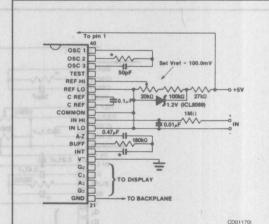


Figure 15: 7136 Operated from Single +5V Supply

An external reference must be used in this application, since the voltage between V<sup>+</sup> and V<sup>-</sup> is insufficient for correct operation of the internal reference.

<sup>\*</sup>Values depend on clock frequency. See Figures 11, 12, 13.

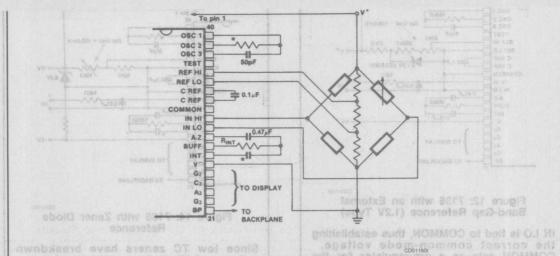


Figure 16: 7136 Measuring Ratiometric Values of Quad Load Cell

The resistor values within the bridge are determined by the desired sensitivity.

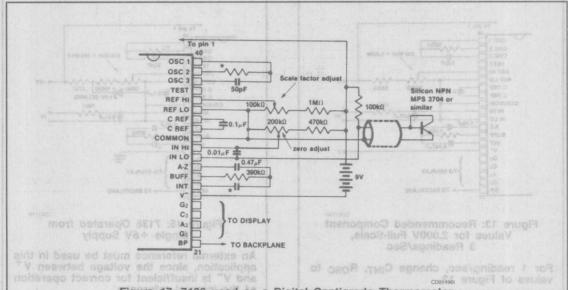
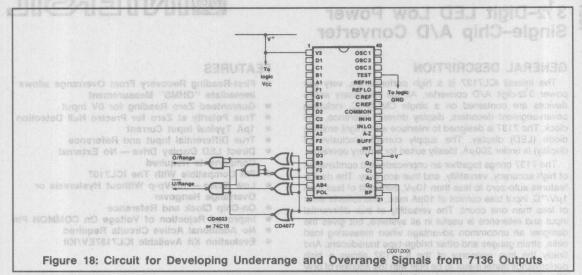
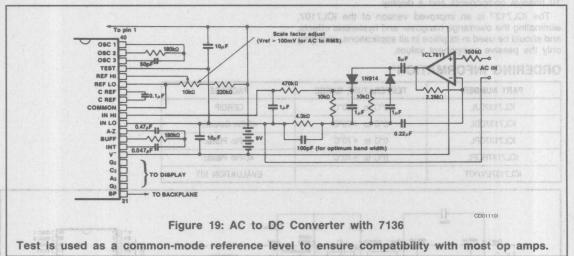


Figure 17: 7136 used as a Digital Centigrade Thermometer

A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL8073/4 and AD590 data sheets for alternative circuits.





## **APPLICATION NOTES**

- A016 "Selecting A/D Converters," by David Fullagar.
- A017 "The Integrating A/D Converter," by Lee Evans.
- A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A019 ''4½-Digit Panel Meter Demonstrator/ Instrumentation Boards," by Michael Dufort.
- A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047 ''Games People Play with Intersil's A/D Converters,'' edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 31/2-Digit A/D Converters," by Dan Watson.

#### 7136 EVALUATION KIT

After purchasing a sample of the 7136, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7136EV/Kit and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

## ICL7137

# 3 /2-Digit LED Low Power Single-Chip A/D Converter

# **WINTERSIL**

## **GENERAL DESCRIPTION**

The Intersil ICL7137 is a high performance, very low power  $3^{1/2}$ -digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200  $\mu$ A, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. The device features auto-zero to less than  $10\mu\text{V}$ , zero drift of less than  $1\mu\text{V}/^{\circ}\text{C}$ , input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

## **FEATURES**

- First-Reading Recovery From Overrange allows Immediate ''OHMS'' Measurement
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LED Display Drive No External Components Required
  - Pin Compatible With The ICL7107
- Low Noise 15μVp-p Without Hysteresis or Overrange Hangover
- On-Chip Clock and Reference
- Improved Rejection of Voltage On COMMON Pin
- No Additional Active Circuits Required
- Evaluation Kit Available ICL7137EV/Kit
   Floure 18: Circuit for Developing Undervange

## **ORDERING INFORMATION\***

PART NUMBER	TEMPERATURE RANGE	PACKAGE	
ICL7137CJL	0°C to +70°C	CERDIP	1.
ICL7137CDL	0°C to +70°C	40-Pin Ceramic	
ICL7137CPL	0°C to +70°C	40-Pin Plastic	V
ICL7137RCPL	0°C to +70°C	40-Pin Plastic	7
ICL7137EV/KIT		EVALUATION KIT	

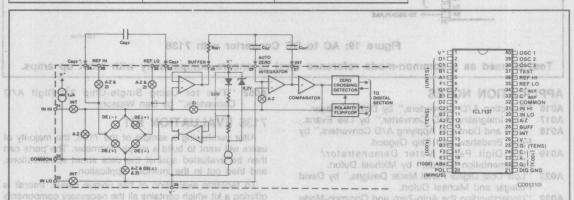


Figure 1: Functional Diagram

Figure 2: Pin Configuration\*
(Outline dwgs PL, JL, DL)

with the ICL7106," by Larry Golf.
A047 "Games People Play with Intersit's A/D

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage V <sup>+</sup>	+6V
Analog Input Voltage (either input)(Note 1)V to Reference Input Voltage (either input)V to	o V-
Clock InputGND to	VT

D D: : :: (Al : - 0)	
Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	65°C to +150°C
Lead Temperature (Soldering, 10sec	)300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 µA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS** (Note 3)

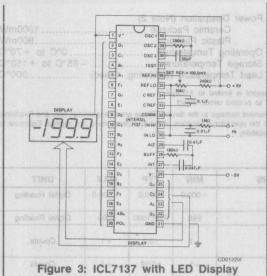
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V <sub>IN</sub> = 0.0V Full-Scale = 200.0mV	- 000.0	±000.0	+ 000.0	Digital Reading
Ratiometric Reading	VIN = VREF, VREF = 100mV	998	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq 200.0$ mV		±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	ysicelo-ba	±0.02	idtz13	Counts
Common-Mode Rejection Ratio (Note 4)	V <sub>CM</sub> = ±1V, V <sub>IN</sub> = 0V Full-Scale = 200.0mV		30		μ\/\
Noise (Pk-Pk value not exceeded 95% of time)	V <sub>IN</sub> = 0V, Full-Scale = 200.0mV		15	er	μV
Leakage Current @ Input	VIN = 0V OM BRIDE		1	10	pA
Zero Reading Drift	V <sub>IN</sub> = 0V, 0°C < T <sub>A</sub> < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V <sub>IN</sub> = 199.0mV, 0°C < T <sub>A</sub> < +70°C (Ext. Ref. Oppm/°C)		1	5	ppm/°C
V *Supply Current (Does not Include LED current)	V <sub>IN</sub> = 0V (Note 5)		70	200	μΑ
V Supply current	Tot begranged to the		40	one S	13
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150	REEMS	ppm/°C
Segment Sinking Current (Except Pins 19 & 20) (Pin 19 only) (Pin 20 only)	V <sup>+</sup> = 5.0V Segment Voltage = 3V	5 10 4	8.0 16 7	ET VSI	mA
Power Dissipation Capacitance	vs. Clock Frequency	THE THE	40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T<sub>A</sub> = 25°C, f<sub>clock</sub> = 16kHz and are tested in the circuit of Figure 4.

4. Refer to "Differential Input" discussion.

5. 48kHz oscillator, Figure 5, increases current by 35µA (typ).

6. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).



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## TEST CIRCUITS

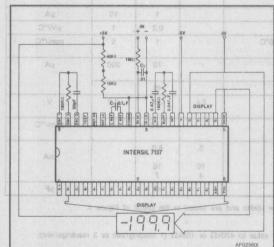
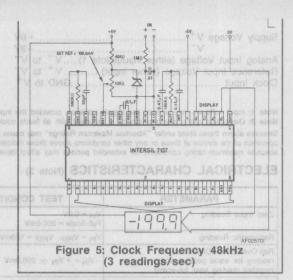


Figure 4: 7137 Clock Frequency 16kHz (1 reading/sec)



## DETAILED DESCRIPTION (Analog Section)

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero-integrator (ZI).

#### **AUTO-ZERO PHASE**

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, CAZ, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10 µV.

#### SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

#### **DE-INTEGRATE PHASE**

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically; the digital reading displayed is 1000(VIN/VREF).

#### ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

## Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive commonmode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

### **Differential Reference**

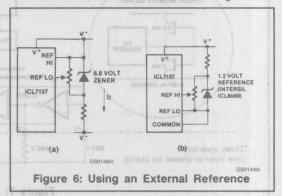
The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

## Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V.

However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COM-MON voltage will have a low voltage coefficient (0.001%/%), low output impedance( $\sim 35\Omega$ ), and a temperature coefficient typically less than 150ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (< 7V). These problems are eliminated if an external reference is used, as shown in Figure 6.



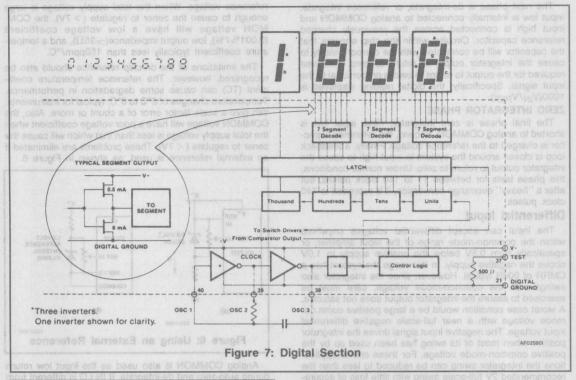
Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

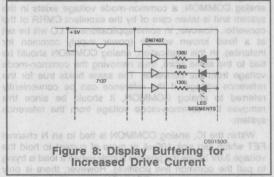
Within the IC, analog COMMON is tied to an N channel FET which can sink 100 µA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

Figure 7 shows the digital section for the 71 TRAIL The TEST pin is coupled to the internal digital supply through a 500Ω resistor, and functions as a 'lamp test.' When TEST is pulled high (to V +) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10mA under these conditions.

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# DETAILED DESCRIPTION (Digital Section)

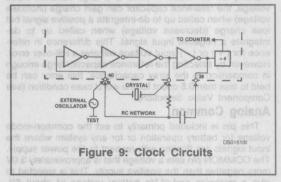
Figure 7 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 8 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

## System Timing grows can Justice actarpoint off

Figure 9 shows the clock oscillator provided in the 7137 Three basic clocking arrangements can be used:

- 1. An external oscillator connected to pin 40.
- 2. A crystal between pins 39 and 40.
  - 3. An RC oscillator using all three pins.



The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts),

ICL7137

zero integrator (11 counts to 140 counts\*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference deintegrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33 /3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66 /3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz.) See also A052.

\*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

## COMPONENT VALUE SELECTION

(See Application Note A052)

## Integrating Resistorous not esuisV

Both the buffer amplifier and the integrator have a class A output stage with  $6\mu\text{A}$  of quiescent current. They can supply  $\sim\!1\,\mu\text{A}$  of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale,  $1.8\text{M}\Omega$  is near optimum, and similarly  $180\text{k}\Omega$  for a 200.0mV scale.

## **Integrating Capacitor**

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal  $\pm 2V$  full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for  $C_{\rm INT}$  are 0.047  $\mu F$ , for 1 reading/second (16kHz) 0.15  $\mu F$ . Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

## **Auto-Zero Capacitor**

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a  $0.47\mu F$  capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (See Application Note A032).

#### Reference Capacitor

A  $0.1\mu F$  capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally,  $1.0\mu F$  will hold the roll-over error to 0.5 count in this instance.

## **Oscillator Components**

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation f  $\simeq$  0.45/RC. For 48kHz clock (3 readings/second), R = 180k $\Omega$ , while for 16kHz (1 reading/sec), R = 560k $\Omega$ .

## Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: VIN = 2VREF. Thus, for the 200.0mV and 2,000V scale, VREF should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V<sub>RFF</sub> = 0.341V. A suitable value for the integrating resistor would be 330k $\Omega$ . This makes the system slightly guieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for  $V_{IN} \neq 0$ . Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

## TYPICAL APPLICATIONS

The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

Figure 11: 7137 with an External Sand-Gap Reference (1.2V Type).

IN LO is fied to COMMON, thus establishing

COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/ sec.

<sup>\*</sup>After an overranged conversion of more than 2060 counts, the zero intergrator phase will last 740 counts, and auto-zero will last 260 counts.

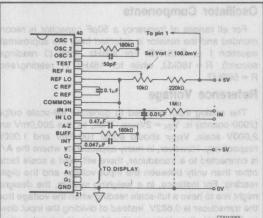


Figure 10: 7137 Using the Internal Reference.

Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

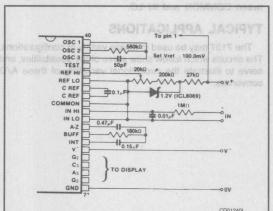


Figure 11: 7137 with an External Band-Gap Reference (1.2V Type).

IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

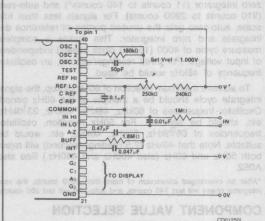


Figure 12: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec.

For 1 reading/sec, change C<sub>INT</sub>, R<sub>OSC</sub> to values of Figure 11.

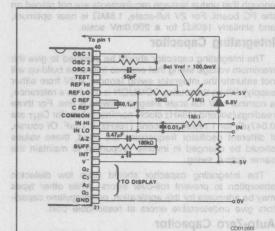


Figure 13: 7137 with Zener Diode Reference.

Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

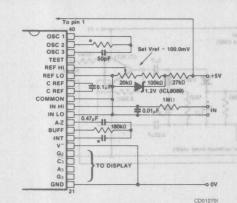


Figure 14: 7137 Operated from Single +5V Supply.

An external reference must be used in this application, since the voltage between V<sup>+</sup> and V<sup>-</sup> is insufficient for correct operation of the internal reference.

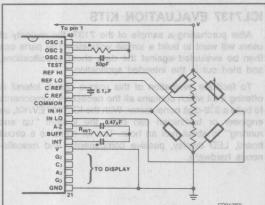


Figure 15: Measuring Ratiometric Values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.

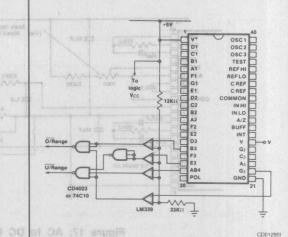
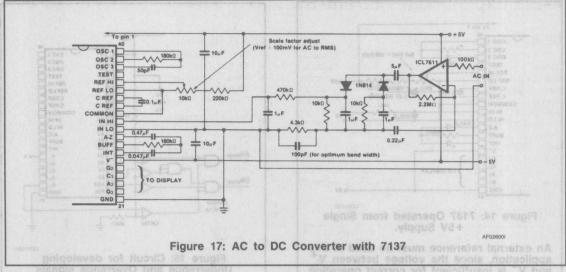


Figure 16: Circuit for developing Underrange and Overrange signals from outputs.

The LM339 is required to ensure logic compatibility with heavy display loading.



## **APPLICATION NOTES**

- A016 "Selecting A/D converters," by David Fullagar.
- A017 "The Integrating A/D Converter," by Lee Evans.
- A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A019 ''4/2-Digit Panel Meter Demonstrator/ Instrumentation Boards," by Michael Dufort.
- A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047 "Games People Play with Intersil's A/D Converters" edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

## **ICL7137 EVALUATION KITS**

After purchasing a sample of the 7137, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a  $3^{1/2}$ -digit panel meter. With the ICL7137EV/Kit, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, LED display, passive components, and miscellaneous hardware.

## ICL8018A/8019A/8020A 4-Bit Expandable Current-Switch



#### GENERAL DESCRIPTION

The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-toanalog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

## ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
ndividual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

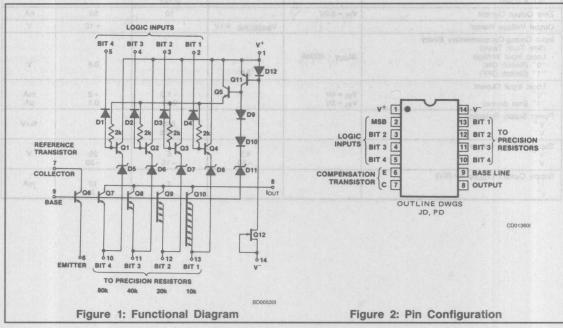
#### **FEATURES**

- TTL Compatible
- 12 Bit Accuracy
- 40ns, Switching Speed
- Wide Power Supply Range
- Low Temperature Coefficient

## **APPLICATIONS:**

- D/A and A/D Converters
- **Digital Threshold Control**
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

\*NOTE: Units ordered in equal quantities will be matched such that the VBE's of the 8019 will be within  $\pm 10\text{mV}$  of the 8018 compensating transistor, and the VBE's of the 8020 will be within  $\pm 50\text{mV}$ . The ICL8018-X matched sets consist of one 8018, one 8019, and one 8020. The 8019-X contains one 8019 and one 8020, while the 8020-X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.



# ICL.8018A/8019A/8020A

## ICL8018A/8019A/8020A

# AOSOB\AOSOB\ SINTERSIL

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Logic Input Voltage	
VBASELINE V	to +5V
Output VoltageVBASELINE	
Storage Temperature -65°C t	0 +150°C

Operating Temperature ICL8018AM
ICL8019/20AM55°C to +125°C
ICL8018/19/20AC0°C to +70°C
Lead Temperature (Soldering, 10sec)300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS** $(4.5V \le V^+ \le 20V, V^- = -15V, T_A = 25^{\circ}C, Voltage @ pin 6 = -5V)$

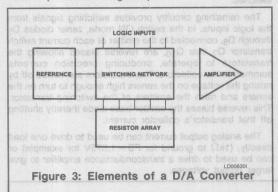
PARAMETER	TEST	MIN MIN	TYP	MAX	UNIT
Absolute Error ICL8018A ICL8019A ICL8020A	V <sub>INHI</sub> = 5.0V V <sub>INLO</sub> = 0.0V	for industrial	metays nottained	±,01 ±0.1 ±1	00 409001
Error Temperature Coefficient ICL8018A ICL8019A ICL8020A	aliaU ,3TOM*	MERCHAL PAMOE PRO DIP	±2 YAA ±2 ±2 ±2	9May ±25	ppm/°C
Settling Time To $\pm$ 1/2 LSB, R <sub>L</sub> = 1k $\Omega$ 8 BIT 12 BIT		STRACPD STRACPD	100 GLVA 200 GLVA	Devices 1 Curon	reutmind Pro. Pro ns
Switching Time To Turn On LSB	1-9108	CHOASS	40	SOGLEN	ns
Output Current (Nominal) BIT 1 (MSB) BIT 2 BIT 3 BIT 4 (LSB)	1-0505 Nv. stas	18ACXPD 19ACXPD 20ACXPD	BJOI 05 CLXMA	36/92 87,88,79 97,88,79 97,89,99	mA
Zero Output Current	V <sub>IN</sub> = 5.0V		10	50	.nA
Output Voltage Range		VBASELINE +1V	entrain otor	+10	V
Input Coding-Complementary Binary (See Truth Table) Logic Input Voltage "0" (Switch ON) "1" (Switch OFF)	Δl <sub>OUT</sub> < 400nA	2.0	20 E0 B9	0.8	٧
Logic Input Current "0" "1" (into device)	V <sub>IN</sub> = 0V V <sub>IN</sub> = 5V	1 150	-1.0 0.01	-2 0.1	mA μA
Power Supply Rejection V + V-	16004	60.37	.005	io Ara	%/V
Supply Voltage Range V+ V-	armen.	4.5 -10	5 -15		V TRANS
Supply Current (V <sub>SUPP</sub> = ±20V)	MERMARY MERMARY	Tracel	7	10	mA

Flaure 2: Pin Configuration

## ICL8018A/8019A/8020A

#### BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 3. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see Figure 4. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.



#### **DEFINITION OF TERMS**

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Table 1) each output corresponding to a particular logic input word.

Table 1: ICL8018/19/20 Truth Table

LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)
0000	1.875
0001	1.750
0010	1.625
0011	1.500
0100	1.375
0 1 0 1	1.250
0110	1.125
0111	1.000
1000	0.825
1001	0.750
1010	0.625
1011	0.500
1100	0.375
1101	0.250
1110	0.125
1111	0.000

Note that **maximum output** of the quad switch is 1 + 1/2 + 1/4 + 1/8 = 1-7/8 = 1.875 mA. If this series of bits were continued as  $1/16 + 1/32 + 1/64 \cdot \dots \cdot 1/2^{(n-1)}$ , the maximum output limit would approach 2.0 mA. This



limiting value is called **full scale output**. The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be 4095/4096 x 10V. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The accuracy of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or absolute error is often expressed as a percentage of the full scale output.

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic**. This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The settling time is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within  $\pm 1/2$  LSB of an N bit converter. Since the 8018A family has been designed with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Table 2.

Table 2: Settling Time vs. Rise Time Resistor Load

±1/2 LSB ERROR % FULL SCALE	NUMBER OF TIME CONSTANTS	NUMBER OF RISE TIMES
.2%	6.2	2.8
.05%	7.6	3.4
.01%	9.2	4.2
	ERROR % FULL SCALE .2% .05%	## CONSTANTS    SCALE   CONSTANTS

Rise Time (10% - 90%) = 2.2 RL Ceff

## ICL8018A/8019A/8020A

## **DETAILED DESCRIPTION**

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125µA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q6, to force the voltage on the common base line, so that the collector current of Q6 is equal to the reference current. The emitter current of Q6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the  $80k\Omega$  resistor in the emitter of Q6. Since this resistor is connected to -15V, this puts the emitter of Q6 at nearly -5V and the common base line at one VBE more positive at -4.35V typically.

Also connected to the common base line are the switched current source transistors  $Q_7$  through  $Q_{10}$ . The emitters of these transistors are also connected through weighted precision resistors to -15V and their collector currents summed at pin 8. Since all these transistors,  $Q_6$  through  $Q_{10}$ , are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage

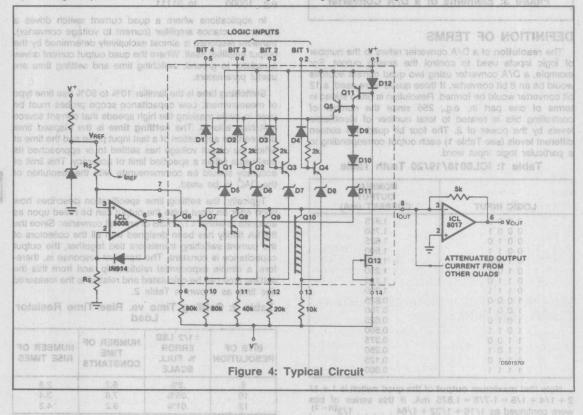
AOSOS/ADEO ® INTERSIL

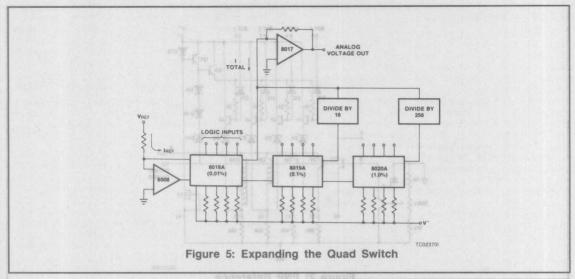
and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of  $\Omega_7$  is equal to that of  $Q_6$ , therefore,  $Q_7$ 's collector current will be  $I_{REF}$  or  $125\mu A$ ,  $Q_8$  has  $40k\Omega$  in the emitter so that its way, the  $20k\Omega$  and  $10k\Omega$  in the emitters of  $Q_9$  and  $Q_{10}$  contribute 0.5 mA and 1 mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes  $D_5$  through  $D_8$ , connected to the emitter of each current switch transistor  $Q_7$  thru  $Q_{10}$ , are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly,  $(1k\Omega)$  to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.





#### **EXPANDING THE QUAD SWITCH**

While there are few requirements for only 4 bit D to A converters, the 8018A is readily expanded to 8 and 12 bits with the addition of other quads and resistor dividers as shown in Figure 5.

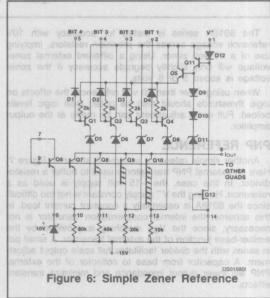
To maintain the progression of binary weighted bit currents, the current output of the first quad drives the input of the transconductance amplifier directly, while a resistor divider network divides the output current of the second quad by 16 and the output current of the third by 256.

e.g., 
$$|T_{Otal}| = 1 \times (1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) + \frac{1}{16}(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) + \frac{1}{256}(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) = 1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{4} + \frac{1}{4} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} + \frac{1}{512} + \frac{1}{1024} + \frac{1}{2048}.$$

Note that each current switch is operating at the same high speed current levels so that standard 10k, 20k, 40k and  $80k\Omega$  resistor networks can be used. Another advantage of this technique is that since the current outputs of the second and third quad are attenuated, so are the errors they contribute. This allows the use of less accurate switches and resistor networks in these positions; hence, the three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted that only the reference transistor on the most significant quad is required to set up the voltage on the common base line joining the three sets of switching transistors (Pin 9).

## GENERATING REFERENCE CURRENTS — ZENER REFERENCE

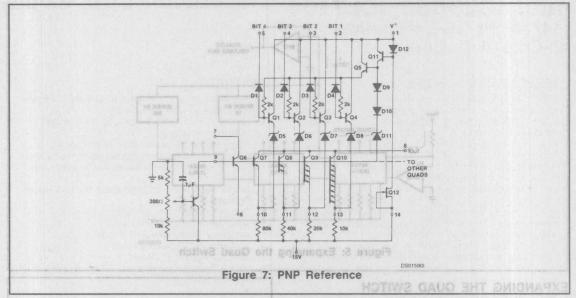
As mentioned above, the 8018A switches currents determined by a constant voltage across the external precision resistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D<sub>11</sub>.



compensation transistor Q6 is connected as a diode in series with the external zener. The VBF of this transistor will approximately match the VBF's of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q6 is operating at a higher current density than the other

The zener current will be typically 1 mA per quad. The

switching transistors, the temperature matching of VBE's is not optimum, but should be adequate for a simple 8 or 10 bit



The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

#### PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the -15 volt supply is used as a reference. Holding the V<sup>-</sup> supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the VBE matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

## **FULL COMPENSATION REFERENCE**

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in Rs by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor  $Q_6$ , provided on the quad switch. The output of the op-amp drives the base of  $Q_6$  keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of  $V_{BE}$  drift, beta drift, resistor drift and changes in  $V^-$ . Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep  $Q_6$  from saturating and prevent latch up if  $V^-$  is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor,  $.001\mu F$  to  $.1\mu F$  from Pin 9 to analog ground is usually sufficient.

## IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of  $V_{BE}$ 's of the current switching transistors. That is, if all the  $V_{BE}$ 's were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.

A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.

# 2-Chip A/D Converter

## GENERAL DESCRIPTION DATION VIGOUS SWITSDOW

The ICL7104, combined with the ICL8052 or ICL8068. forms a member of Intersil's high performance A/D converter family. The ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output UART handshake capability, and other outputs for easy interfacing. The ICL7014-14 is a 14-bit version. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

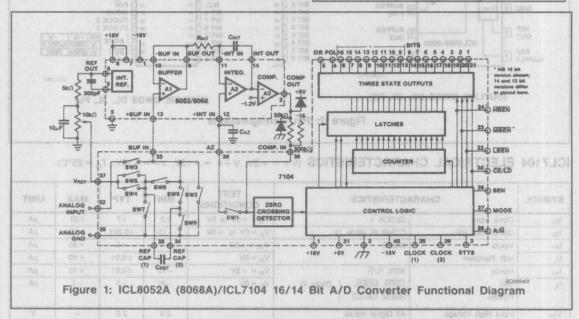
## **FEATURES**

- 16/14 Bit Binary Three-State Latched Outputs
   Plus Polarity and Overrange
- Ideally Suited for Interface to UARTs and
   Microprocessors
- Conversion On Demand or Continuously
- Guaranteed Zero Reading for Zero Volts Input
- True Polarity at Zero Count for Precise Null
   Detection
- Single Reference Voltage for True Ratiometric Operation
- Onboard Clock and Reference
- Auto-Zero: Auto-Polarity
- Accuracy Guaranteed to 1 Count
- All Outputs TTL Compatible
- ±4V Analog Input Range
- Status Signal Available for External Sync, A/Z in Preamp, etc.

#### ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL8052CPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052ACPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068CJD	0°C to +70°C	14-Pin CERDIP
ICL8068ACJD	0°C to +70°C	14-Pin CERDIP

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7104-14CJL	0°C to -70°C	40-Pin CERDIP
ICL7104-14CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-14CDL	0°C to +70°C	40-Pin Ceramic DIF
ICL7104-16CJL	0°C to +70°C	40-Pin CERDIP
ICL7104-16CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-16CDL	0°C to +70°C	40-Pin Ceramic DIP



## ICL8052/ICL7104

## ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1) All Devices500mW	l
Storage Temperature65°C to +150°C	
Operating Temperature 0°C to +70°C	,
Lead Temperature (Soldering, 10sec)300°C	;
ICL8052, 8068	
Supply Voltage±18V	1
Differential Input Voltage (8068)±30V	
(8052)±6\	ŧ.
Input Voltage (2)±15V	
Output Short Circuit Duration, small no notations at	
All Outputs (3)Indefinite	4

True Polarity at Zero Count for Precise Nu

## BINTERSIL

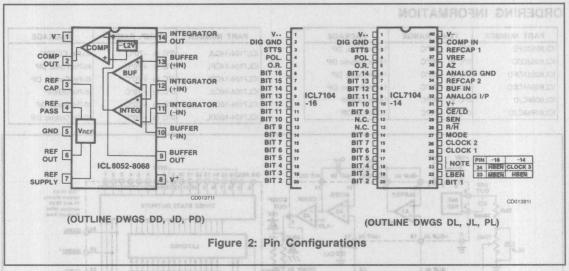
	C	40	-	4	-	-4
1	ε.		7	п	u	а

V+ Supply (GND to V+)	12V
V++ to V	32V
Positive Supply Voltage (GND to V++)	17V
Negative Supply Voltage (GND to V-)	17V
Analog Input Voltage (Pins 32-39) (4) V++ to	V-
Digital Input Voltage	
(Pins 2-30) (5) (GND-0.3V) to (V <sup>+</sup> +0	.3V)
Principal Control of the Control of	

#### Notes

- 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.
- 2: For supply voltages less than  $\pm 15V$ , the absolute maximum input voltage is equal to the supply voltage.
- 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.
- 4: Input voltages may exceed the supply voltages provided the input current is limited to  $\pm 100 \mu A$ .
- 5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## ICL7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V- = -15V, TA = 25°C)

SYMBOL	CHAR	ACTERISTICS	TEST	MIN	ТҮР	MAX	UNIT
liN	Clock Input	CLOCK 1	V <sub>in</sub> = +5V to 0V	±2	±7	±30	μΑ
IIN	Comparator I/P	COMP IN (Note 1)	Vin = 0V to +5V	-10	±0.001	+10	μΑ
l <sub>IH</sub>	Inputs	MODE O O O O O O O O O O O O O O O O O O	V <sub>IN</sub> = +5V	+10-	+5	+30	μΑ
l <sub>L</sub>	with Pulldown	o ser- LEC an ser-	V <sub>in</sub> = 0V	-10	±0.01	+10	μΑ
IIH	Inputs	SEN, R/H	$V_{in} = +5V$	-10	±0.01	+10	μΑ
ht a	with Pullups	HBEN, CE/LD (Note 2)	V <sub>in</sub> = 0V	3) -30	8J5 <sup>5</sup> :r	swall	μΑ
VIH	Input High Voltage	All Digital Inputs		2.5	2.0	-	V

**WINTERSIL** 

## ICL8052/ICL7104

## ICL7104 ELECTRICAL CHARACTERISTICS (CONT.) TRIFFTOARAND JACKSTORIES 8808.101

SYMBOL			CHAR	ACTERISTICS	TEST	MIN	ТҮР	MAX	UNIT
VIL	Input Lo	w Voltage	14110	All Digital Inputs		-	1.5	1.0	V
VOL	Digital		1	LBEN	I <sub>OL</sub> = 1.6mA	-	0.27	.4	V
Vон	Outputs	On the second second		MBEN (16-only) (Note 3)	$I_{OH} = -10\mu A$		4.5		V
Vон	Three-S On	tated	erwise	HBEN CE/LD BIT n, POL, OR	$I_{OH} = -240 \mu A$	2.4	3.5	0313	\$208.10
lor ning i		Outputs tated Off	r Z	BIT n, POL, OR	0 ≤ V <sub>out</sub> ≤ V +	2017EIRE	±.001	+10	IOS MA
VOL	Non-Thr	ee State	PHN	STTS	I <sub>OL</sub> = 3.2mA		0.3	.4	V
Voн	Digital			TIONAL AMPLIPIER	$I_{OH} = -400\mu A$	2.4	3.3	and the second	V
VOL	Output			CLOCK 2	I <sub>OL</sub> = 320μA		0.5	MO Jugal	V 80
VOH	01	2		The State of the second state	$I_{OH} = -320 \mu A$	atovi) (lugni	4.5	Hoput Cur	V 18
VOL				CLOCK 3 (-14 ONLY)	I <sub>OL</sub> = 1.6mA	outsh ricis	0.27	.4	V
VOH		110		Off CV	$I_{OH} = -320 \mu A$	2.4	3.5	Non-Line	٧
RDS(on)			000,03	Switch 1	CNON - OF	-	25k		Ω
RDS(on)				Switches 2,3			4k	20k	Ω
RDS(on)	Switch			Switches 4,5,6,7,8,9		_	2k	10k	Ω
ID(off)	001	00	-	Switch Leakage		Annual Contracts	15	10	pA
*	Clock	ha in the second	lary or my knee	Clock Freq. (Note 4)	A CEACHARA	DC	200	400	kHz
1+	Supply	Currents		+5V Supply Current All outputs high impedance	Freq. = 200kHz	Clash	200	600	μΑ
1++				+ 15V Supply Current	Freq. = 200kHz	Dullag of	.3	1.0	mA
1-		9.51	0.5-	-15V Supply Current	Freq. = 200kHz	рамка ерг	25	200	μΑ
V+	Supply		delines when	Logic Supply	Note 5	4.0	COLUMN TOWNS CO.	+11.0	V
V ++	Range			Positive Supply	The state of the state of	+10.0	egallo	+16.0	V
Asumgo				Negative Supply		-16.0	sphateles	-10.0	VO

NOTES: 1. This spec applies when not in Auto-Zero phase.

2. Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.

3. Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.

4. Clock circuit shown in Figs. 15 and 16.

5. V + must not be more positive than V ++

## ICL8068 ELECTRICAL CHARACTERISTICS (VSUPPLY = ±15V unless otherwise specified)

Value	CHARACTERISTICS	TEST	31 -83178068 TOAR				8068A	BLEC	HETRY
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	TYP MAX		TYP	MAX	TINU Nock Fre
		EACH OPERAT	IONAL AN	PLIFIER				A	continuos de la continuo del continuo del continuo de la continuo
Vos	Input Offset Voltage 3808	V <sub>CM</sub> = 0V		20	65		20	65	mV
IIN TIBYU	Input Current (either input) (Note 1)	V <sub>CM</sub> = 0V	1 84	175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V <sub>CM</sub> = ±10V	70	90	in the second	70	90		dB
ternioobs ge6s	Non-Linear Component of Common- Mode Rejection Ratio (Note 2)	V <sub>CM</sub> = ±2V	0-	110	oll Scale		110	Reading	mg dB nes
Av	Large Signal Voltage Gain	$R_L = 50k\Omega$	20,000	- Manny	Jaky - m	20,000	()	Reading (	V/V
SR	Slew Rate			6		7	6	9 h 32 + 50	V/µs
GBW	Unity Gain Bandwidth	A CIV		2	THE STAB		on2 mga	ute heed n	MHz
Isc	Output Short-Circuit Current			5	10	neswre	por5netti	) v/1000	mA d
		COMPARAT	OR AMPL	IFIER	TOP S VA	bna am	papent cour	os to quie	BIIRD TETOW
AVOL	Small-signal Voltage Gain	$R_L = 30k\Omega$		4000		and made	and the same		V/V
+V0	Positive Output Voltage Swing	0.0	+12	+13	V++mV-	+12	m+13 vi	agen & ev	ligae Vuups
-Vo	Negative Output Voltage Swing		-2.0	-2.6	-	-2.0	-2.6		V
THE REAL PROPERTY.	V4 2	VOLTAGE	REFEREN	ICE	VO.55 AL	10 8 61	рерверхе	Jan Suusy	M-H) soley
Vo	Output Voltage	001	1.5	1.75	2.0	1.60	1.75	1.90	V
Ro	Output Resistance			5	715	-	5		ohms
TC	Temperature Coefficient	6.0		50	247257		40	nititu gr	ppm/°C

## ICL8052/ICL7104



## ICL8068 ELECTRICAL CHARACTERISTICS (CONT.) TEMPTOARAND JACKATOEJE AUTOJO

773933	XAM			8068			8068A			
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
VSUPPLY	Supply Voltage Range		±10		±16	±10		±16	V	
ISUPPLY	Supply Current Total	Ama 1 5 Jal			14		8	14	mA	

## ICL8052 ELECTRICAL CHARACTERISTICS (VSUPPLY = ±15V unless otherwise specified)

ALL	01+ 100± 01-	TEST		8068	109 o TI		8068A		
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	ELECTION DE LES	EACH OPERATI	IONAL AN	APLIFIER	169.5%			bulnet.	unV
Vos	Input Offset Voltage	V <sub>CM</sub> = 0V		20	75		20	75	mV
IIN	Input Current (either input) (Note 1)	V <sub>CM</sub> = 0V		5	50	Telegraphic	2	10	pA
CMRR	Common-Mode Rejection Ratio	V <sub>CM</sub> = ±10V	70	90	LOCK 3	70	90		dB
	Non-Linear Component of Common- Mode Rejection Ratio (Note 2)	V <sub>CM</sub> = ±2V		110			110		dB
Av	Large Signal Voltage Gain	$R_L = 50k\Omega$	20,000	-	1 100101	20,000			V/V
SR	Slew Rate			6	a gorden		6		V/µs
GBW	Unity Gain Bandwidth			1	S. CHILDREN		1	Control	MHz
Isc	Output Short-Circuit Current			20	100		20	100	mA
		COMPARATO	OR AMPL	IFIER	aprile i narate			AMAID	
AVOL	Small-signal Voltage Gain	$R_L = 30k\Omega$	9000	4000	eluctero (b)		BH SHIPE	MARKE	V/V
+Vo	Positive Output Voltage Swing	Energy at 2000king	+12	+13	au8 Vat s	+12	+13		V
-Vo	Negative Output Voltage Swing	S-brook - positi	-2.0	-2.6	STATE OF THE STATE	-2.0	-2.6		V
	1 4.6   +31.0	VOLTAGE	REFEREN	NCE	igou? Sign		acatio	Supply 1	14
Vo	Output Voltage	HE REPOSED IN	1.5	1.75	2.0	1.60	1.75	1.90	V
Ro	Output Resistance			5	G avelage		5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
VSUPPLY	Supply Voltage Range	a 6017 ed bas a	±10	bom edi.	±16	±10	torit marie	±16	V
ISUPPLY	Supply Current Total	a port are to op-	as (88) 8)	6	12	sins emig to	6	12	mA

NOTES: 1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T<sub>J</sub>. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub>Pd where R<sub>θJA</sub> is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

2. This is the only component that causes error in dual-slope converter.

# SYSTEM ELECTRICAL CHARACTERISTICS: ICL8068/7104 (V ++ = $\pm$ 15V, V<sup>+</sup> = $\pm$ 5V, V<sup>-</sup> = $\pm$ 15V, Clock Frequency = 200kHz)

20 - 88 PAV	TEST CONDITIONS	8068A/7104-14			8068A/7104-16			on! soV	
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
Zero Input Reading	V <sub>in</sub> = 0.0V Full Scale = 4.000V	-0.0000	±0.0000	+0.0000	-0.0000	-0.0000	+0.0000	Hexadecimal Reading	
Ratiometric Reading (1)	V <sub>in</sub> = V <sub>Ref.</sub> Full Scale = 4.000V	1FFF	2000	2001	7FFFds	8000	8001	Hexadecimal Reading	
Linearity over ±Full Scale (error of reading from best straight line)	-4V ≤ V <sub>in</sub> ≤ +4V		0.5	1		0.5	a -1 <sub>a</sub> ,	LSB	
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	-4V ≤ V <sub>in</sub> ≤ +4V	ROTAR	.01	in a second	trion	.01	syote, sug	LSB	
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} = +V_{in} \simeq 4V$		0.5	1	Swing	0.5	Company of the Company	LSB	
Noise (P-P value not exceeded 95% of time)	V <sub>in</sub> = 0V Full scale = 4.000V	IR RUA	2			2		μV	
Leakage Current at Input (2)	V <sub>in</sub> = 0V		100	165		100	165	pA	
Zero Reading Drift	V <sub>in</sub> = 0V 0°C ≤ T <sub>A</sub> ≤ 70°C		0.5	2		0.5	2	μV/°C	

	TEGT COMPLETIONS	8088A//104-14			8008A//104-10			
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Scale Factor Temperature (3) Coefficient	$V_{in} = +4V$ $0 \le T_A \le 50$ °C (ext. ref. 0ppm/°C		2 30	5		2 *	5	ppm/°C

# SYSTEM ELECTRICAL CHARACTERISTICS: ICL8052/7104 (V++ = +15V, $V^+$ = +5V, $V^-$ = -15V, Clock Frequency = 200kHz)

	TEAT COMPLETIONS	8052A/7104-14			805	est stime		
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Zero Input Reading	V <sub>in</sub> = 0.0V Full Scale = 4.000V	-0.0000	±0.0000	+ 0.0000	-0.0000	±0.0000	+ 0.0000	Hexadecimal Reading
Ratiometric Reading (3)	V <sub>in</sub> = V <sub>Ref.</sub> Full Scale = 4.000V	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ±Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.5	1 .		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01	( 0	L loss	.01	vageue i	LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	-V <sub>in</sub> = +V <sub>in</sub> ≈4V		0.5	1/-		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V <sub>in</sub> = 0V Full scale = 4.000V		30	4	(tal	30		μV
Leakage Current at Input (2)	V <sub>in</sub> = 0V		20	30		20	30	pA
Zero Reading Drift	V <sub>in</sub> = 0V 0° ≤ T <sub>A</sub> ≤ 70°C		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient	$V_{in} = +4V$ $0 \le T_A \le 70^{\circ}C$ (ext. ref. 0ppm/°C		2	rolleni 5	Comb leadles	2	5	ppm/°C

NOTES: 1. Tested with low dielectric absorption integrating capacitor.

2. the input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T<sub>J</sub>. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub>Pd where R<sub>θAB</sub> is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

where R<sub>0JA</sub> is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

3. The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.

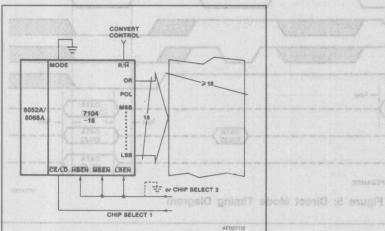
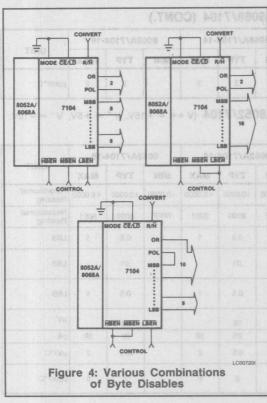
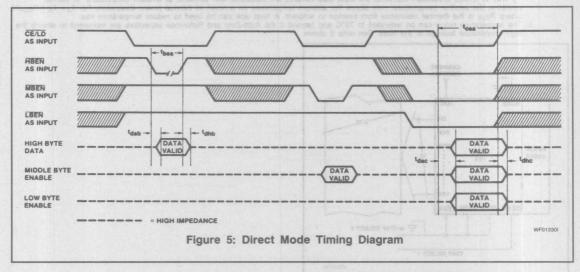


Figure 3: Full 18 Bit Three State Output



AC CHARACTERISTICS (V ++ = +15V, V+ = +5V, V- = -15V)



## ICL8052/ICL7104

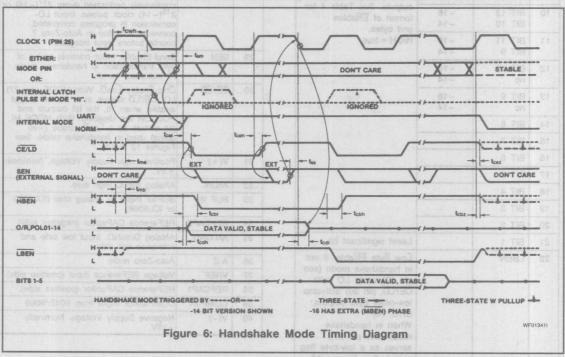
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Table 1: Direct Mode Timing Requirements (Note: Not tested in production)

SYMBOL	DESCRIPTION	-	MIN	TYP	MAX	UNIT
t <sub>bea</sub>	XBEN Min. Pulse Width	NC	DESCRIPTE	300	BOL OPTH	MAS N
tdab Ma shall billi	Data Access Time from XBEN	postic	ve Supply V	300		+101 1
tdhb 118 estavenA	Data Hold Time from XBEN		Vět + vilian	200		ns
tcea (15 mg) Madd	CE/LD Min. Pulse Width		(f) function() u	350		oua s
t <sub>dac</sub>	Data Access Time from CE/LD		markha by	350		
tdhc	Data Hold Time from CE/LD			280		
tcwh	CLOCK 1 High Time	Bearing	TOUGHO GU	1000		0116

Table 2: Handshake Timing Requirements

NAME (1) Mad	DESCRIPTION	MIN	TYP	MAX	UNIT
t <sub>mw</sub>	MODE Pulse (minimum)		20		
t <sub>sm</sub>	MODE pin set-up time	DESCRIPTION OF THE PERSON OF T	-150		POL
tme MOITGIADERG	MODE pin high to low Z CE/LD high delay		200		
t <sub>mb</sub>	MODE pin high to XBEN low Z (high) delay		200		
tcel an an interest in	CLOCK 1 high to CE/LD low delay	Tampe Times	700		ns ns
tceh	CLOCK 1 high to CE/LD high delay	37	600		
tcbl and market Mark	CLOCK 1 high to XBEN low delay		900	- 1	BIT TO
elimitch de pentonnos viis	CLOCK 1 high to XBEN high delay	ne made regis i	700		N TIB
tcdh	CLOCK 1 high to data enabled delay	A SECTION OF THE SECT	1100	- 1	TIS
todi della d	CLOCK 1 low to data disabled delay		1100		TIB
off the test of the same	Send ENable set-up time		-350 m		TIE 8
tcbz	CLOCK 1 high to XBEN disabled delay		2000	200	n na
t <sub>cez</sub>	CLOCK 1 high to CE/LD disabled delay		2000		TIB 6
t <sub>cwh</sub>	CLOCK 1 High Time	1250	1000		TIO



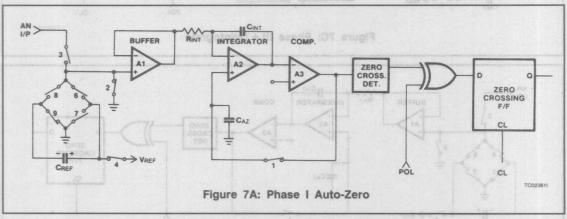
600	п			_	=	-	$\sim$	nn.
B.W.B.W4	$\omega_{l}$	100	57	en:	1	767	W	

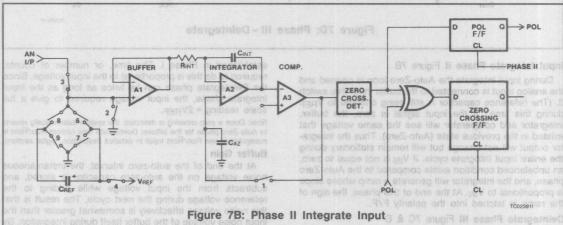
ICI	2052	/ICL7						
1 3/	V(++)		Positive Supply Voltage Nominally +15V					
2	GND		Digital Ground .0V, ground return					
3	STTS	0	STaTuS output. HI during Integrate and Deintegrate until data is latched. LO when analog section is in					
715	A XA	M S	Auto-Zero configuration.					
4	POL	01	POLarity. Three-state output. HI for positive input.					
5	OR		OverRange. Three-state output.					
6	BIT 16	-16						
	BIT 14	-14	(Most significant bit)					
7	BIT 15 BIT 13	-16 -14						
8	BIT 14	-16						
	BIT 12	-14	005					
9	BIT 13	-16	003					
	BIT 11	-14	Data Bits, Three-state outputs. See Table 4 for					
10	BIT 12 BIT 10	-16 -14	format of ENables and bytes.					
11	BIT 11 BIT 9	-16 -14	HIGH = true					
12	BIT 10	-16	arus twee /					
	nc	-14						
13	BIT 9	-16	1					
	nc	-14	Strongs					
14	BIT 8							
15	BIT 7		1					
16	BIT 6		"Transaction of the second of					
17	BIT 5	- 1						
18	BIT 4		S. Percentina Property Construction (Construction)					
19	BIT 3	and the						
20	BIT 2	elfonteriori in gent.						
21	BIT 1		Least significant bit.					
22	LBEN		Low Byte ENable. If not in handshake mode (see pin 27) when LO (with CE/LD, pin 30) activates					
(Second	A TANK MITTAN	TO-RESIDENT	low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 12, 13, 14.					

		1. B-1004-PM	וויייייייייייייייייייייייייייייייייייי					
1/21/	MBEN	2004 - 16 <sup>-1</sup>	Mid Byte ENable. Activates BITS 9-16, see					
		OLYLD Mar	LBEN (pin 22)					
23	HBEN	900×-14	High Byte ENable.					
CE3	Time irom CE	Data Halai	Activates BITS 9-14, POL OR, see LBEN (pin 22)					
rigion	HBEN	-16	High Byte ENable. Activates POL, OR, see					
	10830		LBEN (pin 22).					
24	CLOCK3	14 <sub>A</sub>	RC oscillator pin. Can be used as clock output.					
PIN	SYMBOL	NODE pin	DESCRIPTION					
25	CLOCK1	Clock input.	External clock or ocsillator.					
26	CLOCK2	Clock output	. Crystal or RC oscillator.					
27 no wo be right belds belds belds belds belds belds	MODE down	CE/LD, HBE inputs directl pulsed HI ca handshake m If HI, enable and LBEN as will be entered	rect output mode where N, MBEN and LBEN act as y controlling byte outputs. I uses immediate entry into node (see Figure 14). S CE/LD, HBEN, MBEN, s outputs. Handshake mode and data output as in 13 at conversion					
28	R/H	conversion in	put HI-conversions performed every 2 <sup>17</sup> (-16) of ck pulses. Input LO- n progress completed, I stop in Auto-Zero 7 e input integrate.					
29	SEN A	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates "send".						
30	CE/LD	enable; where POL, OR are pin serves as	LoaD. With MODE (pin 27) serves as a master output in HI, the bit outputs and a disabled. With MODE HI, is a LoaD strobe (-ve in handshake mode. See 113.					
31	V(+)	Positive Logi +5V.	c Supply Voltage. Nominally					
32	AN,IN	ANalog INpu	t. High side.					
33	BUF IN	BUFfer INput or ICL8068)	t to analog chip (ICL8052					
34	REFCAP2	REFerence C	CAPacitor (negative side)					
35	AN.GND.	ANalog Grou reference lov	ND. Input low side and v side.					
36	A-Z	Auto-Zero no	ode.					
37	VREF	Voltage REF	erence input (positive side).					
38	REFCAP1		CAPacitor (positive side).					
39	COMP-IN		INput from 8052/8068					
40	V(-)		oply Voltage. Nominally					

		CE/LD																
	HB	EN		TE	, Tile	MB	EN			1				LB	EN			4
7104-16	POL	O/ R	B16	B15	B14	B13	B12	B11	B10	B9	В8	87	B6	B5	84	вз	B2	B1
			150			HB	EN	1		-				LB	EN			
7104-14			POL	0/ B	B14	B13	B12	B11	B10	В9	B8	В7	В6	B5	B4	ВЗ	B2	B1

Figure 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to Figure 7 below.





## DETAILED DESCRIPTION

## **Analog Section**

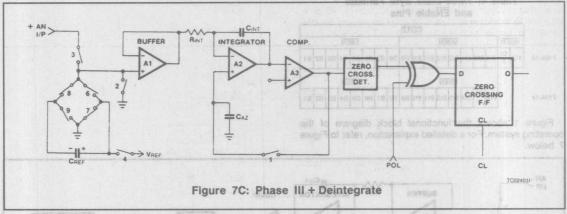
Figure 7 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/Hold pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072

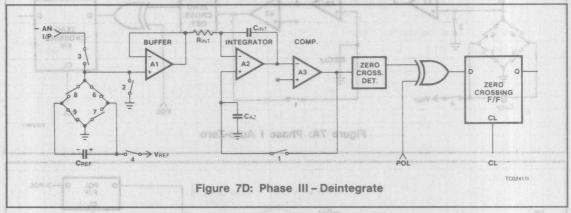
for — 16 and 32,368 for — 14 clock periods per cycle (see Figure 9 conversion timing).

#### Auto-Zero Phase I Figure 7A

During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to VREF.

6





## Input Integrate Phase II Figure 7B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to  $V_{\rm REF}$  during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If  $V_{\rm IN}$  is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to  $V_{\rm IN}$ . At the end of this phase, the sign of the ramp is latched into the polarity F/F.

## Deintegrate Phase III Figure 7C & Diagnal states and it

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is VREF more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause  $+\mbox{VREF}$  to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (-) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point

established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = 2V<sub>RFF</sub>.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/Hold is manipulated, see Run/Hold Input in detailed description, digital section).

#### **Buffer Gain**

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 8. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1 to 2 µV, allowing full 16-bit use

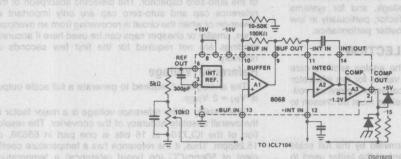
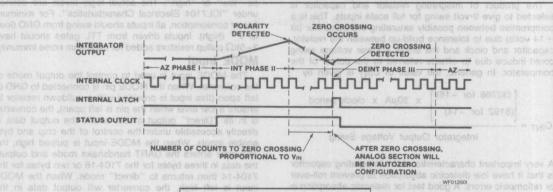


Figure 8: Adding Buffer Gain to ICL8068

Table 5: Typical Component Values (V++ = +15V, V+ = 5V, V- = -15V, Clock Freq = 200kHz)

	ICL8052/8068 WITH	n gaied en	ICL7104-16	04-14	14 off AndS UNIT amon		
	Full scale V <sub>IN</sub>	200	800	4000	100	4000	mV
	Buffer Gain	10	1	1	10	1 = TV	V/V
The state of	RINT	100	43	200	47	180	kΩ
JEGHO	CINT CONDUCTOR STATE OF STATE	.33	.33	00.33	ome 0.1 had	0.10020	al' misquel catola
ALPERT SOURCE	CAZ	1.0	1.0	1.0	1.0	(alo.1.0 and	μF
numia	Cref and a ledahmed TSALL has sing	10	1.0	1.0	10	1.0	FTAIμF
(nyeor	VREF asy aid an OI sound means	100	400	2000	50	2000	mV
t homotor	Resolution	3.1	12	61	6.1	244	O on pv soale



obi	hom exameles COUNTS prefeter and o										
· In	ellille	PHASE I	PHASE II	PHASE III							
441	16	32768	32768	65536							
1 15	14	8192	8192	16384							

Figure 9: Conversion Timing

## ICL8052/ICL7104



## ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

## COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

## **Integrating Resistor**

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 µA give good results with a nominal of 20 µA. The exact value may be chosen by

\*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu\text{A}}$$

## Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at  $\pm$  14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of  $C_{\rm INT}$  is given by

$$C_{INT} = \begin{bmatrix} (32768 \text{ for } -16) \\ (8192 \text{ for } -14) \end{bmatrix} \times 20\mu\text{A} \times \text{clock period}$$

Integrator Output Voltage Swing

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale (100 . . . 000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

## Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

## Reference Voltage

The analog input required to generate a full scale output is V<sub>IN</sub> = 2 V<sub>REF</sub>.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

# DETAILED DESCRIPTION Digital Section

The digital section includes the clock oscillator circuit, a 16 or 14 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 10 (16 bit version shown).

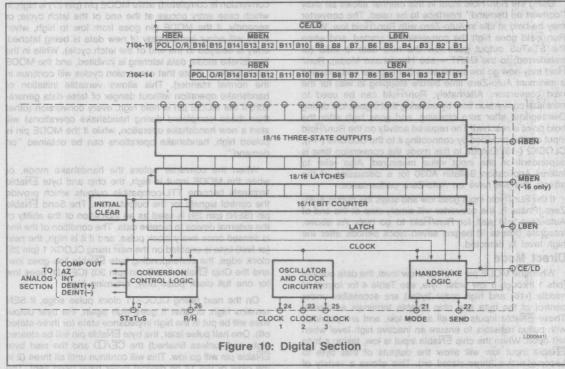
Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V $^{\pm}$  (high). Inputs driven from TTL gates should have  $3-5k\Omega$  pullup resistors added for maximum noise immunity.

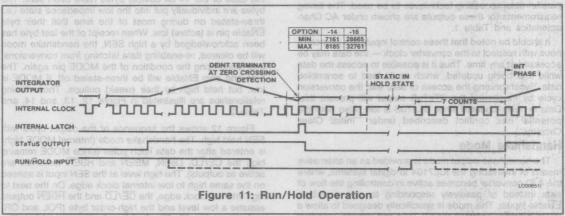
MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

## STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 9 for details of this timing. This signal may be used as a ''data valid'' flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.





## Run/Hold Input list one tot well aniemen tugtue CINE

When the Run/Hold input is connected to V<sup>+</sup> or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 9). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16 and 32768 for 7104-14 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 11 for details.

## ICL8052/ICL7104



Using the Run/Hold input in this manner allows an easy 'convert on demand' interface to be used. The converter may be held at idle in Auto-Zero with Run/Hold low. When Run/Hold goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred) to the UART - see Handshake Mode). Run/ Hold may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/Hold can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/Hold input can be provided by connecting it to the CLOCK3 (-14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

## **Direct Mode**

When the MODE pin is left at a low level, the data outputs [bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes] are accessible under control of the byte and chip ENable terminals as inputs. These ENable inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip ENable input is low, taking a byte ENable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

## Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a

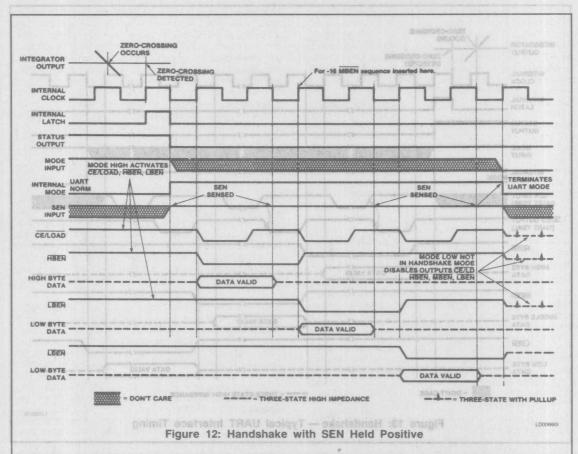
conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained ''on demand.''

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte ENable terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte ENable line goes low and the Chip ENable/LoaD pin (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte ENable pin will be cleared high, and (unless finished) the CE/LD and the next byte ENable pin will go low. This will continue until all three (2 in the case of the 14 bit device) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte ENable pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 12, 13, and 14, and

Figure 12 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the CE/LD, LBEN, MBEN and HBEN terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next to high internal clock edge, the CE/LD and the HBEN outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bits 9-14) outputs are enabled. The CE/LD output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte ENable remains low for two clock periods. Thus the CE/LD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte ENable as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using CE/LD, MBEN and LBEN while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14).





will be sensed on the next ICL7104 internal clock high to

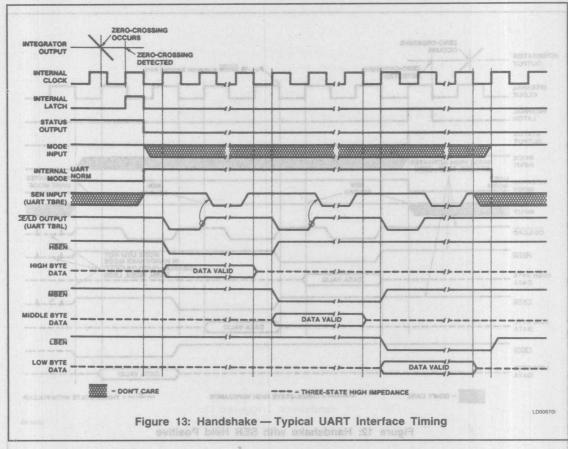
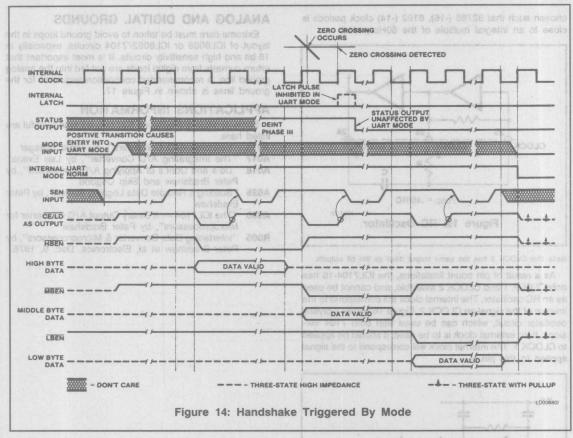


Figure 13 shows an output sequence where the SEN input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LD terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The CE/LD and HBEN terminals will go low after SEN is sensed, and the high order byte outputs become active. When CE/LD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART

TBRE output will now go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the HBEN output returns high. At the same time, the CE/LD and MBEN (-16) or LBEN outputs go low, and the corresponding byte outputs become active. Similarly, when the CE/LD returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register. and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for LBEN. One-half internal clock later, the handshake mode will be cleared, and the chip and byte ENable terminals return high and stay active (as long as MODE stays high).



With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 14 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/Hold input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

## **Initial Clear Circuitry**

The internal logic of the 7104 is supplied by an internal regulator between V ++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" F/F cleared (i.e. in "direct" mode). This, however, will also clear these

registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" F/F should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to bus conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE F/F will be cleared as fast as possible (see Figure 12 for timing). For these and other reasons, adequate supply bypass is recommended.

#### Oscillator

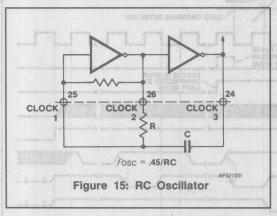
The ICL7104-14 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 15 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. A 50–100k $\Omega$  resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be

# ICL8052/ICL7104

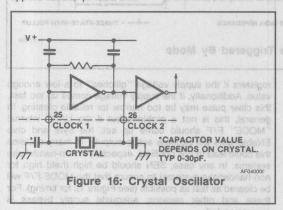
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chosen such that 32768 (-16), 8192 (-14) clock periods is close to an integral multiple of the 60Hz period.



Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 16 shows a crystal oscillator circuit, which can be used with both 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.



#### POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V+ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

#### ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL8068 or ICL8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 17.

#### **APPLICATIONS INFORMATION**

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar

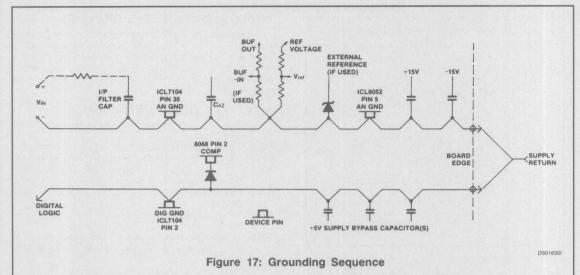
A017 "The Integrating A/D Converter", by Lee Evans

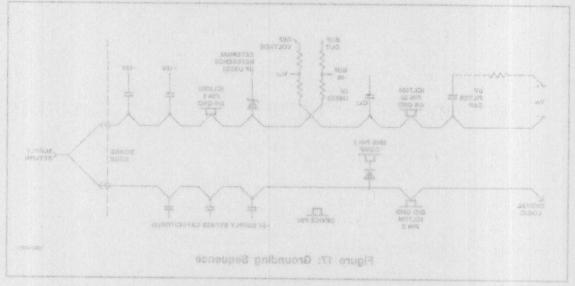
.018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood

A025 "Building a Remote Data Logging Station", by Peter Bradshaw

A030 ''The ICL7104 — A Binary Output A/D Converter for Microprocessors'', by Peter Bradshaw

R005 "Interfacing Data Converter & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.





# Section 7 — Timer/Counter Circuits

Section 7 - Timer/Counter Circuits

The Intersil ICM7206/A/B/C/D are 2-of-8 sine wave

tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate

programmable dividers, a D/A converter, and a high level

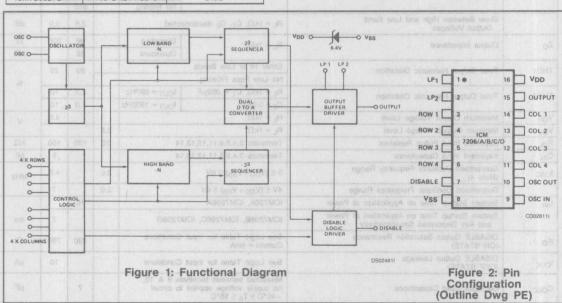
# GENERAL DESCRIPTION

- **FEATURES** · Low Cost
- Oscillator Uses 3.58MHz Color TV Crystal
- High Current Bipolar Output Driver
- Low Output Harmonic Distortion
- Wide Operating Supply Voltage Range: 3 to 6
- Uses 3 x 4 or 4 x 4 Single Contact Keypad
- Low Power (≤ 5.5mW With A 5.5V Supply)
- Single and Dual Tone Capabilities
- Multiple Key Lockout
- Disable Output: Provides Output Switch Function Whenever A Key Is Pressed Custom Options Available

#### ORDERING INFORMATION

output driver.

PART	TEMPERATURE RANGE	PACKAGE
ICM7206IPE	-40°C to +85°C	16 Pin PLASTIC DIP
ICM7206AIPE	-40°C to +85°C	16 Pin PLASTIC DIP
ICM7206BIPE	-40°C to +85°C	16 Pin PLASTIC DIP
ICM7206CIPE	-40°C to +85°C	16 Pin PLASTIC DIP
ICM7206DIPE	-40°C to +85°C	16 Pin PLASTIC DIP
ICM7206/D	-40°C to +85°C	DICE NOT A
ICM7206A/D	-40°C to +85°C	DICE
ICM7206B/D	-40°C to +85°C	DICE
ICM7206C/D	-40°C to +85°C	DICE
ICM7206D/D	-40°C to +85°C	DICE





### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage VDD-VSS (Note 2)	6.0V
Supply Current VSS (terminal 8)	25mA
Supply Current VDD (terminal 16)	40mA
Disable Output Voltage (term. 7) (VDD-6	V) to VDD
Output Voltage (term 15) (VSS-1.0V) to (V	DD + 5.0V)
Input Voltage VSS - 0.3V to	VDD + 0.3V

Output Current (terminal 15)	25mA
Power Dissipation	
Operating Temperature Range40°	C to +85°C
Storage Temperature Range55°C	to +125°C
Lead Temperature (Soldering, 10sec)	

NOTE 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The ICM7206 family has a zener diode connected between V<sub>DD</sub> and V<sub>SS</sub> having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

### ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: VDD = 5.5V, Test Circuit, VSS = 0V TA = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDIT	TIONS	MIN	TYP	MAX	UNIT
IDD	Supply Current	R <sub>L</sub> disconnected		3°08	450	1000	μΑ
VSUPPLY	Guaranteed Operating Supply Voltage Range (Note 3)	-40°C ≤ T <sub>A</sub> ≤ +85°C	10 + 86°C   16	3.0		6.0	CM72
		C <sub>1</sub> , C <sub>2</sub> disconnected — Lo	w Band	0.90	1,15	1.45	
Vout	Peak to Peak Output Voltage	$R_1 = 1k\Omega$ , no filtering — Hi		1.10	1.40	1.70	
001	RMS Output Voltage	$R_L = 1k\Omega$ , $f_{OUT} = 697Hz$	C <sub>2</sub> Only	OSSI.	480	7.00	ICM272
		3040	C <sub>1</sub> to C <sub>2</sub>	rient.	480	75.49	
		2010	No filtering	20ml	490	nyga	mV
		$R_L = 1k\Omega$ , $f_{OUT} = 1633Hz$	C <sub>1</sub>	137035	490	15.53	ICMT20
		3010	C <sub>1</sub> to C <sub>2</sub>	OFOR.	580	mak	
			No filtering		655		
	Skew Between High and Low Band Output Voltages	$R_L = 1k\Omega$ , $C_1$ , $C_2$ disconn	ected		2.5	3.0	dB
Z <sub>O</sub> Output Impedance	Output Impedance	$R_L = 1k\Omega$	Operating		90	200	Ω
20	Output impedance	TIL TANK MARKET	Quiescent		25		kΩ
THD1 Total Output Harmonic	Total Output Harmonic Distortion	Output Harmonic Distortion Either Hi or Low Bands	- Company		20	25	
pgy [ ]a	Total Output Harmonic Distortion	No Low Pass Filtering					%
THD2	Total Output Harmonic Distortion	$R_L = 1k\Omega, C_1 = .002\mu F$	four = 697Hz		2.3	10	
1102	TOTAL SURPLINE THE DISCOURT TO THE DISCOURT TO THE DISCOURT THE DISCOURT TO TH	$C_2 = 0.02 \mu F$	f <sub>OUT</sub> = 1633Hz	114	1.0	10	
Vон	Maximum Output Voltage Level	$R_L = 1k\Omega$				4.6	V
Vol	Minimum Output Voltage Level	$R_L = 1k\Omega$		0.5			
RIN	Keyboard Input Pullup Resistors	Terminals 3,4,5,6,11,12,13,	14	35	100	150	kΩ
CIN	Keyboard Input Capacitance	Terminals 3,4,5,6,11,12,13,	14		HE	5	pF
fosc	Guaranteed Oscillator Fequency Range (Note 4)	3 ≤ (V <sub>DD</sub> - V <sub>SS</sub> ) ≤ 6V	Control 1	2.0		4.5	MHz
	Guaranteed Oscillator Frequency Range	$4V \le (V_{DD} - V_{SS}) \le 6V$		2.0		7	
ton	System Startup Time on Application of Power	ICM7206, ICM7206A	and the same		10	NO.	
	System Startup Time on Application of Power and Key Depressed Simultaneously	ICM7206B, ICM7206C, ICM7206D				7	ms
RD	DISABLE Output Saturation Resistance (ON STATE)	See Logic Table for Input Conditions . Current = 4mA			330	700	Ω
OLK	DISABLE Output Leakage (OFF STATE)	See Logic Table for Input Conditions				10	μΑ
Cosc	Oscillator Load Capacitance	Measured between termina no supply voltage applied -40°C ≤ T <sub>A</sub> ≤ 85°C			7		pF

### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fo	Guaranteed Output Frequency Tolerance	Any output frequency Crystal tolerance ±60ppm Crystal load capacitance CL = 30pF			±0.75	%
tstart	Oscillator Startup Time ICM7206B,C,D	V <sub>DD</sub> - V <sub>SS</sub> = 3V (Note 5)			7	ms

NOTES: 3. Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.

4. The ICM7206 family uses dynamic high frequency circuitry in the initial 2<sup>3</sup> divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.

#### 5. After row input is enabled.

#### TRUTH TABLE

LINE	ROWS <sup>(1)</sup>	COLS(2) ACTIVATED	OUTPUT (TERMINAL #15)	DISABLE (TERMINAL #7)	COMMENTS
1	0	0	Off	Off	Quiescent State
2	1	1	frow + fcol	On -a	Dual Tone
3	1	2 or 3 (incl. col #4)	frow	On	Single Tone
4	2 or 3	1	fcol	On	Single Tone
5	2 or 3	2 or 3 (excl. col #3)	D.C. Level	On	No Tone
6	1	4 or 3 (must excl. col #4)	frow, 50% Duty Cycle	frow, 50% Duty Cycle	f <sub>row</sub> Test
7	4	1 9,83 - 50	f <sub>col</sub> , 50% Duty Cycle	f <sub>col</sub> , 50% Duty Cycle	f <sub>col</sub> Test
8	0	1 or 2 or 3 or 4	Off	Off	n/a*
9	meresor 1	O Chworla sasiyab biase	902Hz + f <sub>row</sub>	On .	n/a*
10	2 or 3	Ouron sanian nice	902Hz	On	n/a*
-11	4	0	902Hz, 50% Duty Cycle	902Hz, 50% Duty Cycle	n/a*
12	2 or 3 or 4	4	D.C. Level	Indeterminate	Multiple Key Lockout
13	4	2 or 3 or 4	D.C. Level	Indeterminate	Multiple Key Lockout

\*n/a -- not applicable to telephone calling

1. Hows are activated for the ICM7206/C by connecting to a negative supply voltage with respect to V<sub>DD</sub> (terminal 16) at least 33% of the value of the supply voltage (V<sub>DD</sub> – V<sub>SS</sub>). For the ICM7206A rows (and columns) are activated by connecting to a positive supply voltage with respect to V<sub>SS</sub> (terminal 8) at least 33% of the value of the supply voltage (V<sub>DD</sub> – V<sub>SS</sub>). The rows and columns of the ICM7206B are activated by connecting to a negative supply voltage.

 Columns (ICM7206) are activated by being connected to a positive supply voltage with respect to V<sub>SS</sub> (terminal 8) at least 33% of the value of the supply voltage (V<sub>DD</sub> – V<sub>SS</sub>).

#### **OPTIONS**

# (For additional information consult the factory)

Options can be achieved using metal mask additions to provide the following.

- The sequence or position of either the row or column terminals can be interchanged i.e., row 1 terminal 3 could become terminal 11, etc.
- 2) Any frequency oscillator from approximately 0.5MHz to 7MHz can be chosen. Note that the accuracy of the output frequencies will depend on the exact oscillator frequency. For instance, a 1MHz crystal could be used with worst case output frequency error of 0.8%. Or, if high accuracy is required, ±0.25%, oscillator frequencies of 5,117,376Hz or 2,558,688Hz could be selected. ROM's are used to program the dividers.
- The 'DISABLE' output may be changed to an inverter or an uncommitted drain n-channel transistor.
- The oscillator may be disabled until a key is depressed.

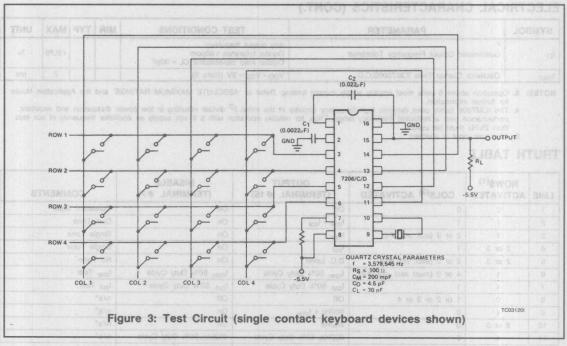
#### COMMENTS

All combinations of row and column activations are given in the truth table. Lines 1 through 7 and 12, 13 represent conditions obtainable with a matrix keyboard. Lines 8 thru 11 are given only for completeness and are not pertinent to telephone dialing.

Lines 6 and 7 show conditions for generating 50% duty cycle full amplitude signals useful for rapid testing of the row and column frequencies on automatic test equipment. In all other cases, output frequencies on terminal 15 are single or dual 4 level synthesized sine waves.

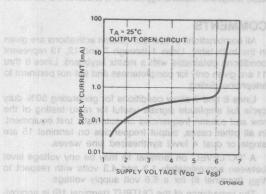
A 'DC LEVEL' on terminal 15 may be any voltage level between approximately 1.2 and 4.3 volts with respect to Vss (terminal 8) for a 5.5 volt supply voltage.

The impedance of the OUTPUT (terminal 15) is approximately 20k ohms in the OFF state. The 'DISABLE OUT-OUT' ON and OFF conditions are defined in the TYPICAL PERFORMANCE CHARACTERISTICS.

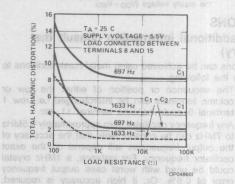


#### TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION AS A FUNCTION OF LOAD RESISTANCE

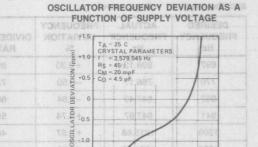


7-4

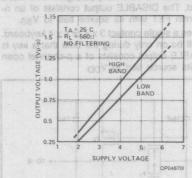
## TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

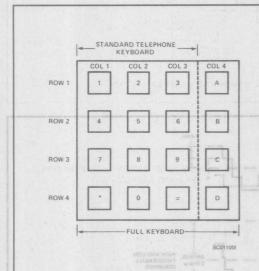
SUPPLY VOLTAGE

OP04850



#### PEAK TO PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE of the odd on





KEY	LOW BAND FREQ. Hz	HI BAND FREQ. Hz
1	697	1209
2	697	1336
ns 31510	697	1477
4 10	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
	941	1209
0	941	1336
1001#1	941	1477
Α	697	1633
BI SIMA	770	1633
C	852	1633
D	941	1633

Figure 4: Keyboard Frequencies

#### DETAILED DESCRIPTION

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately -3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to VDD.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to VDD. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its source is connected to VDD.

The 7206B requires a 4 + 4 double contact keyboard with the common line tied to VSS. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE

output consists of an n-channel open drain FET with its source tied to Vss.

The 7206C uses either a  $3 \times 4$  or  $4 \times 4$  single contact keyboard; the oscillator will be on only during the time that a key is depressed. The DISABLE output consists of an n-channel open drain FET with its source tied to Vss.

The 7206D uses a single contact  $3 \times 4$  or  $4 \times 4$  keyboard. The oscillator will be on only during the time that a key is depressed. DISABLE output consists of a p-channel open drain FET with its source tied to  $V_{DD}$ .

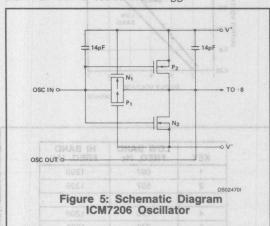
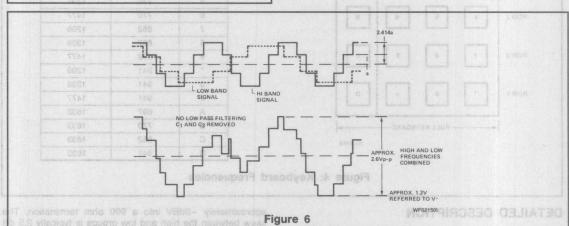


Figure 6 shows individual currents of a low band and high band frequency pair into the summing node A (see Figure 7) and the resultant voltage waveform.

DESIRED FREQUENCY Hz	ACTUAL FREQUENCY Hz	FREQUENCY DEVIATION %	DIVIDE BY N RATIO
697	699.13	+0.30	80
770	766.17	-0.50	73
852	847.43	-0.54	66
941	947.97	+0.74	59
1209	1215.88	+0.57	46
1336	1331.68	-0.32	42
1477	1471.85	-0.35	38
1633	1645.01	+0.74	34



7.0

The ICM7206 family is manufactured with a standard metal gate CMOS technology having proven reliability and excellent reproducability resulting in extremely high yields. The techniques used in the design have been developed over many years and are characterized by wide operating supply voltage ranges and low power dissipation.

To minimize chip size, all diffusions used to define source-drain regions and field regions are butted up together. This results in approximately 6.3 volt zener breakdown between the supply terminals, and between all components on chip. As a consequence, the usual CMOS static charge problems and handling problems are not experienced with the ICM7206.

The oscillator consists of a medium size CMOS inverter having on chip a feedback resistor and two capacitors of 14pF each, one at the oscillator input and the other at the oscillator output. The oscillator is followed by a dynamic ÷ 2³ circuit which divides the oscillator frequency to 447, 443Hz. This is applied to two programmable dividers each capable of division ratios of any integer between 1 and 128, and each counter is controlled by a ROM. The outputs from the programmable counters drive sequencers (divide by 8) which generate the eight time slots necessary to synthesize the 4-level sine waves.

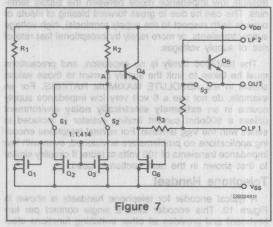
The control logic block recognizes signals on the row and column inputs that are only a small fraction of the supply voltage, thereby permitting the use of a simple matrix single contact per key keyboard, rather than the more usual two contacts per key type having a common line. The row and column pullup resistors are equal in value and connected to the opposite supply terminals (ICM7206/C only; for the ICM7206A all pullup resistors are connected to the VSS terminal and for the ICM7206B they are tied to the VDD. Therefore, connecting a row input to a column input generates a voltage on those inputs which is one half of the supply voltage.

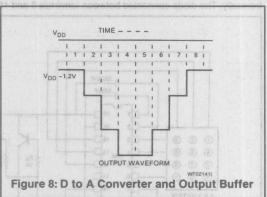
The ICM7206 family employs a unique but extremely simple digital to analog (D to A) converter. This D to A converter produces a 4 level synthesized sine wave having an intrinsic total harmonic distortion level of approximately 20%. Figure 8 shows a single channel D to A converter. The current sources  $\rm Q_2$  and  $\rm Q_3$  are proportioned in the ratio of 1:1.414. During time slots 1 and 8 both S1 and S2 are off, during time slots 2 and 7 only S1 is on, during time slots 3 and 6 only S2 is on, and during time slots 4 and 5 both S1 and S2 are on. The resultant currents are summed at node A, buffered by  $\rm Q_4$  and further buffered by R3, R4 and Q5. Switch S3 allows the output to go into a high impedance mode under quiescent conditions.

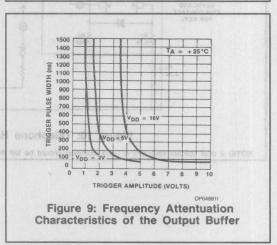
Node A is the common summing point for both the high and low band frequencies although this is not shown in Figure 8.

The synthesized sine wave has negligible even harmonic distortion and very low values of third and fifth harmonic distortion thereby minimizing the filtering problems necessary to reduce the total harmonic distortion to well below the 10% level required for touch tone telephone encoding. Figure 9 shows the low pass filter characteristic of the output buffer for  $C_1 = 0.0022\mu\text{F}$  and  $C_2 = 0.022\mu\text{F}$ . A small

produces a sharper and more desirable knee characteristic than would two simple cascaded RC networks.







# Latchup Considerations

Most junction isolated CMOS integrated circuits, especially those of moderate or high complexity, exhibit latchup phenomena whereby they can be triggered into an uncontrollable low impedance mode between the supply terminals. This can be due to gross forward biasing of inputs or outputs (with respect to the supply terminals), high voltage supply transients, or more rarely by exceptional fast rate of rise of supply voltages.

The ICM7206 family is no exception, and precautions must be taken to limit the supply current to those values shown in the ABSOLUTE MAXIMUM RATINGS. For an example, do not use a 6 volt very low impedance supply source in an **extremely electrically noisy** environment unless a 500ohm current limiting resistor is included in series with the Vss terminal. For normal telephone encoding applications no problems are envisioned, even with low impedance transients of 100 volts or more, if circuitry similar to that shown in the next section is used.

#### Telephone Handset

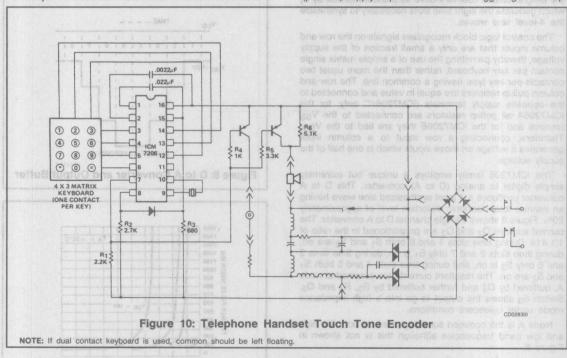
A typical encoder for telephone handsets is shown in Figure 10. This encoder uses a single contact per key keyboard and provides all other switching functions electronically. The diode connected between terminals 8 and 15

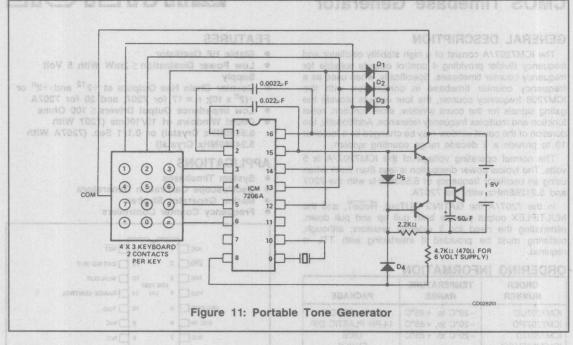
prevents the output going more than 1 volt negative with respect to the negative supply VSS and the circuit operates over the supply voltage range from 3.5 volts to 15 volts on the device side of the bridge rectifier. Transients as high as 100 volts will not cause system failure, although the encoder will not operate correctly under these conditions. Correct operation will resume immediately after the transient is removed.

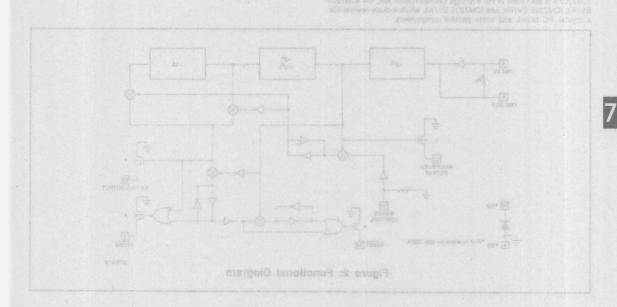
The output voltage of the synthesized sine wave is almost directly proportional to the supply voltage (V<sub>DD</sub>–V<sub>SS</sub>) and will increase with increase of supply voltage until zener breakdown occurs (approximately 6.3 volts between terminals 8 and 16) after which the output voltage remains constant.

#### Portable Tone Generator

The ICM7206A/B require a two contact key keyboard with the common line connected to the positive supply (neg for ICM7206B) (terminal 16). A simple diode matrix may be used with this keyboard to provide power to the system whenever a key is depressed, thus avoiding the need for an on/off switch. In Figure 11 the tone generator is shown using a 9 volt battery. However, if instead, a 6 volt battery is used, the diode  $D_4$  is not required. It is recommended that a 4700hm resistor still be included in series with a negative (positive) supply to prevent accidental triggering of latchup.







# ICM7207/A CMOS Timebase Generator



#### **GENERAL DESCRIPTION**

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts. The typical power dissipation is less than 2mW when using an oscillator frequency of 6.5536MHz with the 7207 and 5.24288mHz with the 7207A.

In the 7207/A the GATING OUTput, ReSeT, and the MULTIPLEX output provide both pull up and pull down, eliminating the need for 3 external resistors; although, buffering must be provided if interfacing with TTL is required.

#### ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7207IJD ICM7207IPD ICM7207/D ICM7207EV/Kit	-20°C to +85°C -20°C to +85°C -20°C to +85°C -	1'4-Pin CERDIP 14-Pin PLASTIC DIP DICE EV/Kit*
ICM7207AIJD ICM7207AIPD ICM7207A/D ICM7207AEV/Kit	-20°C to +85°C -20°C to +85°C -20°C to +85°C	14-Pin CERDIP 14-Pin PLASTIC DIP DICE EV/Kit*

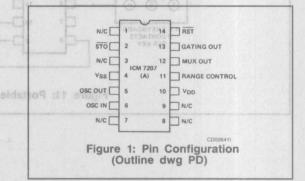
\*These EV/Kits contain just the IC and the corresponding crystal. The ICM7207A is also used in the 4<sup>1</sup>/<sub>2</sub>-Digit Counter/Driver kits, the ICM7224 EV/Kit, ICM7225 EV/Kit, and ICM7236 EV/Kit, which include several ICs, a crystal, PC board, and some passive components.

#### **FEATURES**

- Stable HF Oscillator
- Low Power Dissipation ≤ 2mW With 5 Volt Supply
- Counter Chain Has Outputs at  $\div 2^{12}$  and  $\div 2^{n}$  or  $\div (2^{n} \times 10)$ ; n = 17 for 7207, and 20 for 7207A
- Low Impedance Output Drivers ≤ 100 Ohms
- Count Windows of 10/100ms (7207 With 6.5536MHz Crystal) or 0.1/1 Sec. (7207A With 5.24288MHz Crystal)

#### **APPLICATIONS**

- System Timebases
- Oscilloscope Calibration Generators
- Marker Generator Strobes
- Frequency Counter Controllers



SOSCIN AND STORE

WAS "Full inverters on ICM 7207A RESET TALL

Figure 2: Functional Diagram

10 Voc RESET TALL

11 Voc RESET TALL

11 Voc RESET TALL

12 Voc RESET TALL

12 Voc RESET TALL

13 Voc RESET TALL

14 Voc RESET TALL

15 Voc RESET TALL

16 Voc RESET TALL

17 Voc RESET TALL

17 Voc RESET TALL

18 DOOS 121

#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD - VSS)	Output Currents
Input VoltagesVSS - 0.3V to VDD + 0.3V	Power Dissipation @ 25°C Note 1200mW
Output Voltages:	Operating Temperature Range20°C to +85°C
7207V <sub>SS</sub> to +6V	Storage Temperature Range55°C to +125°C
7207AV <sub>DD</sub> to V <sub>SS</sub>	Lead Temperature (Soldering, 10sec)300°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

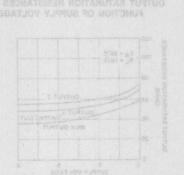
#### **ELECTRICAL CHARACTERISTICS**

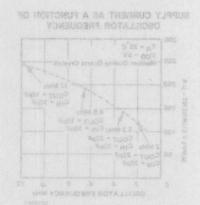
 $f_{OSC} = 6.5536 MHz(7207)$ , 5.24288 MHz(7207A),  $V_{DD} = 5V$ ,  $T_{A} = 25^{\circ}C$ ,  $V_{SS} = 0V$ , test circuit unless otherwise specified.

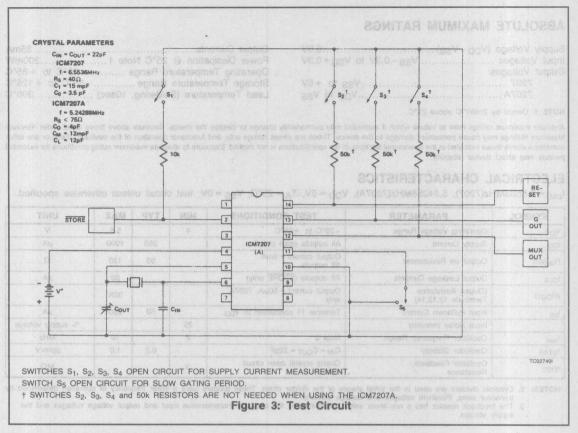
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	INCHES UNIT
V <sub>DD</sub>	Operating Voltage Range	-20°C to +85°C	4		5.5	V
IDD	Supply Current	All outputs open circuit		260	1000	μΑ
R <sub>ds</sub> (on)	Output on Resistances	Output current = 5mA All outputs		50	120	Ω
lolk	Output Leakage Currents	All outputs (STORE only)			50	μΑ
(Rout)	(Output Resistance Terminals 12,13,14)	Output current = 50μA, 7207A only			33K	Ω
lpd	Input Pulldown Current	Terminal 11 connected to V <sub>DD</sub>		50	200	μА
	Input Noise Immunity		25		MEAN IN	% supply voltage
fosc	Oscillator Frequency Range	Note 2	2	-0	10	MHz
fSTAB .	Oscillator Stability	C <sub>IN</sub> = C <sub>OUT</sub> = 22pF		0.2	1.0	ppm/V
rosc	Oscillator Feedback Resistance	Quartz crystal open circuit Note 3	20-3 DU	DIFIC MEN	S. S. C	SWITCHES SILES

NOTES: 2. Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.

3. The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

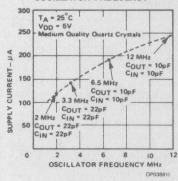




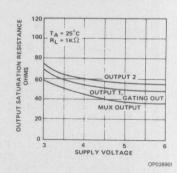


#### TYPICAL PERFORMANCE CHARACTERISTICS

# SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY

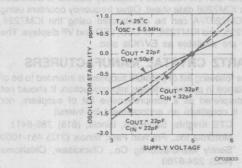


# OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE

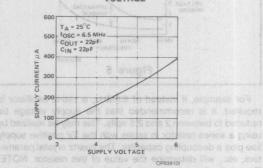


### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

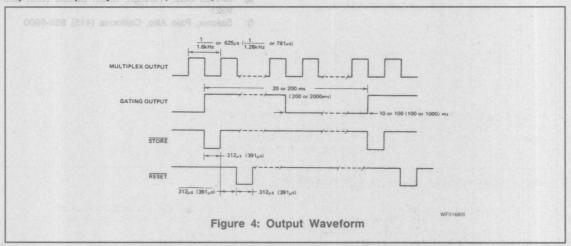
OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



### OUTPUT TIMING WAVEFORMS 7207 (7207A) Crystal Frequency = 6.5536(5.24288)MHz



#### **DETAILED DESCRIPTION**

Referring to the Test Circuit, Figure 3, the crystal oscillator frequency is divided by  $2^{1/2}$  to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to  $V_{DD}$  or  $V_{SS}$  (open circuit).

#### OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

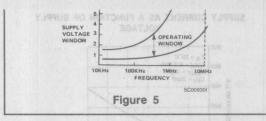
It is recommended that the crystal load capacitance ( $C_L$ ) be no greater than 15pF for a crystal having a series resistance equal to or less than  $75\Omega$ , otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance  $\pm 10 ppm$ , a low series resistance (less than  $25\Omega)$ , a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor  $C_{IN}$  should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05ppm per 0.1 volt change of supply voltage.

#### FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.



For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet. Other frequency counters using the ICM7207/A can be constructed using the ICM7224, ICM7225, and ICM7236, for LCD, LED and VF displays. The latter are available as EV/Kits also.

#### QUARTZ CRYSTAL MANUFACTURERS

The following list of possible suppliers is intended to be of assistance in putting a design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Intersil.

- a) CTS Knights, Sandwich, Illinois, (815) 786-8411
- b) Motorola Inc., Franklin Park, Illinois (312) 451-1000
- Sentry Manufacturing Co., Chickasaw, Oklahoma (405) 224-6780
- d) Tyco Filters Division, Phoenix, Arizona (602) 272-7945
  - e) M-Tron Inds., Yankton, South Dakota (605) 665-9321
  - f) Saronix, Palo Alto, California (415) 856-6900

ANTIRE STATE OF THE ACT OF THE AC

if a very high quality oscillator is desired, it is recommended that a querts crystal be used having a bight busing inderance it toppin, a low series resistance (less than 2553) is low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C<sub>BN</sub> should be 36pF and the oscillator funing capacitor should range between approximately 3 and 60pF.

Use of a high queltly crystal will result in typical oscillator stabilities of 0.05ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM/207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but laster them the disadvantage that there is a maintum consenting trausering at a given succly voltage.

DETAILED DESCRIPTION

Retering to the Test Circuit, Figure 3, the crystel oscillator requency is divided by 2<sup>12</sup> to provide both the multiplex requency and generalls the output pialse widths. The SATING OUTPUT provides a 50% duly cycle signal whose serious apon whether the RANGE CONTROL serious is non-neighborhood to Vigo or Vigo fopen circuit.

The oscillator consists of a GMOS inverter with a nonlinear reservation comerciad between the input and output linear reservation brasing Oscillator stabilities or approximately but comper 0.1 well change are active value at a supply voltage of 5 volts, using low cost crystals. The crystal epochications are shown in the TEST CIRCUIT.

If is recommended that the crystal load capacitance (C) be no greater than 15pF for a crystal having a sense resestance equal to or loss than 75t3, otherwise the output amountains of the oscillator may be too low to drive the

# ICM7208 7-Digit LED Display Counter

### GENERAL DESCRIPTION

The ICM7208 is a fully integrated seven decade counterdecoder-driver and is manufactured using Intersil's low voltage metal gate C-MOS process.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signal gating.

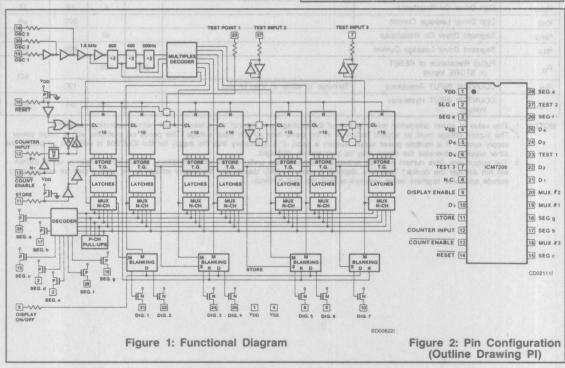


#### **FEATURES**

- Low Operating Power Dissipation < 10mW</li>
- Low Quiescent Power Dissipation < 5mW</li>
- Counts and Displays 7 Decades
- Wide Operating Supply Voltage Range
   2V ≤ V<sub>DD</sub> ≤ 6V
- Drives Directly 7 Decade Multiplexed Common Cathode LED Display
- Internal Store Capability
- Internal Inhibit to Counter Input
- Test Speedup Point

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7208IPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7208IJI	-20°C to +85°C	28 Lead CERDIP
ICM7208/D	aply Voltage Range	DICE



### ICM7208



#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (Note 2) (VDD-VSS)6V
Input Voltage Range (any input terminal)
(Note 2)VSS-0.3V to VDD+0.3V
Output Digit Drive Current (Note 3)150mA
Output Segment Drive Current30mA

Power Dissipation (Note 1)	1W
Operating Temperature Range	20°C to +85°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10sec)	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device, These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS (VDD = 5V, VSS = 0V, TA = 25°C, display off, unless otherwise specified)

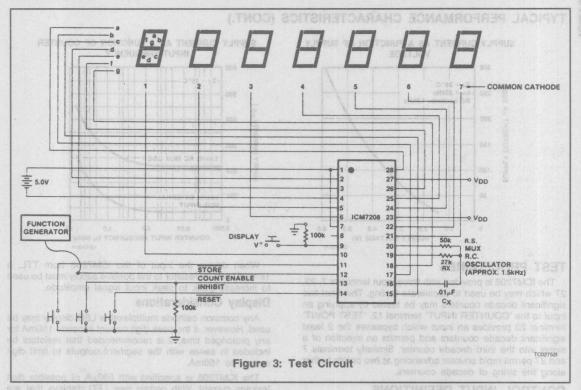
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
lQ1	Quiescent Current	All controls plus terminal 19 connected to VDD No multiplex oscillator	of bal	30	300	Of entire
IQ2 red 80	Quiescent Current	All control inputs plus terminal 19 connected to V <sub>DD</sub> except STORE which is connected to V <sub>SS</sub>	nge for	70	350	1201 0101 200
IDD1	Operating Supply Current	All inputs connected to V <sub>DD</sub> , RC multiplexer osc operating f <sub>in</sub> < 25kHz	M LIGHT IN	210	500	Aug Aug
I <sub>DD2</sub>	Operating Supply Current	fin = 2MHz	8 8 885	WORL THE	700	Chirlo QL 16
VSUPPLY	Supply Voltage Range	f <sub>in</sub> ≤ 2MHz	3.5		5.5	V
Roig	Digit Driver On Resistance		many de	4	12	Ω
IDIG	Digit Driver Leakage Current				500	μΑ
rseg	Segment Driver On Resistance	3		40		Ω
ISLK	Segment Driver Leakage Current	\$ \$ FFFF 1	Section Section	968 NW	500	μΑ
Rp	Pullup Resistance of RESET or STORE Inputs	多	100	400		kΩ
RIN	COUNTER INPUT Resistance	Terminal 12 either at V <sub>DD</sub> or V <sub>SS</sub>			100	Nac
V <sub>HIN</sub>	COUNTER INPUT Hysteresis Voltage			25	50	mV

NOTES: 1. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.

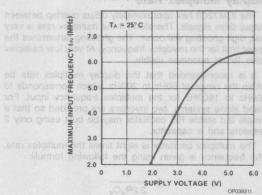
other supplies otherwise the device may be permanently damaged.

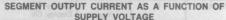
3. The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

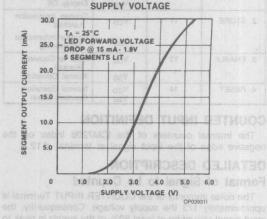


#### TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

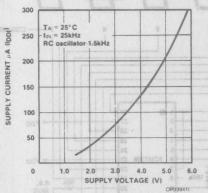






7-17

# SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



#### TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

#### CONTROL INPUT DEFINITIONS

INPUT	INPUT TERMINAL V		FUNCTION
1. DISPLAY	AS PENNO		Display On Display Off
2. STORE	111	V <sub>DD</sub>	Counter Information Latched
		Vss	Counter Information Transferring
3. ENABLE	13	V <sub>DD</sub>	Input to Counter Blocked
		Vss	Normal Operation
4. RESET	14	V <sub>DD</sub> V <sub>SS</sub>	Normal Operation Counters Reset

#### COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

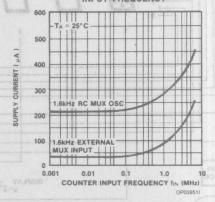
#### **DETAILED DESCRIPTION**

## Format of Signal to be Counted

The noise immunity of the COUNTER INPUT Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply.

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately  $10^{-4} \text{V}/\mu\text{s}$  at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

# SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY



When driving the input of the ICM7208 from TTL, a  $1k-5k\Omega$  pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

#### **Display Considerations**

Any common cathode multiplexable LED display may be used. However, if the peak digit current exceeds 150mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with  $500\mu A$  of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

### Display Multiplex Rate

The ICM7208 has approximately  $0.5\mu s$  overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

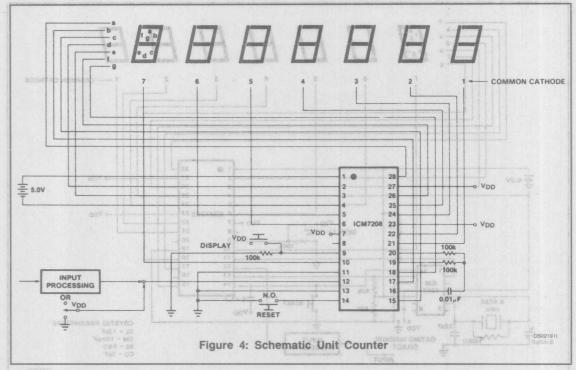
It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input. For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

The multiplex oscillator is eight times the multiplex rate. The frequency is given using the following formulii:

(v) Sparsov vuf = 
$$\frac{1}{2.2R_xC_x}$$

 $R_S$  should always be  $\,\leq 1 M \Omega$  and  $R_S = k R_X$  where k is in the range 2-10.

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.



#### **Unit Counter**

Figure 4 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If  $4 \times 1.5$  volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

#### Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 5). The ICM7207 uses a crystal controlled oscillator to provide the store and reset pulses together with

the counting window. Figure 6 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches, and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

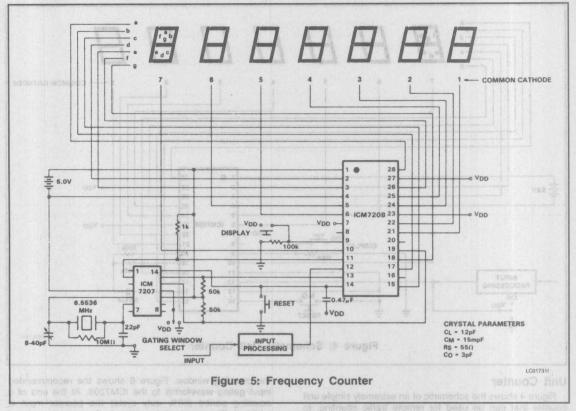
Using a 6.5536MHz quartz crystal and the ICM7207 driving the ICM7208, two ranges of counting may be obtained, using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

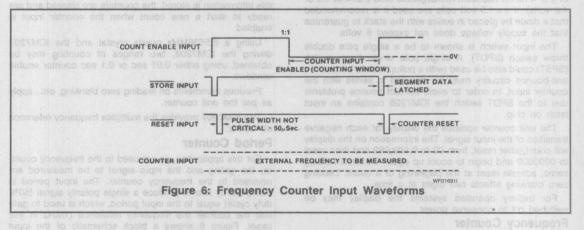
The ICM7207 provides the multiplex frequency reference of 1.6kHz.

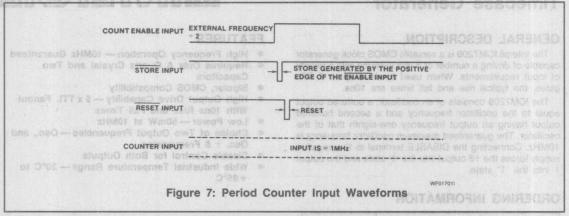
#### **Period Counter**

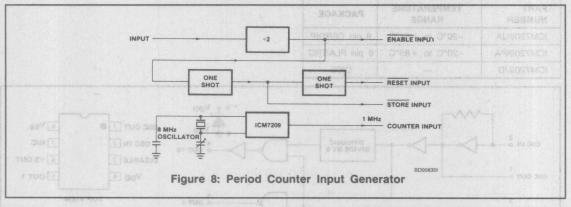
For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure 8 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 7.



Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.







7

Pld i is designated by either a dot

# ICM7209 Timebase Generator



#### GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

# FEATURES

- High Frequency Operation 10MHz Guaranteed
- Requires Only A Quartz Crystal and Two Capacitors
- Bipolar, CMOS Compatibility
- High Output Drive Capability 5 x TTL Fanout With 10ns Rise and Fall Times
- Low Power 50mW at 10MHz
- Choice of Two Output Frequencies Osc., and Osc. ÷ 8 Frequencies
- Disable Control for Both Outputs
- Wide Industrial Temperature Range 20°C to +85°C

# Figure 7: Period Counter Input Wavefor NOITAMROANI BRIDANO

PART NUMBER	TEMPERATURE RANGE	PACKAGE	
ICM7209IJA	-20°C to +85°C	8 pin CERDIP	
ICM7209IPA	-20°C to +85°C	8 pin PLASTIC	
ICM7209/D		DICE	

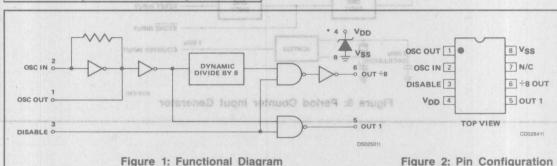


Figure 1: Functional Diagram
\*Zener Voltage is Typically 6.3 Volts

Figure 2: Pin Configuration (Outline dwg PA) Pin 1 is designated by either a dot or a notch

Supply Voltage	6V
Output VoltagesVSS - 0.3V to VDD + 0.	3V
Input VoltagesVSS - 0.3V to VDD + 0.	31

Power Dissipation (25°C)	.300mW
Storage Temperature55°C to	+125°C
Operating Temperature Range20°C to	+85°C
Lead Temperature (Soldering, 10sec)	

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

(VDD - VSS = 5V±10%, test circuit, fosc = 10MHz, TA = 25°C unless otherwise specified.)

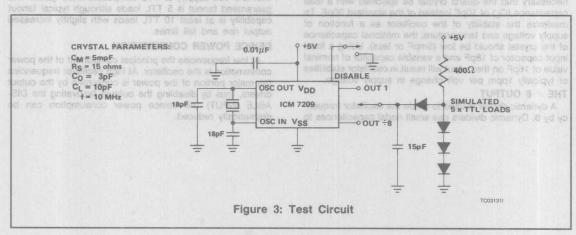
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD BOATION	Supply Current	Note 1 No Load		11	20	mA
C <sub>D</sub>	Disable Input Capacitance		19107-39	5	199	pF
lilk	Disable Input Leakage	Either '1' or '0' state	L		±10	μΑ
FOR THE TOTAL TOTAL	Output Low State	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	1000000	1055Hz	0.4	14,8001 V
Voh	Output High State	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	4.0	4.9		
t <sub>R</sub>	Output Rise Time (Note 3)	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10		ns
te beau ers doldw	Output Fall Time (Note 3)	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	11	0110 FC	раза а	DETAIL
fosc	Minimum OSC Frequency for ÷8 Output	Note 2	2 2/4	DITARBO	SMOO HO	MHZ
ndow of operation. PERFORMANCE	Output ÷8 duty cycle	Any operating frequency Low state : High state	sen erb ne	7:9		ricear resist
GM	Oscillator Transconductance	DARIAND COMMITTEE CHARAC	80	200	CALCIE SUNG	μs

NOTES: 1. The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent

by the oscillator tank components.

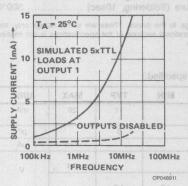
2. The ÷8 circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the and a consumption and a significantly improve high frequency performance and to decrease power consumption absolutely a new electronic consumption and a significantly improve high frequency performance and to decrease power consumption absolutely and the significant in the signi

3. Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

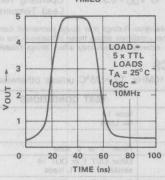


# 

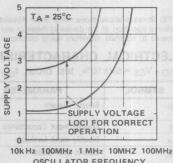
SUPPLY CURRENT AS A FUNCTION TYPICAL OUT 1 RISE AND FALL OF OSCILLATOR FREQUENCY



TIMES & O + naV of



SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF +8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY.



OSCILLATOR FREQUENCY

Rise and fall times of OUT ÷8 are similar to those of OUT 1.

#### DETAILED DESCRIPTION

#### OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a nonlinear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10kHz) to 10MHz.

The oscillator circuit consumes about 500 µA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (CL) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

#### THE + 8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to

store voltage levels instead of latches (which are used in static dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see TYPICAL PERFORMANCE CHARACTERISTICS).

#### **OUTPUT DRIVERS**

The output drivers consist of CMOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other CMOS gates operating with a 5 volt supply, or TTL compatible MOS gates. The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

#### DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DIS-ABLE INPUT) the device power consumption can be dramatically reduced.

# ICM7213

# One Second/One Minute Timebase Generator

# GENERAL DESCRIPTION

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304MHz crystal will produce a variety of output frequencies including 2048Hz, 1024Hz, 34.133Hz, 16Hz, 1Hz, and 1/60Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate CMOS technology which uses 6.4 volt zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (See Figure 7).

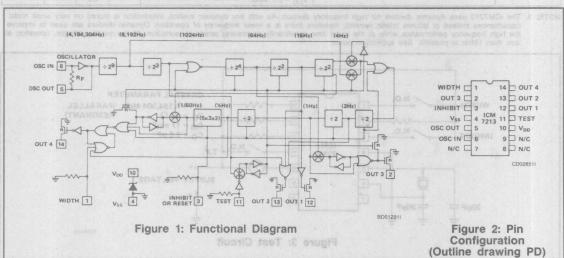
#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7213IJD	-20°C to +85°C	14 pin CERDIP
ICM7213IPD	-20°C to +85°C	14 pin PLASTIC DIP
ICM7213/D	1.0	DICE



#### **FEATURES**

- Guaranteed 2 Volts Operation
- Very Low Current Consumption: Typ. 100μA @
   3V
- All Outputs TTL Compatible
- On Chip Oscillator Feedback Resistor
- Oscillator Requires Only 3 External Components: Fixed Capacitor, Trim Capacitor, and A Quartz Crystal
- Output Inhibit Function
- 4 Simultaneous Outputs: One Pulse/Sec, One Pulse/Min, 16Hz and Composite 1024 + 16 + 2Hz Outputs
- Test Speed-Up Provides Other Frequency Outputs



Supply Voltage (V <sub>DD</sub> – V <sub>SS</sub> )	Operating Temperature Range20°C to +85°C Storage Temperature Range40°C to +125°C
All Input and Oscillator Voltages (Note 1)	Power Dissipation (Note 2)200mW
V <sub>SS</sub> -0.3V to V <sub>DD</sub> +0.3V	Lead Temperature (Soldering, 10sec)300°C
All Output Voltages (Note 1)VSS to 6.0V	TOTALIST SAMODOLOUIT DEITS BOUND IN THE TOTAL STANDARD BUTT.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: The ICM7213 like most CMOS devices, may enter a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting.

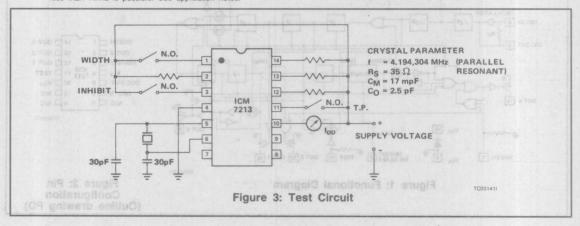
NOTE 2: Derate linearly power rating of 200mW at 25°C to 50mW at 70°C.

### ELECTRICAL CHARACTERISTICS

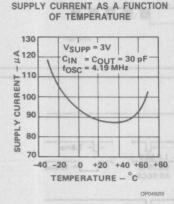
(V<sub>DD</sub> - V<sub>SS</sub> = 3.0V, f<sub>osc</sub> = 4.194304MHz, Test Circuit, T<sub>A</sub> = 25°C unless otherwise specified)

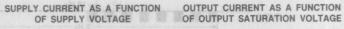
SYMBOL	PARAMETER	TEST CONDITIONS		TYP	MAX	UNIT
IDD YOUR	Supply Current	shity, the ICMZZ13 is finited 10	upaend	100	140	μΑ
VSUPPLY	Guaranteed Operating Supply Voltage Range (VDD - VSS)	-20°C < T <sub>A</sub> < 85°C	2	d qeo x	BEALE TEMPE	v v
lolk	Output Leakage Current	Any output, Vout = 6 Volts	13 (Se	ov B G	10	μΑ
ROUT	Output Sat. Resistance	Any output, I <sub>OLK</sub> = 2.5mA	CA SAIN	120	200	Ω
l <sub>1</sub>	Inhibit Input Current	Inhibit terminal connected to VDD	P-75013.	10	40	Last rate and
ITP	Test Point Input Current	Test point terminal connected to V <sub>DD</sub>	ARRO	10	40	μΑ
lw	Width Input Current	Width terminal connected to V <sub>DD</sub>	SUCCESSION OF THE SECOND	10	40	PER SE
9m	Oscillator g <sub>m</sub>	V <sub>DD</sub> = 2V	100	08-	Chies	μs
fosc	Oscillator Frequency Range (Note 3)	- BE°C   14 pm PLASTIC	o1 3°	084	(10	MHz
fSTAB .	Oscillator Stability	2V < V <sub>DD</sub> < 4V		1.0	Malan	ppm
ts	Oscillator Start Time	anio		0.1	Centre	sec
		V <sub>DD</sub> = 2.0 volts		0.2	-	300

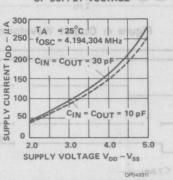
NOTE: 3. The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible. See application notes.

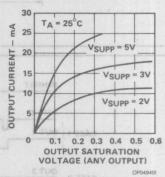


### TYPICAL PERFORMANCE CHARACTERISTICS

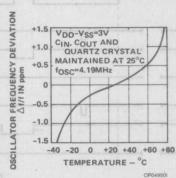




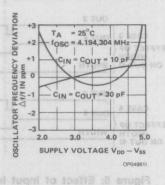




OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE



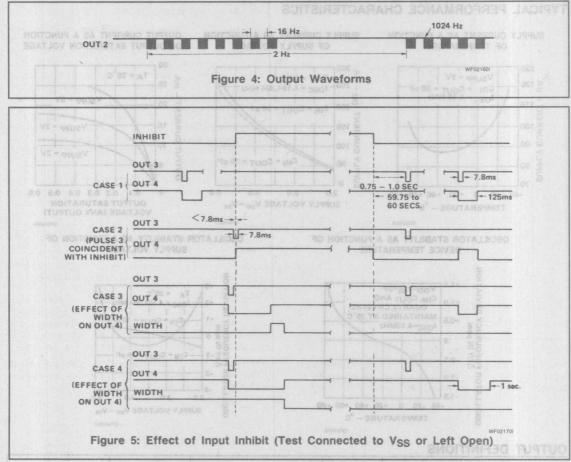
#### OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



#### OUTDUT DEFINITIONS

INPUT STATES*		PIN 12 PIN 13		PIN 2	PIN 14	
TEST	INHIBIT	WIDTH	OUT 1 OUT 2		OUT 3	OUT 4
L	L	L	16Hz ÷2 <sup>18</sup>	1024 + 16 + 2Hz (+212 + 122 + 123 +	1Hz, 7.8ms ÷2 <sup>22</sup>	1/60Hz, 1 Sec. ÷(2 <sup>24</sup> x 3 x 5)
MOTHRA	1	Н	16Hz ÷2 <sup>18</sup>	1024 + 16 + 2Hz (÷2 <sup>12</sup> ÷2 <sup>18</sup> ÷2 <sup>21</sup> ) composite	1Hz, 7.8ms ÷2 <sup>22</sup>	1/60Hz, 125ms
L	Н	L	16Hz ÷2 <sup>18</sup>	1024 + 16Hz (÷2 <sup>12</sup> ÷2 <sup>18</sup> ) composite	OFF STEDISTICS	OFF STOV MARGIN
L	Н	Н	16Hz ÷2 <sup>18</sup>	1024 + 16Hz (÷2 <sup>12</sup> ÷2 <sup>18</sup> ) composite	OFF OS mon as	SEE WAVEFORMS
H <sub>am</sub> H <sub>a</sub> nobseq(	L Correct (	L o wobniW	ON	4096 + 1024Hz (÷2 <sup>10</sup> ÷2 <sup>12</sup> ) composite	2048Hz ÷2 <sup>11</sup>	34.133Hz, 50% D.C. ÷(2 <sup>13</sup> x 5 x 3)
Н	L	Н	ON	4096 + 1024Hz (÷2 <sup>10</sup> ÷2 <sup>12</sup> ) composite	2048Hz ÷2 <sup>11</sup>	34.133Hz, 50% D.C. ÷(2 <sup>13</sup> x 5 x 3)
rebivib rotals		ago og ure to opply by using cocceso) by		1024Hz set to relined edit / ÷2 <sup>12</sup> allow	approximately 1.7	the supply voltaged or
The state of the s		consultaption		1024Hz ÷2 <sup>12</sup>	ON	OFF

NOTE: When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

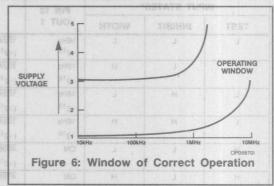


All time scales are arbitrary, and in the case of OUT 3 only the pulses coinciding with the negative edge of OUT 4 are shown. Where time intervals are relevant they are clearly shown.

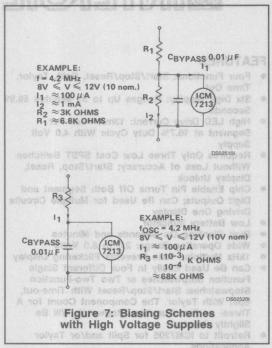
#### **APPLICATIONS**

### Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to 1/60Hz using a 4,194,304Hz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.



The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.



### **Logic Family Compatibility**

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

#### **Oscillator Considerations**

The oscillator consists of a CMOS inverter and a feed-back resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

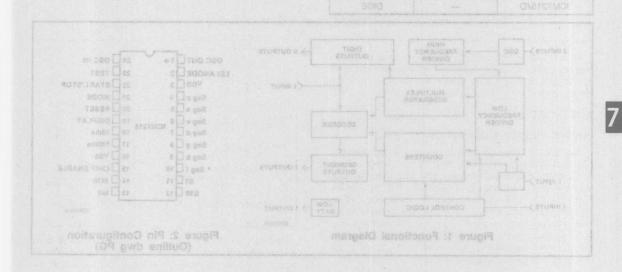
If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance  $\pm 10 \mathrm{ppm}$ , a low series resistance (less than 25 ohms), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor  $C_{\rm IN}$  should be 30pF and the oscillator tuning capacitor should range between approximately 16 and 60pF.

Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

#### **Control Inputs**

The TEST input inhibits the 2<sup>18</sup> output and applies the 2<sup>9</sup> output to the 2<sup>21</sup> divider, thereby permitting a speedup of the testing of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1 sec, or to change the state of OUT 4 from ON to OFF during INHIBIT.



# GENERAL DESCRIPTION

The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED. The only components required for a complete stopwatch are the display, three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an ON-OFF switch. For a two function stopwatch, or to add a display off feature, one additional slide switch is required. The circuit divides the oscillator frequency by 2<sup>15</sup> to obtain 100Hz, which is fed to the fractional seconds, seconds and minutes counters, while an intermediate frequency is used to obtain the 1/6 duty cycle 1.07kHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP only of these thy Islavio villaup rigid a to said

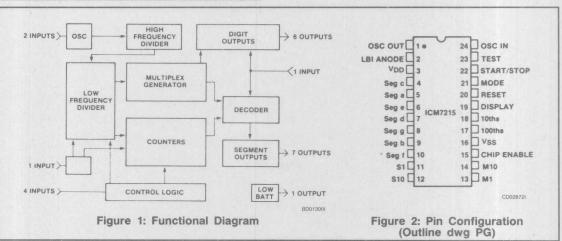
#### ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE 24-Pin PLASTIC DIP		
ICM7215IPG	-20°C to +70°C			
ICM7215/D		DICE		

### FEATURES

- Four Functions: Start/Stop/Reset, Split, Taylor,
  Time Out
- Six Digit Display: Ranges Up to 59 Minutes 59.99 Seconds
- High LED Drive Current: 13mA Peak Per Segment at 16.7% Duty Cycle With 4.0 Volt Supply
- Requires Only Three Low Cost SPST Switches Without Loss of Accuracy: Start/Stop, Reset, Display Unlock
- Chip Enable Pin Turns Off Both Segment and Digit Outputs; Can Be Used for Multiple Circuits Driving One Display
- Low Battery Indicator
- Digit Blanking On Seconds and Minutes
- Wide Operating Range: 2.0 to 5.0 Volts
- 1kHz Multiplex Rate Prevents Flickering Display
- Can Be Used Easily In Four Different Single Function Stopwatches or Two Two-Function Stopwatches: Start/Stop/Reset With Time-out, Split With Taylor. The Component Count for A Three- or Four-Function Stopwatch Will Be Slightly Greater
- Retrofit to ICM7205 for Split and/or Taylor Applications

with other logic families. These resistors must be connected



TYPICAL PERFORMANCE CHARACTERISTICS

#### **ABSOLUTE MAXIMUM RATINGS**

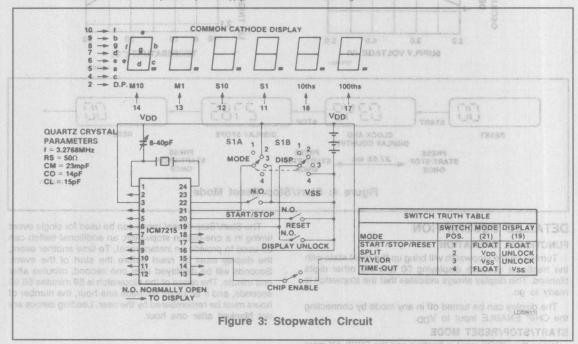
Supply Voltage (VDD to VSS)	Storage Temperature55°C to +125°C
Power Dissipation (Note 1)	Input VoltageVSS-0.3V to VDD+0.3V
Operating Temperature20°C to +70°C	Output VoltageVSS to VDD

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS:**  $(T_A = +25^{\circ}C, \text{ stopwatch circuit, } V_{DD} = 4.0V, V_{SS} = 0V, \text{ unless otherwise specified.)}$ 

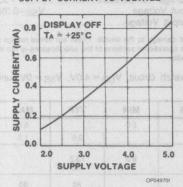
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VSUPPLY	Supply Voltage (VDD - VSS)	-20°C ≤ T <sub>A</sub> ≤ +70°C		2.0		5.0	V
IDD	Supply Current	Display off			0.6	1.5	mA
ISEG	Segment Current Peak Average	5 segments lit 1.8 Volts across display	8.0	9.0	13.2	2.0	
Switch Actuation Current  Switch Actuation Current	All inputs except CHIP ENABLE	úrso	eled.	20	50		
	Switch Actuation Current	Chip enable	STREET	THOU VICE	50	200	
IDLK	Digit Leakage Current	V <sub>DIG</sub> = 2.0V	1			50	μΑ
ISLK	Segment Leakage Current	V <sub>SEG</sub> = 2.0V	-	Marine James		100	
V <sub>LBI</sub>	Low Battery Indicator Trigger Voltage	T T	K	2.2	CA = +29° C	2.8	· V
ILBI	LBI Output Current	V <sub>DD</sub> = 2.0V, V <sub>LBI</sub> = 1.6V		1	2.0	78 19	mA
fSTAB	Oscillator Stability	$V_{DD} = 2.0V$ to $V_{DD} = 5.0V$	1		6	10 25	ppm
9m	Oscillator Transconductance	V <sub>DD</sub> = 2.0V	1	120		2 2	μs
Cosci	Oscillator Input Capacitance	10.3			30	1 25	pF

NOTE: 1. The output devices on the ICM7215 have very low impedence characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA.

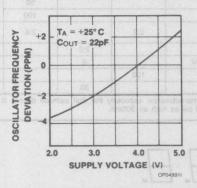


#### TYPICAL PERFORMANCE CHARACTERISTICS

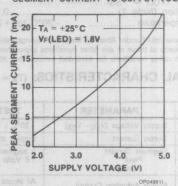
SUPPLY CURRENT VS VOLTAGE



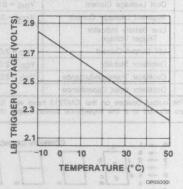
OSC. STABILITY VS SUPPLY VOLTAGE



SEGMENT CURRENT VS SUPPLY VOLTAGE



LOW BATTERY INDICATOR (LBI) TRIGGER VOLTAGE VS TEMPERATURE





### DETAILED DESCRIPTION

#### FUNCTIONAL OPERATION

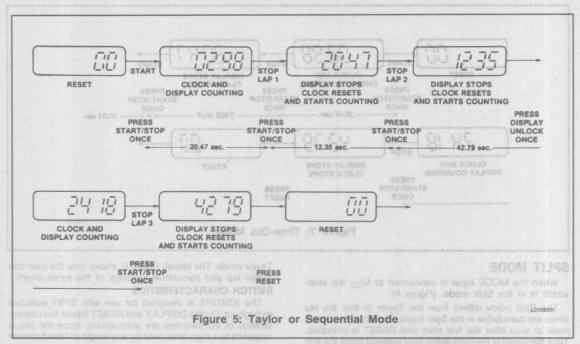
Turning on the stopwatch will bring up the reset state with the fractional seconds displaying 00 and the other digits blanked. This display always indicates that the stopwatch is ready to go.

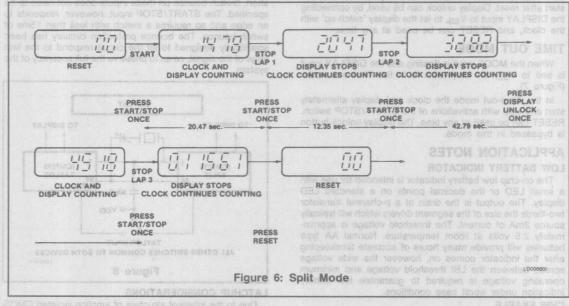
The display can be turned off in any mode by connecting the CHIP ENABLE input to  ${\rm V}_{\rm DD}.$ 

#### START/STOP/RESET MODE

When the MODE input is floating and the DISPLAY input is floating or connected to V<sub>DD</sub> the circuit is in the Start/Stop/Reset mode. (Figure 4).

The Start/Stop/Reset mode can be used for single event timing in a one-button stopwatch; an additional switch can be used to provide an instant reset. To time another event, the display must be reset before the start of the event. Seconds will be displayed after one second, minutes after one minute. The range of the stopwatch is 59 minutes 59.99 seconds, and if an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.



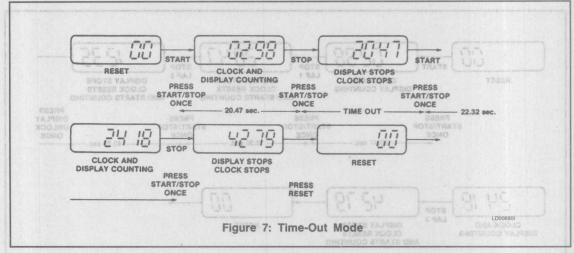


#### TAYLOR OR SEQUENTIAL MODE

When the MODE input is connected to V<sub>SS</sub>, the stopwatch is in the Taylor or Sequential mode. (Figure 5).

Each split time is measured from zero in the Taylor mode; i.e., after stopping the watch, the counters reset momentari-

ly and start counting the next interval. The time displayed is that elapsed since the last activation of START/STOP. The display is stationary after the first interval unless the display unlock is used, by connecting the DISPLAY input to VSS, to show the running clock. RESET can be used at any time.



#### SPLIT MODE

When the MODE input is connected to  $V_{\mbox{\scriptsize DD}}$  the stopwatch is in the Split mode. (Figure 6).

The Split mode differs from the Taylor in that the lap times are cumulative in the Split mode. The counters do not reset or stop after the first start until RESET is activated. Time displayed is the cumulative time elapsed since the first start after reset. Display unlock can be used, by connecting the DISPLAY input to VSS, to let the display 'catch up' with the clock, and RESET can be used at any time.

#### TIME OUT MODE

When the MODE input is floating and the DISPLAY input is tied to VSS, the stopwatch is in the Time-out mode. (Figure 7).

In the Time-out mode the clock and display alternately start and stop with activations of the START/STOP switch. RESET can be used at any time. The display unlock button is bypassed in this mode.

## APPLICATION NOTES LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers which will typically source 2mA of current. The threshold voltage is approximately 2.5 volts at room temperature. Normal AA type batteries will provide many hours of accurate timekeeping after the indicator comes on, however the wide voltage spread between the LBI threshold voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

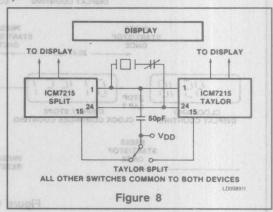
#### CHIP ENABLE

The CHIP ENABLE input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the CHIP ENABLE input is floating or connected to V<sub>SS</sub>, the display is enabled, and when the tied to V<sub>DD</sub> the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the

Taylor mode. The circuit, Figure 8, shows how the user can obtain lap and cumulative readings of the same event.

#### SWITCH CHARACTERISTICS

The ICM7215 is designed for use with SPST switches throughout. On the DISPLAY and RESET inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any length of time however short. Switch bounce on these inputs does not need to be specified. The START/STOP input, however, responds to an edge and so requires a switch with less than 15ms of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.



#### LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to the 7215. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

After deciding on a crystal and a nominal load capacitance, take the worst case values of  $C_{\text{in}}$ ,  $C_{\text{out}}$  and  $R_{\text{S}}$  and calculate the  $g_{\text{m}}$  required by:

$$g_{m} = \omega^{2} C_{in} C_{out} R_{S} \left[ 1 + \frac{c_{o} (C_{in} + C_{out})}{C_{in} C_{out}} \right]^{2}$$

Co = static capacitance and one of the common of the capacitance and one of the capacitance and the capacitance are capacitance are capacitance and the capacitance are ca

Rs = series resistance

Cin = input capacitance

Cout = output capacitance

 $\omega = 2\pi \times \text{crystal frequency}$  for allows it

The resulting  $g_{\text{m}}$  should be less than half the  $g_{\text{m}}$  specified for the device. If it is not, a lower value of crystal

 Decimal Point and Leading Zero Blanking May the Externally Selected

#### **OSCILLATOR TUNING**

Tuning can be accomplished by using the 10th or 100th seconds with the device reset. The frequency on the cathode should be tuned to 1066.667Hz, which is equivalent to a period of 937.5 microseconds. Note that a frequency counter cannot be connected directly to the oscillator because of possible loading.

#### large multiplexed UED displays. The counter inputs TRST

The TEST input is used for high speed testing of the device. When the input is pulsed low, a latch is set which speeds up counting by a factor of 32; each pulse on the TEST input rapidly advances both minutes and seconds in a parallel mode. To accurately rapid advance the signal applied to the TEST input must be free of switch bounce. The circuit is taken out of the test mode by using either RESET or START/STOP.

## REPLACING THE ICM7205 WITH THE ICM7215

The ICM7215 is designed to be compatible with circuits using the ICM7205. If the 7205 is used only in the Split mode no changes are required. If the 7205 is used in the Taylor mode and the Split-Taylor input (pin 21) is left open, a jumper from pin 21 to V<sub>SS</sub> must be added when converting to the 7215. A jumper may also be needed if the 7205 is used with a Split/Taylor switch. Once the jumper has been added the board can be used with either device.

All versions of the ICM7216 incorporate leading zero blanking, Frequency is displayed in kHz. In the ICM7216A and B. time is displayed in us. The display is multiplaxed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 26mA. The ICM7216B and D are designed for common cathode idisplay with typical peak segment currents of 12mA. In the display with typical peak segment divers are turned display of mode, both digit and segment divers are turned on a reading the display to be used for other functions.

#### ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	PART NUMBER
		CM7216A/D
	-20°C to +85°C	
	-20°C to +86°C	
28 pin PLASTIC DIP	-20°C to +85°C	
	-20°C to +85°C	
		ICM7216C/D
	0°88 + 61 0°08-	
		IOM/216DRPL
	-20°C to +85°C	ILIGATSVMOL

### ICM7216A/B/C/D 8-Digit Multi-Function Frequency Counter/Timer

#### GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Timer Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio ( $f_A/f_B$ ) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1  $\mu$ s resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in  $\mu$ s. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7216A/D	-20°C to +85°C	DICE
ICM7216AIJL	-20°C to +85°C	28 pin CERDIP
ICM7216B/D	-20°C to +85°C	DICE
ICM7216BIPI	-20°C to +85°C	28 pin PLASTIC DIP
ICM7216BIJL	-20°C to +85°C	28 pin CERDIP
ICM7216C/D	-20°C to +85°C	DICE
ICM7216CIJL	-20°C to +85°C	28 pin CERDIP
ICM7216D/D	-20°C to +85°C	DICE
ICM7216DIPI	-20°C to +85°C	28 pin PLASTIC DIP
ICM7216DIJL	-20°C to +85°C	28 pin CERDIP



#### FEATURES beinglach at tiumin ent bire -

#### ALL VERSIONS:

- Functions as a Frequency Counter (DC to 10MHz)
- Four Internal Gate Times: 0.01 Sec, 0.1 Sec, 1 Sec, 10 Sec in Frequency Counter Mode
- Directly Drives Digits and Segments of Large Multiplexed LED Displays (Common Anode and Common Cathode Versions)
- Single Nominal 5V Supply Required
- Highly Stable Oscillator, Uses 1MHz or 10MHz
  Crystal
- Internally Generated Decimal Points, Interdigit Blanking, Leading Zero Blanking and Overflow Indication
- Display Off Mode Turns Off Display and Puts Chip Into Low Power Mode
- Hold and Reset Inputs for Additional Flexibility ICM7216A AND ICM7216B
- Functions Also as a Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter
- 1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes
- Measures Period From 0.5μs to 10s ICM7216C AND ICM7216D
- Decimal Point and Leading Zero Blanking May Be Externally Selected



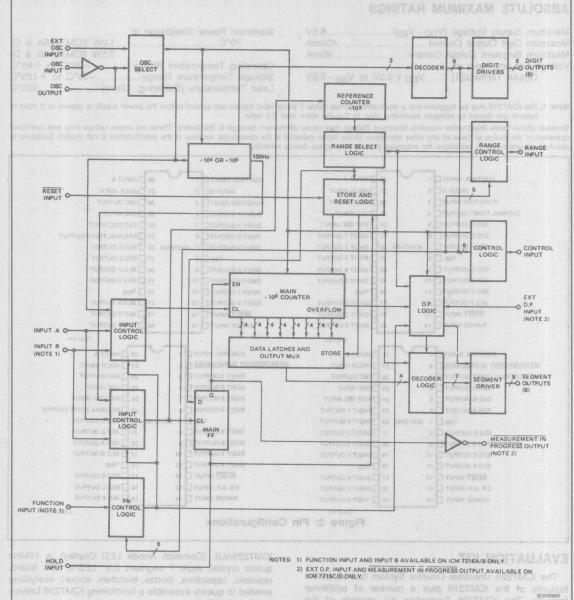
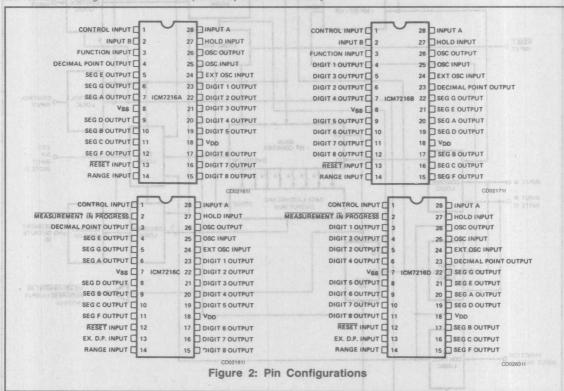


Figure 1: Functional Diagram

ıvıaxımımı suppiy voitage (VDD - VSS)6.5V	Maximum Power Dissipation at
Maximum Digit Output Current400mA	70°C1.0W (ICM7216A & C)
Maximum Segment Output Current60mA	0.5W (ICM7216B & D)
Voltage On Any Input or	Operating Temperature Range20°C to +85°C
Output Terminal[1]V <sub>DD</sub> + 0.3V to V <sub>SS</sub> - 0.3V	Storage Temperature Range55°C to +125°C
	Lead Temperature (Soldering, 10sec)300°C

Note: 1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V<sub>DD</sub> to V<sub>SS</sub> by more than 0.3 volts.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



#### **EVALUATION KIT**

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the

ICM7226AIJL (Common Anode LED Display), a 10MHz quartz crystal, eight 7 segment 0.3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

## ICM7216A/B/C/D

## ELECTRICAL CHARACTERISTICS (ICM7216A/B) SYMON SOTTERSTOARAND JACKTOBLE

(VDD = 5.0V ±5%, VSS = 0, TA = 25°C, unless otherwise specified.)

SYMBOL	NAM PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	JOUNIT
	ICM7216A/B				TOMESE	
I <sub>DD</sub> Am	Operating Supply Current	Display Off, Unused Inputs to VSS	misne	2	5	mA
VSUPPLY	Supply Voltage Range (VDD - VSS)	-20°C < T <sub>A</sub> < +85°C, INPUT A, INPUT B Frequency at f <sub>max</sub>	4.75	mP egeth	6.0	y manie v
fA(max)	Maximum Frequency INPUT A, Pin 28	-20°C < T <sub>A</sub> < +85°C 4,75 < V <sub>DD</sub> ≤ 6.0V, Figure 3, Function = Frequency, Ratio, Unit		Fraqueno Pin 28	Maxim-om	(campl)
	07	Counter Function = Period, Time Interval	10 2.5	Casc Fra Light	Maxemuss Osc. Pred	MHz MHz
fB(max)	Maximum Frequency INPUT B, Pin 2	-20°C < T <sub>A</sub> < +85°C 4.75 < V <sub>DD</sub> ≤ 6.0V, Figure 4	2.5	oaQ he ocueneri	Minimum deciliator	MHz
am	Minimum Separation INPUT A to INPUT B Time Interval Function	$-20^{\circ}\text{C} < \text{T}_{\text{A}} < +85^{\circ}\text{C}$ $4.75 < \text{V}_{\text{DD}} \le 6.0\text{V},$ Figure 5	250	selvi cisav	self emili	ns
fosc	Maximum Osc. Freq. and Ext. Osc. Frequency	-20°C < T <sub>A</sub> < +85°C 4.75 < V <sub>DD</sub> ≤ 6.0V	10	SpidleV w	ST BIRS	MHz
fosc	Minimum Ext. Osc. Freq.		The state of the s	at mounts	100	kHz
9m May	Oscillator Transconductance	V <sub>DD</sub> = 4.75V, T <sub>A</sub> = +85°C	2000		Pins 12	μs
f <sub>mux</sub>	Multiplex Frequency	f <sub>osc</sub> = 10MHz		500	legal bags	Hz
- PA	Time Between Measurements	f <sub>osc</sub> = 10MHz		200	1 Pin 22,	ms
Aq	Input Voltages: Pins 2,13,25,27,28 Input Low Voltage	-20°C < T <sub>A</sub> < +85°C = 40V		STIBQUI	1.0	V 80
VINL VINH	Input High Voltage	Supplies Well Sypassed	3.5		I Input Rate	V
RIN	Input Resistance to V <sub>DD</sub> Pins 13,24	V <sub>IN</sub> = V <sub>DD</sub> - 1.0V	100	400	1081721	kΩ
lilk	Input Leakage Pin 27,28,2		0.81,22,23	16,17,19,2	20	μΑ
dV <sub>IN</sub> /dt	Input Range of Change	Supplies Well Bypassed	in	15	DO MARK	mV/μs
	ICM7216A			200000	BANKSAR	
loh lot	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	V <sub>OUT</sub> = V <sub>DD</sub> - 2.0V V <sub>OUT</sub> = V <sub>SS</sub> + 1.0V	-140	-180 +0.3	Pins S,4 Low Out High Out Multiples	mA HO
lor North	SEGment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	Vout = Vss + 1.5V Vout = Vpp - 2.5V	20 28V 0	35 -100	Pins I, I ligate Lo Input Ho Input Ro	mA μA
VINL VINH RIN	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to VSS	V <sub>IN</sub> = V <sub>SS</sub> + 1.0V + = 140	2.0	100	0.8	ν ν kΩ
	ICM7216B			100	10 mg/m	
IOL AS	Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	V <sub>OUT</sub> = V <sub>SS</sub> + 1.3V V <sub>OUT</sub> = V <sub>DD</sub> - 2.5V	50		High Oal	mA
IOH ISLK	SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Cutput Current Leakage Current	V <sub>OUT</sub> = V <sub>DD</sub> - 2.0V V <sub>OUT</sub> = V <sub>DD</sub> - 2.5V	-10	3,14 w Voltage sh Voltage	pJ hight	mA A
VINL VINH RIN	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V <sub>DD</sub>	$V_{\text{IN}} = V_{\text{DD}} - 2.5V$	V <sub>DD</sub> - 0.8	360	V <sub>DD</sub> - 2.0	ν ν kΩ

### ICM7216A/B/C/D

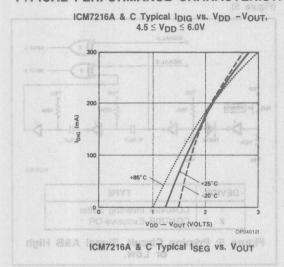


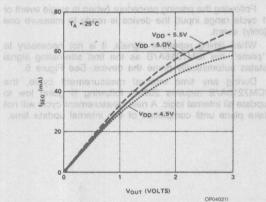
## ELECTRICAL CHARACTERISTICS (ICM7216C/D) STMOD CONTRIBUTOARAHO JACKATOSJE

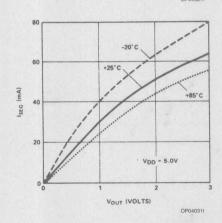
 $(V_{DD} = 5.0V \pm 5\%, V_{SS} = 0, T_A = 25$ °C, unless otherwise specified.)

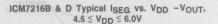
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ICM7216C/D			S\A	1CM721	
IDD	Operating Supply Current	Display Off, Unused Inputs to VSS	Inamo	123	5.40	mA
VSUPPLY	Supply Voltage Range (VDD - VSS)	-20°C < T <sub>A</sub> < +85°C, INPUT A Frequency at f <sub>max</sub>	4.75	telft Rotel	6.0	V. Vada
f <sub>A(max)</sub>	Maximum Frequency INPUT A, Pin 28	-20°C < T <sub>A</sub> < +85°C 4.75 < V <sub>DD</sub> < 6.0V, Figure 3	10	Frequenci Plo, 28	Maximum A TUPINI	MHz
fosc and	Maximum Osc. Freq. and Ext. Osc. Frequency	-20°C < T <sub>A</sub> < +85°C 4.75 < V <sub>DD</sub> < 6.0V	10			MHz
fosc	Minimum Ext. Osc. Freq.	2/88+ > AT > D*08-		anduper3	100	kHz
9m	Oscillator Transconductance	$V_{DD} = 4.75V, T_A = +85^{\circ}C$	2000	Pin 2	BITURIA	μs
f <sub>mux</sub>	Multiplex Frequency	f <sub>osc</sub> = 10MHz		500		Hz
	Time Between Measurements	f <sub>osc</sub> = 10MHz		200	A STREET	ms
VINL VINH	Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage	-20°C < T <sub>A</sub> < +85°C	3.5	oval Fue Oso Fre uency	1.0	V
RIN	Input Resistance to V <sub>DD</sub> Pins 12,24	V <sub>IN</sub> = V <sub>DD</sub> - 1.0V	100	400	ramilioaO	kΩ
SH .	Input Leakage Pin 27, Pin 28	1000 = 10001		consupari	Xetallick/	
ILK	Output Current	N - 10XIIIS	0.00	seM care	20	μΑ
OL		V <sub>OL</sub> = +.4V	0.36	28306	InV tuos	mA
ЮН	Pin 2	V <sub>OH</sub> = V <sub>DD</sub> - 0.8V	265	positio's vi	1,3 6 14 1	μΑ
dV <sub>IN</sub> /dt	Input Rate of Change	Supplies Well Bypassed		15	M sugni	mV/μs
O.A	ICM7216C	V0.1 - G0V = MV	604	DE SEUTHERS	Pas 10	
I <sub>OH</sub> V <sub>III</sub>	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	V <sub>OUT</sub> = V <sub>DD</sub> - 2.0V V <sub>OUT</sub> = V <sub>SS</sub> + 1.0V	-140	-180 0.3	Physical Car Physical Par Chout Rat	mA mA
loL loh	SEGment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	V <sub>OUT</sub> = V <sub>SS</sub> + 1.5V V <sub>OUT</sub> = V <sub>DD</sub> - 2.5V	20	30 -100	1CN/F21E Digit (John Pins 16 Junto Or	mA μA
VINL VINH RIN	Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to VSS	V <sub>IN</sub> = +1.0V	2.0		0.8	ν ν κΩ
	ICM7216D			atugni	nel@ifu.ivi	
lor loh	Digit Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	V <sub>OUT</sub> = +1.3V V <sub>OUT</sub> = V <sub>DD</sub> - 2.5V	50	75 100		mΑ μΑ
loh Islk	SEGment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	V <sub>OUT</sub> = V <sub>DD</sub> - 2.0V V <sub>OUT</sub> = V <sub>DD</sub> - 2.5V	10	15	mQ 200	mA μA
VINL VINH	Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V <sub>DD</sub>	V <sub>IN</sub> = V <sub>DD</sub> – 1.0V	V <sub>DD</sub> - 0.8	fput Quini Driverni 18,17,193	V <sub>DD</sub> – 2.0	ν ν κΩ

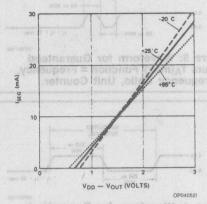
#### TYPICAL PERFORMANCE CHARACTERISTICS



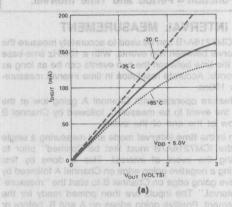


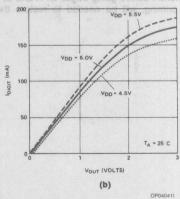


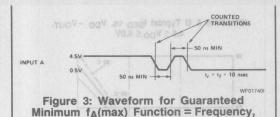


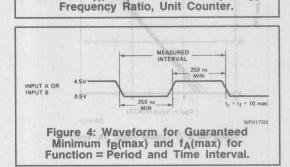


#### ICM7216B & D Typical IDIGIT vs. VOUT







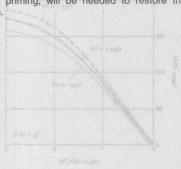


#### TIME INTERVAL MEASUREMENT

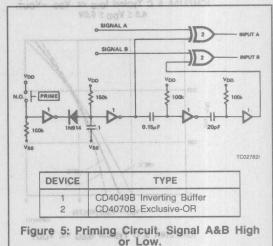
The ICM7216A/B can be used to accurately measure the time interval between two events. With a 10MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7216A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.



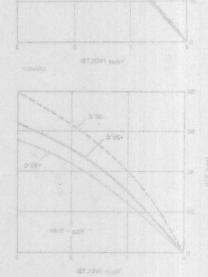
(Figure 5).

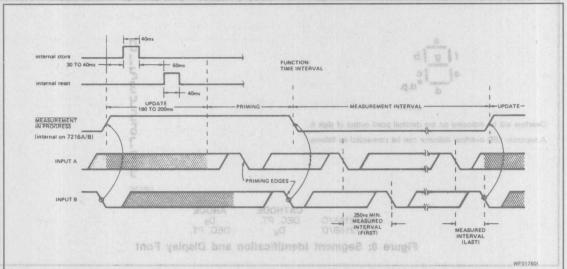


Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A/B as the first alternating signal states automatically prime the device. See Figure 5.

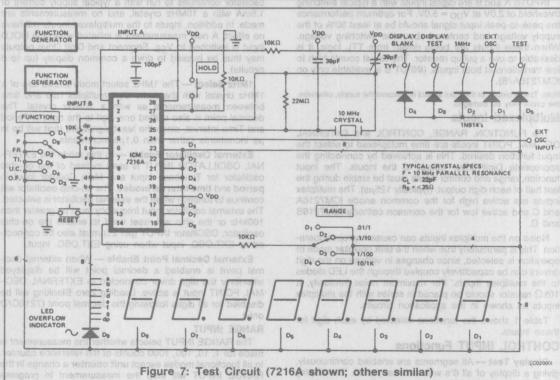
During any time interval measurement cycle, the ICM7216A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

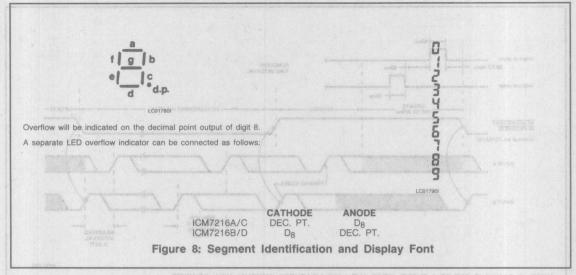




NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

Figure 6: Waveforms for Time Interval Measurement (Others are similar, but without priming phase).





## DETAILED DESCRIPTION INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at  $V_{DD}=5.0$ V. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A/B).

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

#### **Multiplexed Inputs**

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125µs). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a  $10 \mathrm{k}\Omega$  resistor should be placed in series with the multiplex inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

#### **CONTROL INPUT Functions**

**Display Test** — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Blank Display is selected at the same time.

Display Off — To disable the drivers, it is necessary to tie  $\rm D_4$  to the CONTROL INPUT and have the HOLD input at

V<sub>DD</sub>. The chip will remain in this "Display Off" mode until HOLD is switched back to V<sub>SS</sub>. While in the "Display Off" mode, the segment and digit driver outputs are open, the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal, and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V<sub>SS</sub>. Segment and Digit Drive outputs may thus be bussed to drive a common display (up to 6 circuits).

1MHz Select — The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in  $\mu$ s increments rather than 0.1 $\mu$ s increments.

External Oscillator Enable — In this mode the EXTERNAL OSCILLATOR INPUT is used instead of the on-chip oscillator for Timebase input and Main Counter input in period and time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself to enable the on-chip oscillator. OSCillator INPUT (pin 25) must also be connected to EXT.OSC. input when using EXT.OSC. input.

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to EXTERNAL DECIMAL POINT input is active. Leading Zero Blanking will be disabled for all digits following the decimal point (7216C/D only).

#### RANGE INPUT

The RANGE INPUT selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except **unit counter** a change in the RANGE INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

## ICM7216A/B/C/D

Table 1: Multiplexed Input Functions

	FUNCTION	DIGIT
FUNCTION INPUT Pin 3 (ICM7216A & B Only)	Frequency Period Frequency Ratio	D <sub>1</sub> D <sub>8</sub> D <sub>2</sub>
	Time Interval Unit Counter Oscillator Frequency	D <sub>5</sub> D <sub>4</sub> D <sub>3</sub>
RANGE INPUT Pin 14	.01 sec/1 Cycle .1 sec/10 Cycles 1 sec/100 Cycles 10 sec/1K Cycles	D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub>
CONTROL INPUT Pin 1	Blank Display Display Test 1 MHz Select External Oscillator Enable External Decimal	D <sub>4</sub> and Hold D <sub>8</sub> D <sub>2</sub> D <sub>1</sub>
EXT. D.P. INPUT Pin 13, ICM7216C & D Only		t for same

#### **FUNCTION INPUT**

The six functions that can be selected are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency. This input is available on the ICM7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the Reference Counter, as shown in Table 2. In all cases, only 1→0 transitions are counted or timed. In time Interval, a flip-flop is toggled first by a 1→0 transition of INPUT A and then by a 1→0 transition of INPUT B. The oscillator is gated into the Main Counter from the time INPUT A toggles the flip-flop until INPUT B toggles it. In unit counter mode, the main counter contents are continuously displayed. A change in the FUNCTION INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed.

Table 2: 7216A/B Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE
Frequency (f <sub>A</sub> )	Input A SUD 10	100 Hz (Oscillator ÷10 <sup>5</sup> or 10 <sup>4</sup> )
Period (t <sub>A</sub> )	Oscillator	Input A
Ratio (f <sub>A</sub> /f <sub>B</sub> )	Input A	Input B
Time Interval (A → B)	Osc•(Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (fosc)	Oscillator	100 Hz (Oscillator ÷ 10 <sup>5</sup> or 10 <sup>4</sup> )

#### **EXTernal DECimal Point INput**

When the **external decimal point** is selected this input is active. Any of the digits, except  $D_8$ , can be connected to this point.  $D_8$  should not be used since it will override the overflow output and leading zeros will remain unblanked

after the decimal point. This input is available on the ICM7216C and D only.

HOLD Input — Except in the unit counter mode, when the HOLD Input is at V<sub>DD</sub>, any measurement in progress (before STORE goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In unit counter mode when HOLD input is at V<sub>DD</sub>, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

RESET Input — The RESET input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

#### **DISPLAY CONSIDERATIONS**

The display is multiplexed at a 500Hz rate with a digit time of 244  $\mu$ s. An interdigit blanking time of 6  $\mu$ s is used to prevent ghosting between digits. The decimal point and leading zero blanking assume right hand decimal point displays, and zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows. Overflow is indicated by the decimal point on digit 7 turning on.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with  $V_F=1.8V$  at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with  $V_F=1.8V$  at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. The Typical Performance Characteristics curves show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays,  $V_{DD}$  may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

#### **ACCURACY**

In a Universal Counter crystal drift and quantization effects cause errors. In **frequency**, **period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 9, the least accuracy will be obtained at 10kHz. In **time interval** 

### ICM7216A/B/C/D

measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 10. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 11.

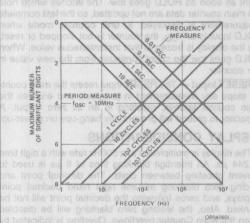


Figure 9: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common caffode displays a peak current of 15mA/segment using displays with Vr = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays. If required, The Typical Performance Characteristics curves show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, Vpp may

be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

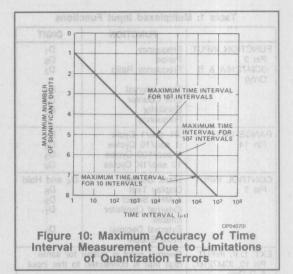
The segment and digit outputs in ICM7218's are not

directly compatible with either TR or CMOS logic when deving LEDs. Therefore, level stiffling with discrete transisters may be required to use these outputs as logic signals.

In a Universal Counter crystal doft and quantization offects cause errors in frequency, period and time interval modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter Thorefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/\*C will

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by dispisying more digits. In the frequency mode the maximum accuracy is obtained with right requency is obtained in partical mode maximum accuracy is obtained with tow frequency inputs. As can be seen in Figure 8, the seen to service will be obtained at 10km/s. In time statement





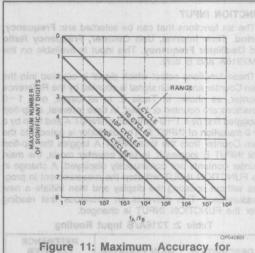
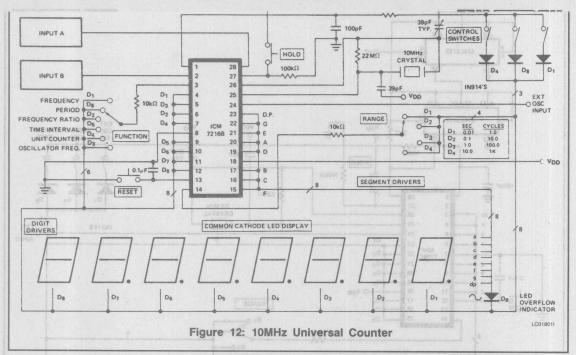


Figure 11: Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

	Unit Counter (Count A)
100 Hz (Oscillator + 10 <sup>5</sup> or 10 <sup>5</sup> )	

When the external decimal point is selectively. Any of the digits, except DB, can be used the control of the co

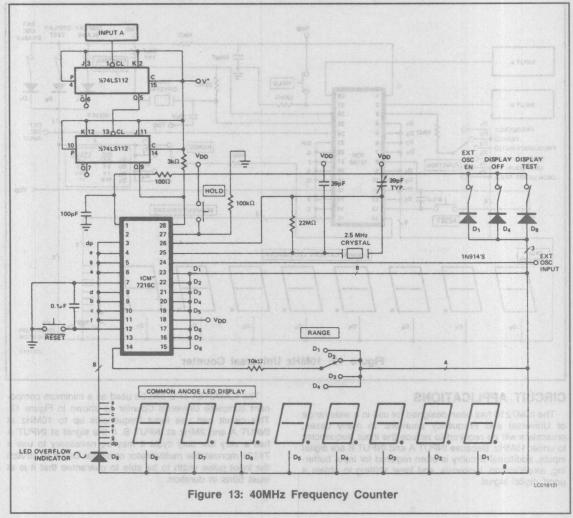


#### CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

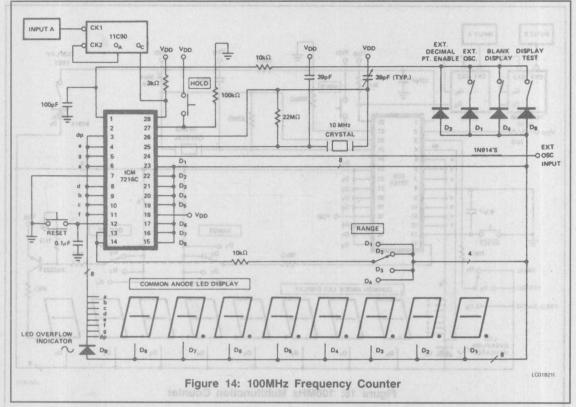
The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 12. This circuit can use input frequencies up to 10MHz at INPUT A and 2MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ns in duration.

7



To measure frequencies up to 40MHz the circuit of Figure 13 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well

as the input frequency. In doing this the time between measurements is also lengthened to 800ms and the display multiplex rate is decreased to 125Hz.



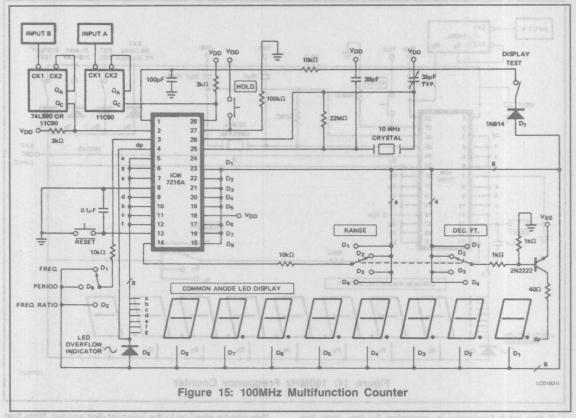
If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1MHz, but the decimal point must be moved one digit to the right. Figure 14 shows a frequency counter with a  $\div 10$  prescaler and an ICM7216C. Since there is no external decimal point control with the ICM7216A/B, the decimal point may be controlled externally with additional drivers as shown in Figure 15. Alternatively, if separate anodes are available for the decimal points,

they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 16 additional logic has been added to count the input directly in period mode for maximum accuracy. In Figures 14 through 16, INPUT A comes from  $Q_{\rm C}$  of the prescaler rather than  $Q_{\rm D}$  to obtain an input duty cycle of 40%.

7

the TOMP's mode and town in the TWHA mode.

The crystal and estillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or IMPUT can ocure



#### OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of  $10M\Omega$  to  $22M\Omega$  should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required gm can be calculated as follows:

$$g_{m} = \omega^{2} C_{in} C_{out} Rs \left(1 + \frac{C_{O}}{C_{L}}\right)^{2}$$

where 
$$C_L = \left(\frac{C_{in}C_{out}}{C_{in} + C_{out}}\right)$$

CO = Crystal Static Capacitance

Rs = Crystal Series Resistance

Cin = Input Capacitance

Cout = Output Capacitance

 $\omega = 2\pi f$ 

The required gm should not exceed 50% of the gm specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to Cin and Cout. For maximum stability of frequency, Cin and Cout should be approximately twice the specified crystal static capacitance.

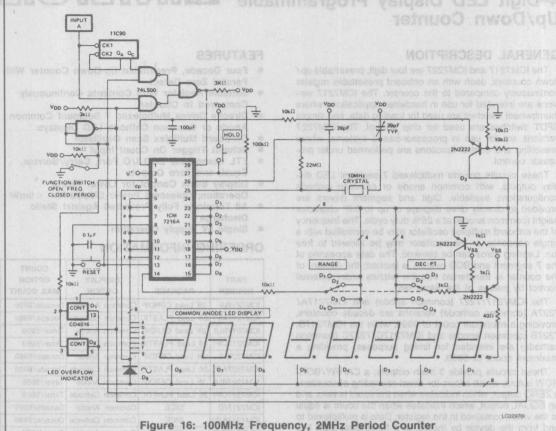
In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10MHz or 1MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate

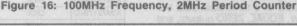
isf<sub>mux</sub> = 
$$\frac{f_{osc}}{2 \times 10^4}$$
 for 10MHz mode and  $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$  for the  $\frac{f_{osc}}{2 \times 10^6}$ 

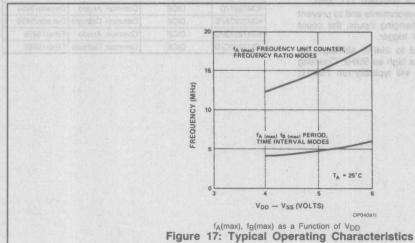
1MHz mode. The time between measurements is

the 10MHz mode and  $\frac{2 \times 10^5}{f_{osc}}$  in the 1MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.







# ICM7217/ICM7227 4-Digit LED Display Programmable Up/Down Counter



#### **GENERAL DESCRIPTION**

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

These circuits provide 3 main outputs; a CARRY/BOR-ROW output, which allows for direct cascading of counters, a ZERO output, which indicates when the count is zero, and an EQUAL output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, EQUAL, ZERO outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

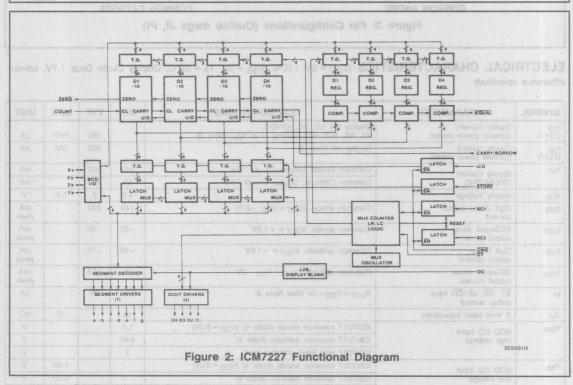
Input frequency is guaranteed to 2MHz, although the device will typically run with fin as high as 5MHz. Counting and comparing (EQUAL output) will typically run 750kHz maximum.

#### **FEATURES**

- Four Decade, Presettable Up-Down Counter With Parallel Zero Detect
- Settable Register With Contents Continuously Compared to Counter
- Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays
- On-Board Multiplex Scan Oscillator
- Schmitt Trigger On Count Input
- TTL Compatible BCD i/O Port, Carry/Borrow, Equal, and Zero Outputs
- Display Blank Control for Lower Power Operation; Quiescent Power Dissipation < 5mW</li>
- All Terminals Fully Protected Against Static Discharge
- Single 5V Supply Operation

#### ORDERING INFORMATION

PART NUMBER	DISPLAY OPTION		COUNT OPTION MAX COUNT	
ICM7217IJI	28 Lead CERDIP	Common Anode	Decade/9999	
ICM7217AIPI	28 Lead PLASTIC	Common Cathode	Decade/9999	
ICM7217BIJI	28 Lead CERDIP	Common Anode	Timer/5959	
ICM7217CIPI	28 Lead PLASTIC	Common Cathode	Timer/5959	
ICM7227IJI	28 Lead CERDIP	Common Anode	Decade/9999	
ICM7227AIPI	28 Lead PLASTIC	Common Cathode	Decade/9999	
ICM7227BIJI	28 Lead CERDIP	Common Anode	Timer/5959	
ICM7227CIPI	28 Lead PLASTIC	Common Cathode	Timer/5959	
ICM7217/D	DICE	Common Anode	Decade/9999	
ICM7217A/D	DICE	Common Cathode	Decade/9999	
ICM7217B/D	DICE	Common Anode	Timer/5959	
ICM7217C/D	DICE	Common Cathode	Timer/5959	
ICM7227/D	DICE	Common Anode	Decade/9999	
ICM7227A/D	DICE	Common Cathode	Decade/9999	
ICM7227B/D	DICE	Common Anode	Timer/5959	
ICM7227C/D	DICE	Common Cathode	Timer/5959	



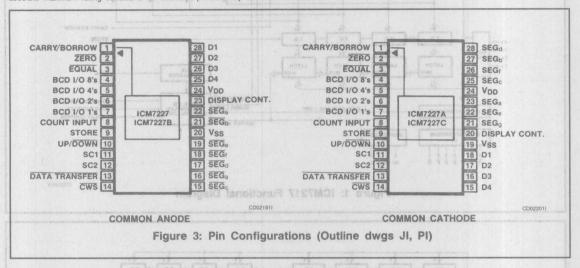
## ICM7217/ICM7227



#### **ABSOLUTE MAXIMUM RATINGS**

Power Dissipation (common cathode/Plastic) 0.5W
Note 1
Operating Temperature Range25°C to +85°C
Storage Temperature Range55°C to +125°C Lead Temperature (Soldering, 10sec)300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.



**ELECTRICAL CHARACTERISTICS** ( $V_{DD} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_A = 25$ °C, Display Diode Drop 1.7V, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DD</sub> (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V <sub>DD</sub> (Note 3)	4	350	500	μΑ
I <sub>DD</sub> (7227)	Supply current (Lowest power mode)	Display off (Note 3)	1	300	500	μΑ
IOP	Supply Current	Common Anode, Display On, all "8's"	140	200		mA
	OPERATING	Common Cathode, Display On, all "8's"	50	100		mA
V <sub>DD</sub>	Supply Voltage	TOTAL PARTY SAN SAN SAN SAN SAN SAN SAN SAN SAN SAN	4.5	- 5	5.5	V
lDIG	Digit Driver output	Common anode, V <sub>OUT</sub> = V <sub>DD</sub> -2.0V	140	200		mA peak
ISEG	SEGment driver output current	Common anode, V <sub>OUT</sub> = +1.5V	-20	-35		mA peak
IDIG	Digit Driver output current	Common cathode, V <sub>OUT</sub> = +1.0V	-50	-75		mA peak
ISEG	SEGment driver output current	Common cathode V <sub>OUT</sub> = V <sub>DD</sub> -2V	9	12.5		mA peak
lp .	ST, RS, UP/DN input pullup current	V <sub>OUT</sub> = V <sub>DD</sub> -2V (See Note 3)	5	25		μΑ
ZIN	3 level input impedance		40		75	kΩ
V <sub>BIH</sub>	BCD I/O input	ICM7217 common anode (Note 4) (V <sub>DD</sub> = 5.0V)	1.5			V
	high voltage	ICM7217 common cathode (Note 4)	4.40	Treasure.		V
	70-E	ICM7227 with 50pF effective load	3			V
V <sub>BIL</sub>	BCD I/O input	ICM7217 common anode (Note 4) (VDD = 5.0V)			0.60	V
With the second second	low voltage	ICM7217 common cathode (Note 4)	and the second		3.2V	V
		ICM7227 with 50pF effective load		ENATE:	1.5	V

#### ELECTRICAL CHARACTERISTICS (CONT.) 8017819313A9ANO 30MAM909839 JASI9YI

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IBPU /	BCD I/O input pullup current	iCM7217 common cathode V <sub>IN</sub> = V <sub>DD</sub> -2V (Note 3)	5	25	TESTAS:	μΑ
IBPD	BCD I/O input pulldown current	ICM7217 common anode V <sub>IN</sub> = +2V (Note 3)	5	25	287227B	μА
Voн	BCD I/O, ZERO, EQUAL Outputs output high current	ΙΟΗ = 100μΑ	3.5			V
Vol	BCD I/O, CARRY/BORROW ZERO, EQUAL Outputs output low current	I <sub>OL</sub> = -1.6mA			0.4	٧
fin	Count input frequency (Guaranteed)	$V_{DD} = 5V \pm 10\%, -20^{\circ}C < T_{A} < +70^{\circ}C$	0	5	2	MHz
VTH VO	Count input threshold	V <sub>DD</sub> = 5V (Note 5)	1 48 +	2		V
VHYS	Count input hysteresis	V <sub>DD</sub> = 5V (Note 5)	1007	0.5		V
VCIL	Count input LO	V <sub>DD</sub> = 5V	0.40	T.		V
VCIH	Count Input HI	V <sub>DD</sub> = 5V	(87,101):	uova	3.5	V
fds	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)	.V .ev	oral to	10	kHz
TA	Operating Temperature Range	Industrial temperature range	-25	4.5V ≤	+85	°C

- NOTES: 1. These limits refer to the package and will not be obtained during normal operation.
  2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V<sub>DD</sub> or less than V<sub>SS</sub> may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned
  - on first.

    In the ICM7217 the UP/DOWN, STORE, RESET and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 µA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.

    These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.

    Parameters not tested (Guaranteed by Design).

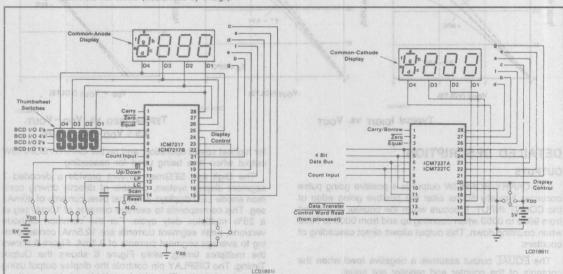
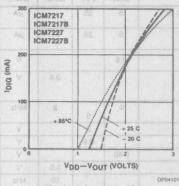


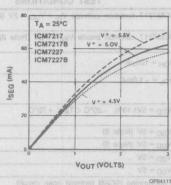
Figure 4: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

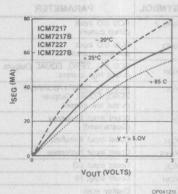
### ICM7217/ICM7227

**WINTERSIL** 

TYPICAL PERFORMANCE CHARACTERISTICS (TWOO) EDITERISTOARAHO LAGIRTOALA (DIGIT AND SEGMENT DRIVERS)

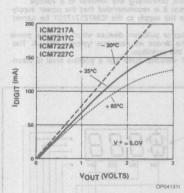


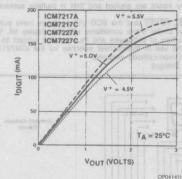


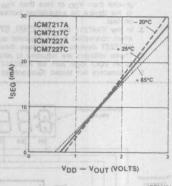


Typical I<sub>DIG</sub> vs. V  $_{+}$  -V<sub>OUT</sub>, 4.5V  $\leq$  V  $_{-}^{+}$   $\leq$  6.0V

Typical ISEG vs. Vout







Typical IDIGIT vs. VOUT

Typical I<sub>SEG</sub> vs.  $V_{DD} - V_{OUT}$ , 4.5  $\leq V_{DD} - V_{SS} \leq 6.0V$ 

### DETAILED DESCRIPTION

#### **OUTPUTS**

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

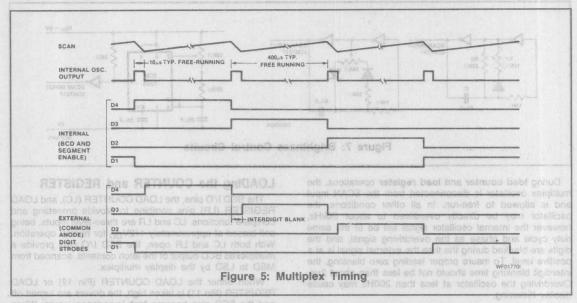
The EQUAL output assumes a negative level when the contents of the counter and register are equal.

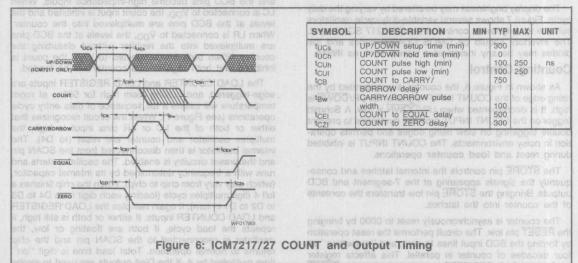
The ZERO output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW,  $\overline{\text{EQUAL}}$  and  $\overline{\text{ZERO}}$  outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA @ 0.4V (on resistance 250 $\Omega$ ), and for a logic one, the outputs will source  $> 60 \mu \text{A}$ . A  $10 \text{k}\Omega$  pull-up resistor to  $V_{DD}$  on the  $\overline{\text{EQUAL}}$  or  $\overline{\text{ZERO}}$  outputs is recommended

for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/ seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 5 shows the multiplex timing, while Figure 6 shows the Output Timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (VDD); this corresponds to normal operation. When this pin is connected to VDD, the segments are inhibited, and when connected to VSS, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 4.





#### Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for ICM7217 versions) are shown in Table 1 power consumption. In this display off condition, the wolled

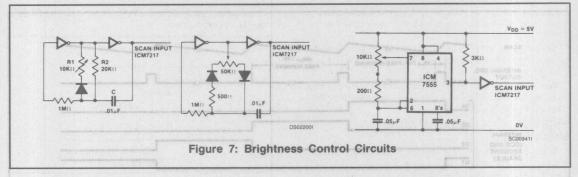
The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplexed Rate Control

SCAN CAPACITOR	NOMINAL OSCILLATOR FREQUENCY	DIGIT REPETITION RATE	SCAN CYCLE TIME (4 digits)
None Pr	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms or br

### ICM7217/ICM7227

## **WINTERSIL**



During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2µs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 7 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

#### **Counting Control**

As shown in Figure 6, the counter is incremented by the rising edge of the COUNT INPUT signal when  $UP/\overline{DOWN}$  is high. It is decremented when  $UP/\overline{DOWN}$  is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The STORE pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the STORE pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the RESET pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the RESET input is low, the register will also be set to zero. The STORE, RESET and UP/DOWN pins are provided with pullup resistors of approximately 75k $\Omega$ .

#### BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines as inputs.

#### LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately  $1/2V_{DD}$  for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to  $V_{DD}$ , the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to  $V_{DD}$ , the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to  $V_{DD}$ , the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 7). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 8). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, EQUAL, ZERO, UP/DOWN, RESET and STORE functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input

tions.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

## Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Figure 8. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid-loading problems.

#### **Output and Input Restrictions**

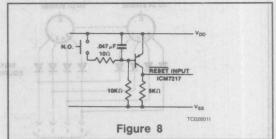
The CARRY/BORROW output is not valid during load counter and reset operations.

The EQUAL output is not valid during load counter or load register operations.

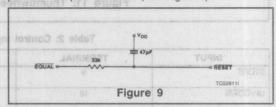
The ZERO output is not valid during a load counter operation.

The RESET input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500 µs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the RESET input can cause trouble. A simple circuit which provides a

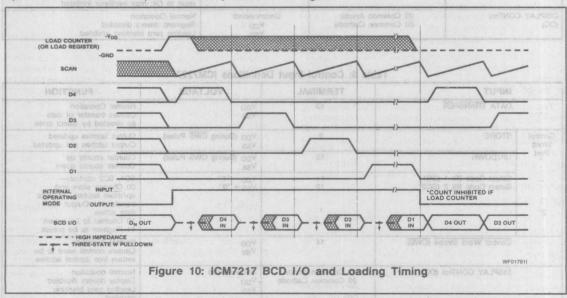
input is snown below.



When using the circuit as a programmable divider ( $\div$  by n with equal outputs) a short time delay (about 1 $\mu$ s) is needed from the  $\overline{\text{EQUAL}}$  output to the  $\overline{\text{RESET}}$  input to establish a pulse of adequate duration. (See Figure 9)

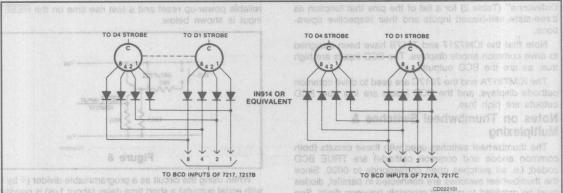


When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching EQUAL), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. RESET will not clear the register.



### ICM7217/ICM7227





Note: If the BCD pins are to be used for outputs a  $10k\Omega$  resistor should be placed in series with each digit line to avoid loading problems through the switches.

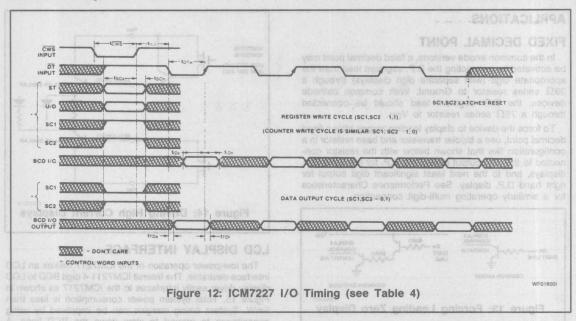
Figure 11: Thumbwheel Switch/Diode Connections

Table 2: Control Input Definitions ICM7217

INPUT	TERMINAL	VOLTAGE	The formal function FUNCTION PARAD and
STORE	9	V <sub>DD</sub> (or floating) V <sub>SS</sub>	Output latches not updated Output latches updated
UP/DOWN @	93001 10	V <sub>DD</sub> (or floating) V <sub>SS</sub>	Counter counts up Counter counts down
	When the orthit is configure	V <sub>DD</sub> (or floating) V <sub>SS</sub>	Normal Operation Counter Reset
I/O OFF	200AE), toadin stime will be di our. It tink hoad time is longer th	Unconnected VDD VSS	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
	rt the register, the register nee new value is to be entered, agister.	Unconnected VDD VSS	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V <sub>DD</sub> V <sub>SS</sub>	Normal Operation Segment drivers disabled Leading zero blanking inhibited

Table 3: Control Input Definitions ICM7227

	INPUT	TERMINAL	VOLTAGE	FUNCTION
	DATA TRANSFER	- 13	V <sub>DD</sub> V <sub>SS</sub>	Normal Operation Causes transfer of data as directed by select code
Control Word	STORE	9	V <sub>DD</sub> (During CWS Pulse)	Output latches updated Output latches not updated
Port	UP/DOWN	10	V <sub>DD</sub> (During CWS Pulse) V <sub>SS</sub>	Counter counts up Counter counts down
2"	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V <sub>DD</sub> = ''4'' V <sub>SS</sub> = ''0''	SC1, SC2 control:— 00 Change store and up/down latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	Control Word Strobe (CWS)	14	V <sub>DD</sub> V <sub>SS</sub>	Normal operation Causes control word to be written into control latches
	DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected VDD VSS	Normal operation Display drivers disabled Leading zero blanking inhibited



#### CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/DOWN, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the CWS (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/ or Up/Down latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/Down latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/Down latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a data transfer operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the DATA TRANSFER pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while DT is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first  $\overline{\text{DT}}$  pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first  $\overline{\text{DT}}$  pulse, the data for D3 must be valid during the second  $\overline{\text{DT}}$  pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth  $\overline{\text{DT}}$  pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Figure 12 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
tows	Control Word Strobe Width (min)		275	1783	ns
tics	Internal Control Set-up (min)	1 5	2.5	3	μs
totw	DATA TRANSFER pulse width (min)	13	300		ns
tscs	Control to Strobe setup (min)	100	300		ns
tsch	Control to Strobe hold (min)	183	300		ns
tIDs	Input Data setup (min)	Sel. 1	300		ns
tIDh	Input Data Hold (min)	1000	300		ns
tTDacc	Output Data access		300	100	ns
tTDf	Output Transfer to Data float	13/	300		ns

### ICM7217/ICM7227

## **BINTERSIL**

#### **APPLICATIONS**

#### **FIXED DECIMAL POINT**

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a  $39\Omega$  series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a  $75\Omega$  series resistor to Vpp.

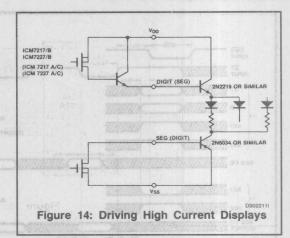
To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Performance Characteristics for a similarly operating multi-digit connection.



Figure 13: Forcing Leading Zero Display

#### DRIVING LARGER DISPLAYS

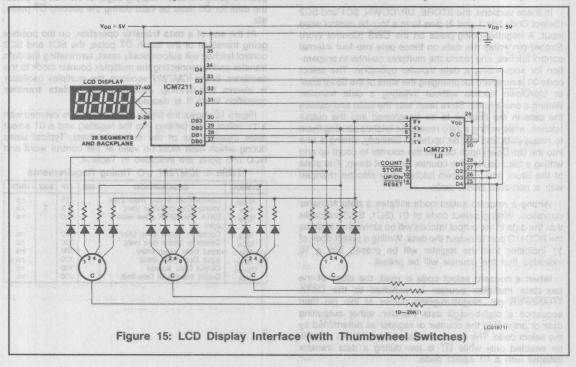
For displays requiring more current than the ICL7217/7227 can provide, the circuits of Figure 14 can be used.

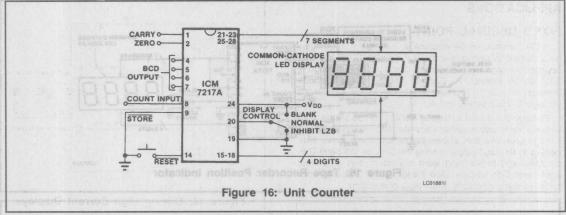


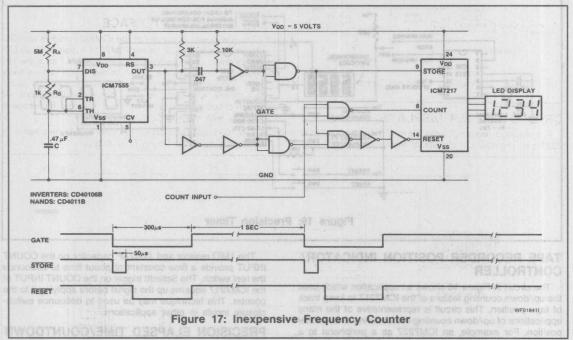
#### LCD DISPLAY INTERFACE

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 15. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10-20k $\Omega$  resistors on the switch BCD lines serve to isolate the switches during BCD output.







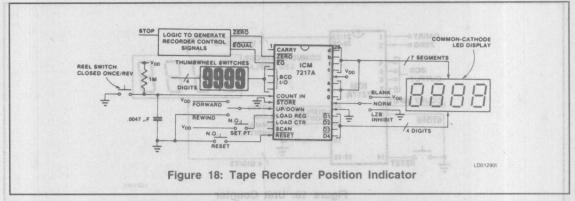
#### UNIT COUNTER WITH BCD OUTPUT

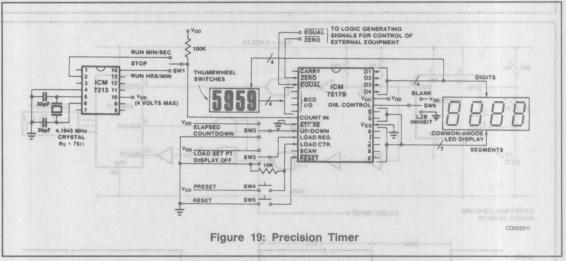
The simplest application of the ICM7217 is a 4 digit unit counter (Figure 16). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/ down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

#### **INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER**

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, STORE and RESET signals as shown

in Figure 17. To provide the gating signal, the timer is configured as an astable multivibrator, using RA, RB and C to provide an output that is positive for approximately one second and negative for approximately 300-500 µs. The positive waveform time is given by  $t_{WP} = 0.693 (R_A + R_B)C$ while the negative waveform is given by twn = 0.693 RBC. The system is calibrated by using a  $5M\Omega$  potentiometer for  $R_A$  as a "coarse" control and a  $1k\Omega$  potentiometer for  $R_B$ as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.





## TAPE RECORDER POSITION INDICATOR/CONTROLLER

The circuit in Figure 18 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the EQUAL or ZERO outputs, and serve as a numerical display for the processor.

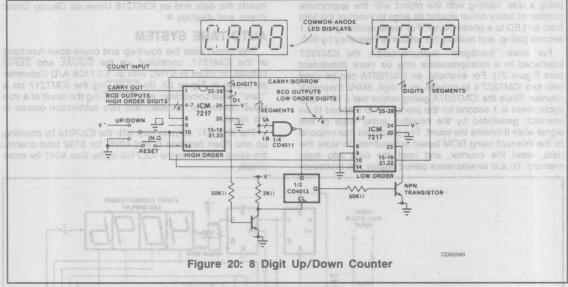
In the tape recorder application, the LOAD REGISTER, EQUAL and ZERO outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the EQUAL output used to stop the recorder either on fast forward, play or rewind.

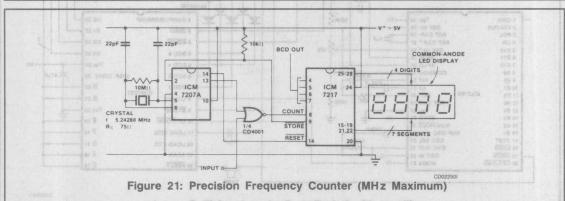
To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the ZERO output to be used to stop the recorder on rewind, leaving the leader on the reel.

The  $1M\Omega$  resistor and .0047 $\mu$ F capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

## PRECISION ELAPSED TIME/COUNTDOWN

The circuit in Figure 19 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the EQUAL output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.





This technique may be used on any 3-level input. The  $100 k\Omega$  pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 17 to generate a 1Hz reference.

#### 8-DIGIT UP/DOWN COUNTER

This circuit (Figure 20) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments  $\bar{a}$  or  $\bar{b}$  is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the

ICM7227 devices, since the two devices are operated as peripherals to a processor.

#### PRECISION FREQUENCY COUNTER/ TACHOMETER

The circuit shown in Figure 21 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the  $\overline{\text{STORE}}$  and  $\overline{\text{RESET}}$  signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to  $V_{DD}$ , the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01 second gating with Pin 11 connected to  $V_{DD}$ , and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by

number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

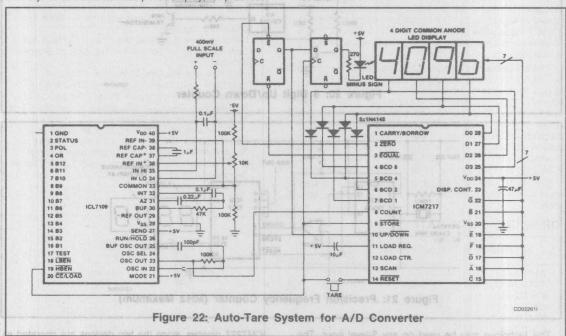
For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor

stores and displays it.

#### **AUTO-TARE SYSTEM**

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the EQUAL and ZERO outputs, to count in SYNC with an ICL7109 A/D Converter as shown in Figure 22. By RESETing the ICM7217 on a "tare" value conversion, and STORE-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7019 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.



at of

## ICM7224/ICM7225

## 4½-Digit LCD/LED Display Counter

#### GENERAL DESCRIPTION

The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V  $\pm 10\%$  supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In LED systems, the BRighTness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic or CERDIP package, or in dice.

#### ORDERING INFORMATION

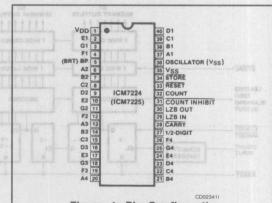
PART NUMBER	DISPLAY TYPE	COUNT
CM7224IPL	LCD	19999
ICM7224AIPL	LCD	15959
ICM7224/D	LCD	19999
ICM7224A/D	LCD	15959
ICM7224AIJL	LCD	15959
ICM7224IJL	LCD	19999
CM7225IPL	LED	19999
CM7225AIPL	LED	15959
ICM7225/D	LED	19999
CM7225A/D	LED	15959
CM7225AIJL	LED	15959
ICM7225IJL	LED	19999

Evaluation Kits, order ICM7224 EV/Kit or ICM7225 EV/Kit

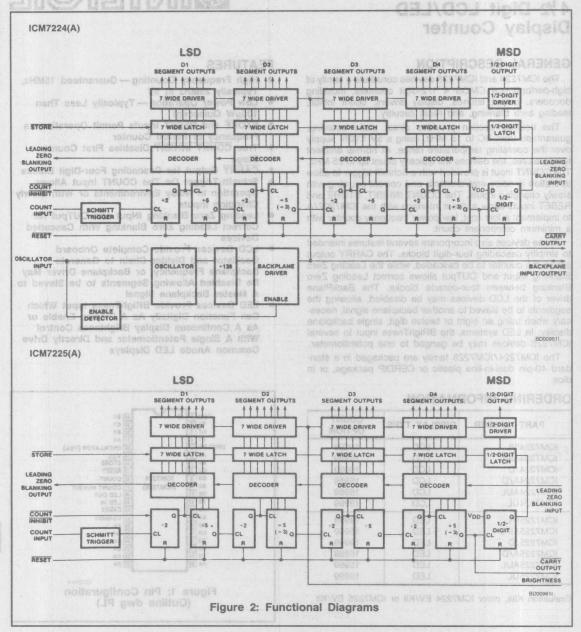
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#### **FEATURES**

- High Frequency Counting Guaranteed 15MHz, Typically 25MHz at 5V
- Low Power Operation Typically Less Than 100μW Quiescent
- STORE and RESET Inputs Permit Operation as Frequency or Period Counter
- True COUNT INHIBIT Disables First Counter Stage
- CARRY Output for Cascading Four-Digit Blocks
- Schmitt-Trigger On The COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs
- Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices
- LCD Devices Provide Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May Be Disabled Allowing Segments to be Slaved to A Master Backplane Signal
- LED Devices Provide BRighTness Input Which
  Can Function Digitally As A Display Enable or
  As A Continuous Display Brightness Control
  With A Single Potentiometer and Directly Drive
  Common Anode LED Displays



M7225 EV/Kit Figure 1: Pin Configuration (Outline dwg PL)



### ICM7224/ICM7225

### ABSOLUTE MAXIMUM RATINGS

 Operating Temperature Range ...... -20°C to +85°C Storage Temperature Range ..... -55°C to +125°C Lead Temperature (Soldering, 10sec) ......300°C

**BINITERSIL** 

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than Vpp or less than Vss may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Theses are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **ELECTRICAL CHARACTERISTICS** ( $V_{DD} = 5V \pm 10\%$ , $T_A = 25$ °C, $V_{SS} = 0V$ unless otherwise indicated) ICM7224 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Operating current	Test circuit, Display blank		10	50	μΑ
VSUPPLY	Operating supply voltage range (VDD - VSS)	KY VOLTAGE (VI	3		6	٧
losci	OSCILLATOR input current	Pin 36		±2	±10	μА
t <sub>R</sub> , t <sub>F</sub>	Segment rise/fall time	C <sub>load</sub> = 200pF	INT IN	0.5	DAU OL	
t <sub>R</sub> , t <sub>F</sub>	BackPlane rise/fall time	C <sub>load</sub> = 5000pF		1.5		μs
fosc	Oscillator frequency	Pin 36 Floating		19		kHz
fBP	Backplane frequency	Pin 36 Floating		150		Hz

#### **ICM7225 CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISTBY	Operating current display off	Pin 5 (BRighTness) at Vss Pins 29, 31-34 at V <sub>DD</sub>		10	50	μΑ
VSUPP	Operating supply voltage range (VDD - Vss)	1981 - 2000	4		6	٧
IDD	Operating current	Pin 5 at V <sub>DD</sub> , Display 18888	Pos	200	and sale	mA
ISLK	Segment leakage current	Segment Off		±0.01	±1	μΑ
ISEG	Segment on current	Segment On, Vout = +3V	5	. 8	11	
1 <sub>H</sub>	Half-digit on current	Half-digit on, Vout = +3V	10	16	4100	mA

### **FAMILY CHARACTERISTICS**

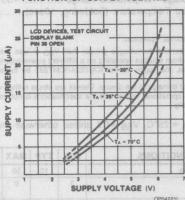
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
lp (	Input Pullup Currents	Pins 29, 31, 33, 34 Vout = V <sub>DD</sub> – 3V	IRR SIN	10	3A8.49 30	μΑ
VIH	Input High Voltage	Pins 29, 31, 33, 34	3	7000	10007	
VIL	Input Low Voltage	Pins 29, 31, 33, 34	I P	华不成.	1	
VCT	COUNT Input Threshold	17 THE R. P. LEWIS CO., LANSING MICH. 400 P. LEWIS CO., LANSING, M		2		V
VCH	COUNT Input Hysteresis		-	0.5	100	
Іон	Output High Current	CARRY Pin 28 Leading Zero Blanking OUT Pin 30 Vout = V <sub>DD</sub> – 3V	350	500	mr 5	
loL	Output Low Current	CARRY Pin 28 Leading Zero Blanking Out Pin 30 Vout = +3V	350	500	1 98	μΑ
fCOUNT	Count Frequency	4.5V < V <sub>DD</sub> < 6V	0		15	MHz
ts,t <sub>R</sub>	STORE, RESET Minimum Pulse Width		3	100	OF THE	μs

### ICM7224/ICM7225

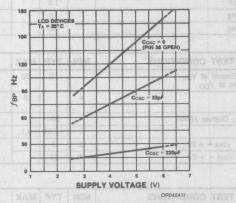
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### TYPICAL PERFORMANCE CHARACTERISTICS

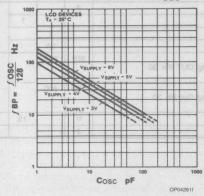
7224 OPERATING SUPPLY CURRENT AS A CONTROL OF SUPPLY VOLTAGE



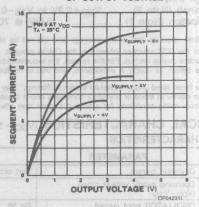
7224 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



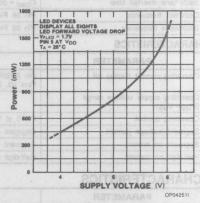
7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC



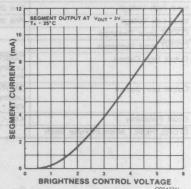
Ve a 7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

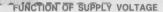


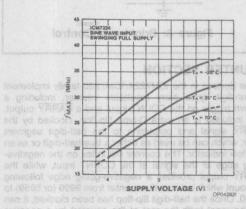
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

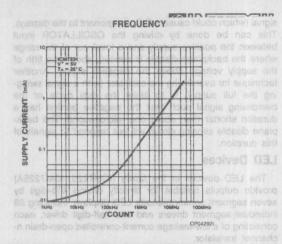


7225 LED SEGMENT CURRENT AS A FUNCTION
OF BRIGHTNESS CONTROL VOLTAGE









INPUT	TERMINAL	ta level VOLTAGE	oo ed uso etotelene u eFUNCTION up disto edi
Leading Zero Blanking INput	in set, and supported	V <sub>DD</sub> or Floating V <sub>SS</sub>	Leading Zero Blanking Enabled Leading Zeroes Displayed
COUNT INHIBIT	31 ,	V <sub>DD</sub> or Floating	Counter Enabled Counter Disabled
RESET the lucifle ment of	e-by-two instructions and a state of the sta	V <sub>DD</sub> or Floating	Inactive Counter Reset to 0000
STORE almod ealst aine	rang dainw34ugni TMUC	V <sub>DD</sub> or Floating	Output Latches not Updated Output Latches Updated

### CONTROL INPUT DEFINITIONS

In this table, V<sub>DD</sub> and V<sub>SS</sub> are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

# DETAILED DESCRIPTION

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional 4 ½-digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any D.C. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to Vss. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on

the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding  $5\mu s$  (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short  $(1-2\mu s)$  rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V<sub>DD</sub>; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

### ICM7224/ICM7225

**BINTERSIL** 

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

#### **LED Devices**

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving 4 ½-digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value ( $100k\Omega$  to  $1M\Omega$ ) to minimize power consumption, which can be significant when the display is off.

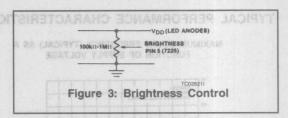
The BRighTness input may also be operated digitally as a display enable; when a  $V_{DD}$ , the display is fully on, and at  $V_{SS}$ , fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for Vss; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (15mW/°C above 35°C). Power dissipation for the device is given by:

### P = (VDD -VFLED) x (ISEG) x (nSEG)

where V<sub>FLED</sub> is the LED forward voltage drop, I<sub>SEG</sub> is segment current, and n<sub>SEG</sub> is the number of "ON" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.



### COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a CARRY output. Also included is an extra D-type flip-flop, clocked by the CARRY signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT input, while the CARRY output provides a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the RESET terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent CARRY outputs will not be affected.

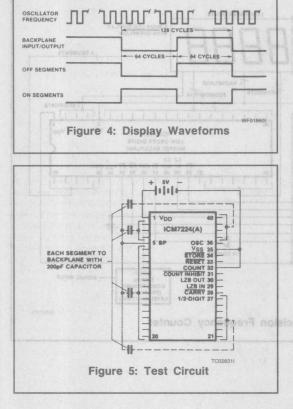
A negative level at the COUNT INHIBIT input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

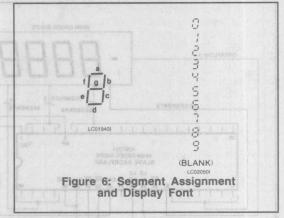
Each decade of counter drives directly into a four-toseven decoder which develops the seven-segment output code. The output data is latched at the driver, when the STORE pin is low, these latches are updated, and when high or floating, the latches hold their contents.

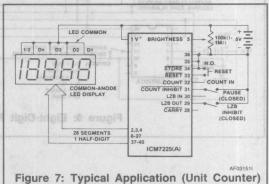
The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes; when low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

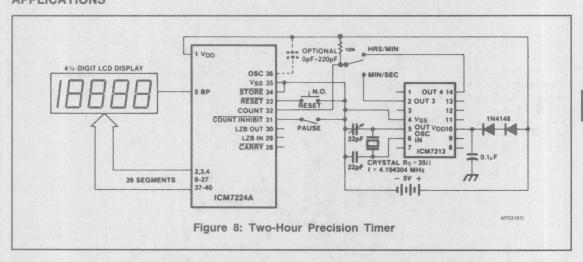
The STORE, RESET, COUNT INHIBIT, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The CARRY and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 to ICM7225 devices in four-digit blocks.

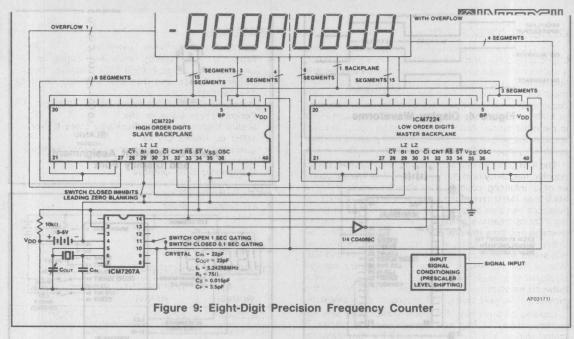


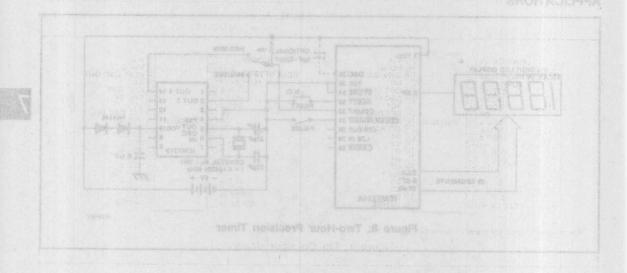




**APPLICATIONS** 







### ICM7226A/B 8-Digit Multi-Function Frequency Counter/Timer

### GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio ( $f_A/f_B$ ) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval**, the 10MHz timebase gives a  $0.1\mu s$  resolution. In **period average** and **time interval average**, the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in  $\mu$ s. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.



#### **FEATURES**

- CMOS Design for Very Low Power
- Output Drivers Directly Drive Both Digits and Segments of Large 8 Digit LED Displays. Both Common Anode and Common Cathode Versions Are Available
- Measures Frequencies From DC to 10MHz;
   Periods From 0.5 μs to 10s
- Stable High Frequency Oscillator Uses Either 1MHz or 10MHz Crystal
- Control Signals Available for External Systems Operation
- Multiplexed BCD Outputs

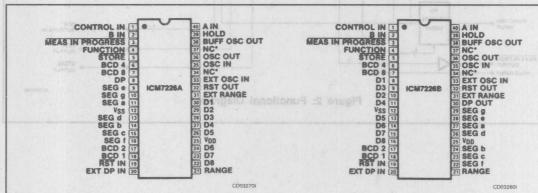
### **APPLICATIONS**

- Frequency Counter
- Period Counter
- Unit Counter
- Frequency Ratio Counter
- Time Interval Counter

### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7226AIPL	-25°C to +55°C	40 pin PLASTIC DIP
ICM7226A/D	- ATHOS	DICE
ICM7226BIJL	-25°C to +85°C	40 pin CERDIP
ICM7226B/D	- Sumpared	DICE
ICM7226AIJL	-25°C to 85°C	40 pin CERDIP
ICM7226BIPL	-25°C to 85°C	40 pin PLASTIC DIP

NOTE: An evaluation kit is available for these devices order ICM7226AEV/KIT.



\*For maximum frequency stability, connect to VDD or VSS

Figure 1: Pin Configurations

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### ABSOLUTE MAXIMUM RATINGS

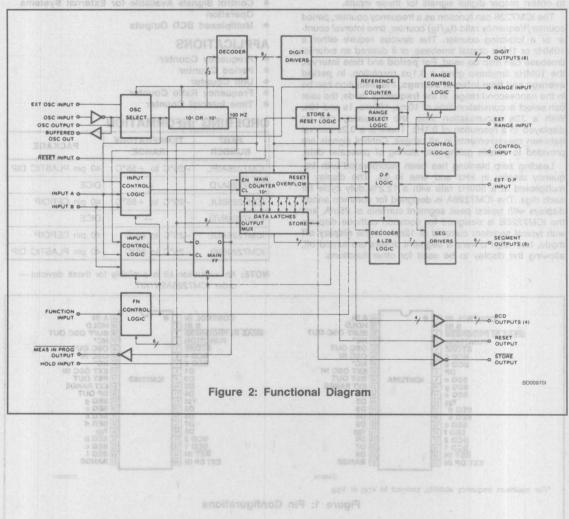
Maximum Supply Voltage (VDD - VSS)6.5V
Maximum Digit Output Current400mA
Maximum Segment Output Current60mA
Voltage on any Input or Output Terminal (Note 1)
$(V_{SS}-0.3V)$ to $(V_{DD}+0.3V)$

Maximum Power Dissipation at 70°C (Note 2)	
ICM7226A	1.0W
ICM7226B	
Operating Temperature Range25°C to	+85°C
Storage Temperature Range55°C to -	+125°C
Lead Temperature (Soldering, 10sec)	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\*Note 1: Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding VDD or VSS by 0.3V.

Note 2: Assumes all leads soldered or welded to PC board and free air flow.





### **ELECTRICAL CHARACTERISTICS** (V<sub>DD</sub> = 5.0V, T<sub>A</sub> = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
loo	Operating Supply Current	Display Off Unused inputs to VSS	14.18.18	2 0	5	mA
VSUPPLY	Supply Voltage Range V <sub>DD</sub> - V <sub>SS</sub>	-25°C < T <sub>A</sub> < 85°C Input A, Input B Frequency at f <sub>MAX</sub>		Hips curre	6.0	V <sub>o</sub> l
fA(max)	Maximum Guaranteed Frequency Input A, Pin 40	-25°C < T <sub>A</sub> < 85°C 4.75V < V <sub>DD</sub> < 6.0V Figure 4 Function = Frequency,	0,89,89,75 the	23,24,26, ofput curt		140
	01	Ratio, Unit Counter Function = Period, Time Interval	10 2.5	20143 B	Parket Military	MHz
fB(max)	Maximum Frequency Input B, Pin 2	-25°C < T <sub>A</sub> < 85°C 4.75V < V <sub>DD</sub> < 6.0V Figure 5	2.5	1,20,21 voltage di voltage	of trade for trade fr SMIS	I IV
Ωχ	Minimum Separation Input A to Input B Time Interval Function	-25°C < T <sub>A</sub> < 85°C 4.75V < V <sub>DD</sub> < 6.0V Figure 6	250	il eonatei ileat too	ien Yugni ma seutav	ns
fosc	Osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	-25°C < T <sub>A</sub> < 85°C 4.75V < V <sub>DD</sub> < 6.0V	10 (0.1)	717	INOU	MHz
9m	Oscillator Transconductance	V <sub>DD</sub> = 4.75V T <sub>A</sub> = +85°C	2000	is ava	tot neut	μs
f <sub>mux</sub>	Multiplex Frequency	f <sub>osc</sub> = 10MHz	boised	500	Leganie	Hz
	Time Between Measurements	fosc = 10MHz	sidt to	200	MEN THE	ms
dV <sub>in</sub> /dt	Input Rate of Charge	Inputs A, B	ABSSTN	15	aven ne	mV/μs
V <sub>IL</sub>	INPUT VOLTAGES PINS 2, 19, 33, 39, 40, 35 input low voltage	-25°C < T <sub>A</sub> < +85°C	roafly, i ladz on realstor	Special MHz qu Choaca	1,0	ATZZEALU
VIH	input high voltage	set ICM7228AEV/Ids	3.5	ket Ord	nes Of E	
lilk	PIN 2, 39, 40 INPUT LEAKAGE, A, B		-	nauvarijašimi	20	μΑ
RIN	Input resistance to V <sub>DD</sub> PINS 19,33	V <sub>IN</sub> = V <sub>DD</sub> -1.0V	100	400		kΩ
R <sub>IN</sub>	Input resistance to VSS PIN 31	V <sub>IN</sub> = +1.0V	50	100	-4	Kaz
loL	Output Current PINS 3,5,6,7,17,18,32,38	V <sub>OL</sub> = +0.4V	400	FEWARDS		μΑ
ЮН	PINS 5,6,7,17,18,32	V <sub>OH</sub> = +2.4V	100	(49)(30)		μΑ
ГОН	PINS 3,38	$V_{OH} = V_{DD} - 0.8V$	265	THE REV		μΑ
	ICM7226A PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER	0/9 0 dg 030m 2 Gg	Aruo SCR	reception.		
ЮН	high output current	$V_O = V_{DD} - 2.0V$	150	180		mA
lor	low output current	$V_0 = +1.0V$	141U8 0 80	-0.3		
loL	SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	V <sub>O</sub> = +1.5V	25	35	STIS.	mA
ІОН	high output current	V <sub>O</sub> = V <sub>DD</sub> - 1.0V		100	100	μΑ
VIL	MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage	90V 00 00 00 00 00 00 00 00 00 00 00 00 0	7(24)	UO 9 608 UO A 028	0.8	MEIN SUB MEIN SUB
VIH	input high voltage	The Control of the Co	2.0			V
RIN	input resistance to Vss	$V_{IN} = +1.0V$	50	100		kΩ

Figure 3: Test Circuit



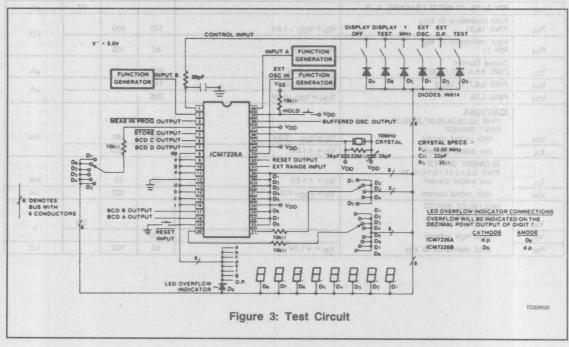
### ELECTRICAL CHARACTERISTICS (CONT.) AT NOS - DOWN CONTRACTOR AND LADIATORIES

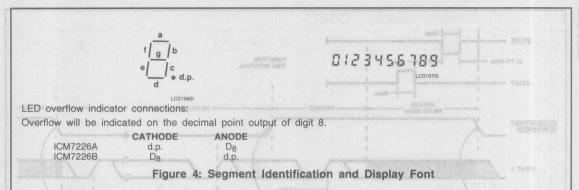
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Am	ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16	Display OH Unused arguits to Vsg		Ylqque	Operating	gal
loL	low output current	V <sub>O</sub> = +1.0V	50	75	Bospey Vo	mA .v
ЮН	high output current	$V_O = V_{DD} - 2.5V$		100		μΑ
ІОН	SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30 high output current	$V_O = V_{DD} - 2.0V$	voreuper3 5	015	munikski A tugal	mA
ILIN .	leakage current	Vo = Vss			10	μΑ
VIL	MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage	-25°C < 7x < 86°C 4.75V < Mopy 5.0V		Pregusnos Plo 2	V <sub>DD</sub> -2.0	(xemist
VIH	input high voltage	, a arupmi	V <sub>DD</sub> -0.8			V
RIN	input resistance to VDD	$V_{IN} = V_{DD} - 1.0V$	100	360	muminavi	kΩ

NOTE: Typical values are not tested.

### **EVALUATION KIT**

An evaluation kit is available for the ICM7226A. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226A. With the help of this kit, an engineer or technician can have the ICM7226A "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIJL, a 10MHz quartz crystal, eight each 7-segment 0.3" LEDs, PC board, resistors, capacitors, diodes, switches and IC socket. Order Number ICM7226AEV/Kit.





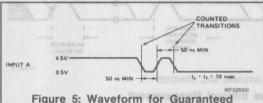


Figure 5: Waveform for Guaranteed Minimum f<sub>A</sub>(max) Function = Frequency, Frequency Ratio, Unit Counter.

### TIME INTERVAL MEASUREMENT

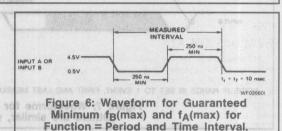
The ICM7226A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A/B as the first alternating signal states automatically prime the device. See Figure 7.



During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

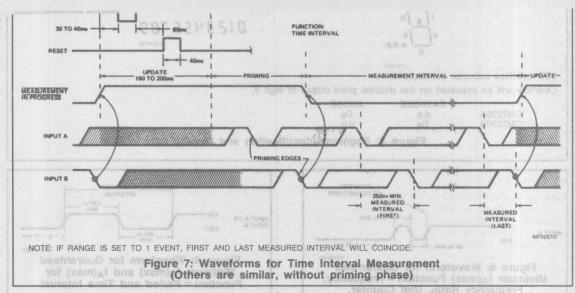
### **DETAILED DESCRIPTION**

#### INPUTS A & B

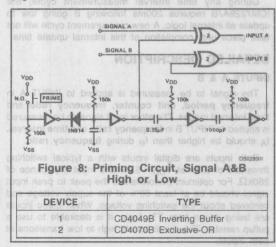
The signal to be measured is applied to INPUT A in frequency period, unit counter, frequency ratio and time interval modes. The other input signal to be measured is applied to INPUT B in frequency ratio and time interval. fA should be higher than fB during frequency ratio.

Both inputs are digital inputs with a typical switching threshold of 2.0V at  $V_{DD} = 5.0V$  and input impedance of  $250k\Omega$ . For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

**Note:** The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.



This can be easily accomplished with the following circuit: (Figure 8).



#### MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically  $125\mu$ s). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a  $10k\Omega$  resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Table 1: Multiple Input Control

	FUNCTION	DIGIT
FUNCTION INPUT Pin 4	Frequency Period Frequency Ratio Time Interval Unit Counter Oscillator Frequency	D <sub>1</sub> D <sub>8</sub> D <sub>2</sub> D <sub>5</sub> D <sub>4</sub>
PIN 31	1 Sec/100 Cycles 10 Sec/1k Cycles Enable External Range	D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub>
CONTROL INPUT PIN 1	Display Off Display Test 1MHz Select External Oscillator Enable External Decimal Point Enable	D <sub>4</sub> & Hold D <sub>8</sub> D <sub>2</sub> D <sub>1</sub> D <sub>3</sub>
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output Digit That is Connected Input	

#### CONTROL INPUTS

**Display Test** — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if **display off** is selected at the same time.

HOLD input at V<sub>DD</sub>. The chip will remain in this mode until HOLD is switched low. While in the **display off** mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5mA with a 10MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter.)

1MHz Select — The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in 1 µs increments rather than 0.1 µs.

External Oscillator Enable — In this mode, the EXTernal OSCillator INput is used, rather than the on-chip oscillator, for the Timebase and Main Counter inputs in period and time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to both OSC IN (pin 35) and EXT OSC IN (pin 33), or provide crystal for "default" oscillation, to avoid hang-up problems if an external OSC or TXCO will always be used, AC couple to OSC IN.

External Decimal Point Enable — When external decimal point is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

### Pigure 12: ICM7226A Typical TUPNI BANGE

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter, or if the EXTernal RANGE INput determines the measurement time. In all functional modes except unit counter, a change in the RANGE input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

#### **FUNCTION INPUT**

Six functions can be selected. They are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In **time interval** a flip flop is set first by a  $1 \to 0$  transition at INPUT A and then reset by a  $1 \to 0$  transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow indication is output on the Decimal Point Output during  $D_{\rm B}$ .

DESCRIPTION	MAIN COUNTER	COUNTER
Frequency (f <sub>A</sub> )	Input A	100 Hz (Oscillator ÷ 10 <sup>5</sup> or 10 <sup>4</sup> )
Period (t <sub>A</sub> )	Oscillator	Input A 190 Yakan
Ratio (f <sub>A</sub> /f <sub>B</sub> )	Input A	Input B
Time Interval (A → B)	Osc ON Gate	Osc OFF Gate
Unit Counter (Count A)	Input Asell nee	Not Applicable
Osc. Freq. (fosc)	Oscillator	100 Hz (Oscillator ÷ 10 <sup>5</sup> or 10 <sup>4</sup> )

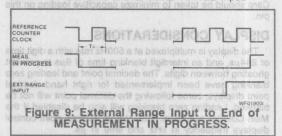
#### EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected, this input is active. Any of the digits, except D<sub>8</sub>, can be connected to this point. D<sub>8</sub> should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

**HOLD Input** — Except in the **unit counter** mode, when the HOLD input is at  $V_{DD}$ , any measurement in progress (before STORE goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at  $V_{DD}$ , the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

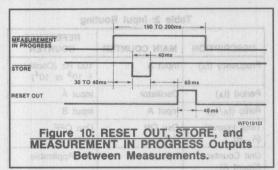
RESET Input — The RESET Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTernal RANGE Input — The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure 9 shows the relationship between MEASurement IN PROGRESS and EXTernal RANGE Input.



MEASUREMENT IN PROGRESS, STORE AND RESET Outputs — These Outputs are provided to facilitate external interfacing. Figure 10 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The MEASUREMENT IN PROGRESS output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.





BCD Outputs — The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A-Common Anode) or negative going (ICM7226B — Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

Table 3: Truth Table BCD Outputs

NUMBER	PIN 7	PIN 6	PIN 17	PIN 18
elomo jasi				
eriw epom.				
2				(1)
Bed 3 ped	0	0	100 120 61	1
9082				
5	0	1 1	()	the counter
6	0	1	1	0
duco 7 am e				
ru-asigane i	пв ,акетро	id ulo ueu	Missou A	0 300
100 go one	s Hsins n	0	sed on re	mugo <sub>1</sub> niem

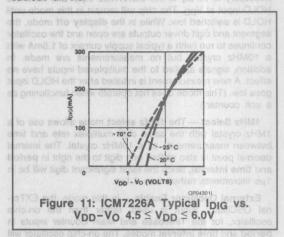
BUFFered OSCillator OUTput — The BUFFered OSCillator OUTput has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

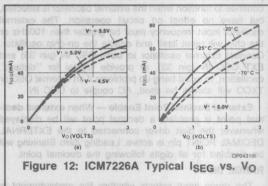
#### **DISPLAY CONSIDERATIONS**

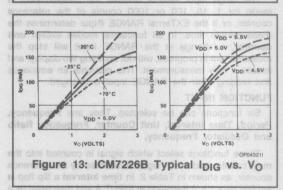
The display is multiplexed at a 500Hz rate with a digit time of  $244\mu s$ , and an interdigit blanking time of  $6\mu s$  to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the Main Counter overflows. The internal decimal point control displays frequency in kHz and time in  $\mu s$ .

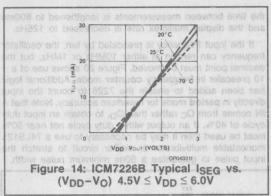
The ICM7226A is designed to drive common anode LED displays at a peak current of 25mA/segment, using displays with  $V_F = 1.8V$  at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with  $V_F = 1.8V$  at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 11, 12, 13 and 14 show the digit and segment currents as a

function of output voltage for common anode and common cathode drivers.









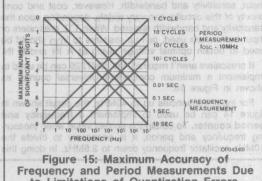
To increase the light output from the displays, VDD may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

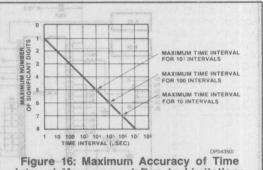
### **ACCURACY**

In a Universal Counter, crystal drift and quantization errors cause errors. In frequency, period and time interval modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

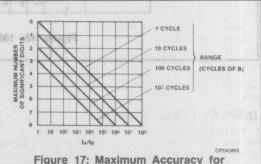
In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the frequency mode, maximum accuracy is obtained with high frequency inputs, and in period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 15, the least accuracy will be obtained at 10kHz. In time interval measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 16. In frequency ratio measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 17.



to Limitations of Quantization Errors.



Interval Measurement Due to Limitations of Quantization Errors.



Frequency Ratio Measurement Due to Limitations of Quantization Errors.

#### CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance



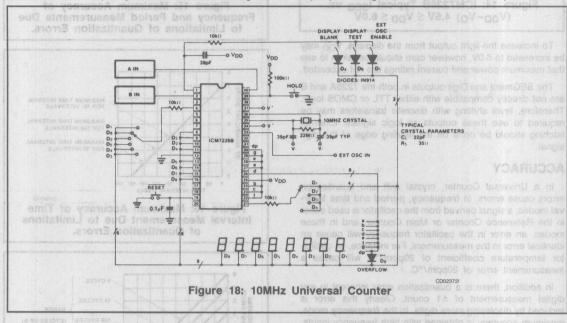
input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V<sub>DD</sub> should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in Figure 18.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **frequency and period counter.** To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this

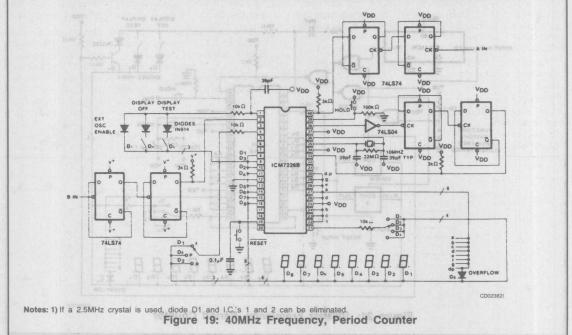
the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

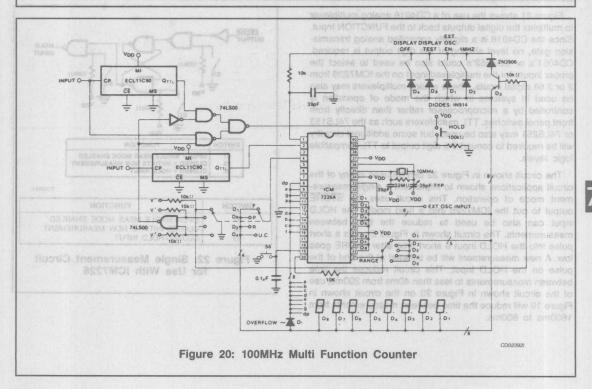
If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 20 shows use of a  $\div$  10 prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy. Note that A IN comes from QC rather than QD, to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74LS121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.



CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other directive in a variety of applications. Since A IN and B IN assigned inputs, additional circuity, with be required in mains applications, for input buffering, amplification, hysteresis and level shifting to obtain the required digital voltage. For many applications an FET source follower can be used for input buffering, and an EC. 101 (6) line receiver can be used for amplification and hysteresis to obtain righ impediance.





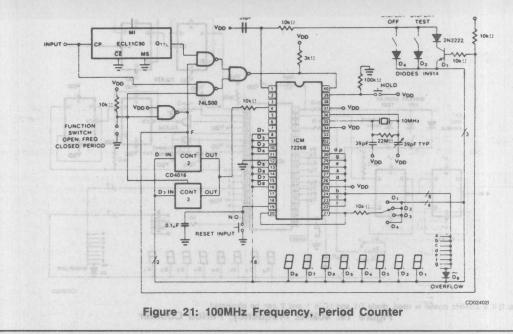


Figure 21 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74LS153 or 74LS251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

The circuit shown in Figure 22 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the STORE output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in Figure 23 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 23 on the circuit shown in Figure 19 will reduce the time between measurements from 1600ms to 800ms.

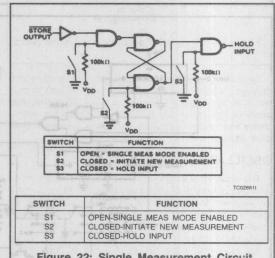


Figure 22: Single Measurement Circuit for Use With ICM7226

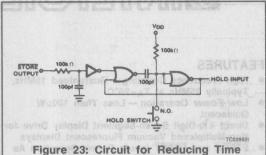


Figure 23: Circuit for Reducing Time **Between Measurements** 

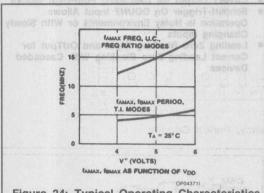


Figure 24: Typical Operating Characteristics

Figure 25 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive two ICM7211 display drivers. The ICM7226 EV/Kit may easily be interfaced to 2 ICM7211 EV/Kits in this way. A similar arrangement can be used for driving vacuum fluorescent displays with the ICM7235.

#### OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of  $10M\Omega$  or  $22M\Omega$  should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a load capacitance of 22pF and a series resistance of less than  $35\Omega$ . Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required gm can be calculated as follows:

$$g_{\rm m} = \omega^2 \ C_{\rm IN} \ C_{\rm OUT} \ {\rm Rs} \left(1 + \frac{C_{\rm O}}{C_{\rm L}}\right)^2$$

where 
$$C_L = \frac{C_{IN}C_{OUT}}{C_{IN} + C_{OUT}}$$

$$C_O = C_{rystal} \text{ static capacitance}$$

= Crystal Series Resistance = Input Capacitance Cin = Output Capacitance Cout

The required gm should not exceed 50% of the gm

specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4pF to CIN and COUT. For maximum frequency stability, CIN and Cour should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10MHz nor 1MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate

is  $f_{mux} = \frac{f_{osc}}{2 \times 10^4}$  for 10MHz mode and  $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$  for the 1MHz mode. The time between measurements is - in the 10MHz mode and  $\frac{2 \times 10^5}{f}$  in the 1MHz mode.

fosc The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a  $10k\Omega$  resistor should be added from the buffered oscillator output to VDD.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFFfered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator INput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to VDD or VSS and these two signals should be kept away from the oscillator circuit.

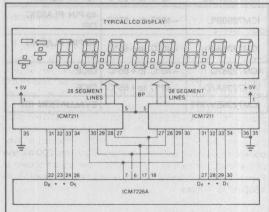


Figure 25: 10MHz Universal Counter System with LCD Display

### ICM7236

# 4½-Digit Counter/Vacuum Fluorescent Display Driver

### **GENERAL DESCRIPTION**

The ICM7236 and ICM7236A devices are high-performance CMOS 4½-digit counters. They include 7-segment decoders, output latches, count inhibit, reset, and leading zero blanking circuitry, as well as twenty-nine high-voltage open drain P-channel transistor outputs suitable for driving non-multiplexed (static) vacuum fluorescent displays.

The ICM7236 is a decade counter, providing a maximum count of 19999, while the ICM7236A is intended for timing purposes, and provides a maximum count of 15959.

The counter section of the two devices in the ICM7236 family provides direct static counting from DC to 15MHz guaranteed (with a 5V  $\pm 10\%$  supply) over the operating temperature range. At normal room temperatures, the device will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger for operation in noisy environments and allows correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allow a direct interface to the ICM7207 devices. This results in a low cost, low power frequency counter with minimum component count.

These devices also incorporate features intended to simplify cascading in four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allow correct leading zero blanking between four-decade blocks.

The ICM7236 and ICM7236A are packaged in a standard 40-pin dual-in-line plastic and CERDIP packages.

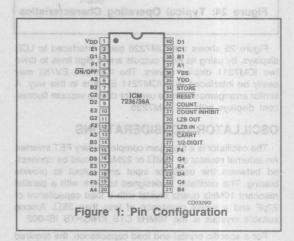
### ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE	
ICM7236IJL	-40°C to +85°C	40-PIN CERDIP	
ICM7236AIJL	-40°C to +85°C	40-PIN CERDIP	
ICM7236IPL	-40°C to +85°C	40-PIN PLASTIC DIP	
ICM7236AIPL	-40°C to+85°C	40-PIN PLASTIC DIP	
ICM7236/D	-40°C to+85°C	DICE	
ICM7236A/D	-40°C to+85°C	DICE	
ICM7236EV/KIT		EVALUATION KIT	



#### **FEATURES**

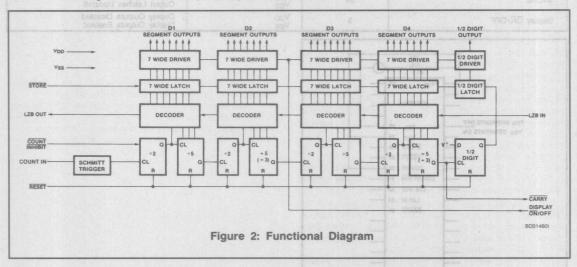
- High Frequency Counting Guaranteed 15MHz, Typically 25MHz at T<sub>A</sub>-25°C
- Low Power Operation Less Than 100μW Quiescent
- Direct 4 ½-Digit Seven-Segment Display Drive for Non-Multiplexed Vacuum Fluorescent Displays
- STORE and RESET Inputs Permit Operation As Frequency or Period Counter
- True COUNT INHIBIT Disables First Counter
- CARRY Output for Cascading Four-Digit Blocks
- Schmitt-Trigger On COUNT Input Allows
   Operation in Noisy Environments or With Slowly
   Changing Inputs
- Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices



### ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) 0.5W @ +70°C	Operating Temperature Range40°C to +85°C
Supply Voltage (V <sub>DD</sub> – V <sub>SS</sub> )	Storage Temperature Range55°C to +125°C Lead Temperature (Soldering, 10sec)300°C
Input VoltageVSS-0.3V to VDD+0.3V	Lead Temperature (Soldering, Tosec)

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



### ELECTRICAL CHARACTERISTICS (All parameters measured with VDD = 5V, TA = 25°C, VSS = 0V unless otherwise indicated).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUPPLY	Operating Supply Voltage Range (VDD - VSS)		3	5	6	V
IDD	Operating Current	Test circuit, Display blank	P0.770.77	10	50	μΑ
VDISP	Display Voltage		30 11	Last 1	30	٧
IDLK	Display Output Leakage	Output OFF, V <sub>DISP</sub> = V <sub>DD</sub> - 30V		0.1	10	μΑ
l <sub>p</sub>	Input Pullup Currents	Pins 29, 31, 33, 34 V <sub>IN</sub> = V <sub>DD</sub> -3V	ISHU	10		μΑ
VIH	Input High Voltage	Pins 29, 31, 33, 34	3			٧
VIL	Input Low Voltage	Pins 29, 31, 33, 34	The same	Fig. 8	2	٧
VCT	COUNT Input Threshold	enter 1		2		٧
VCH	COUNT Input Hysteresis	- Delite Little and State of the Company of the Com		0.5		٧
Юн	Output High Current	CARRY (Pin 28), LZB OUT (Pin 30) V <sub>OUT</sub> = V <sub>DD</sub> -3V.	350	500		μА
loL	Output Low Current	CARRY (Pin 28), LZB OUT (Pin 30) V <sub>OUT</sub> = +3V.	350	500		μА
fcount	Count Frequency	4.5V < V <sub>DD</sub> < 6V	0	25	15	MHz
ts, tw	STORE, RESET Minimum Pulse Width	N N I I I I WALLENDAL	3		E TO	μs

NOTES:

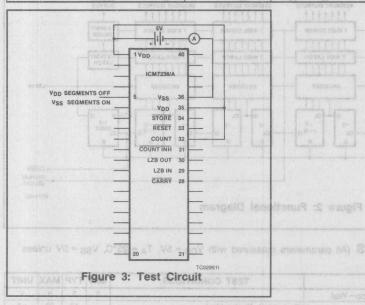
This limit refers to that of the package and will not occur during normal operation.
 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V<sub>DD</sub> or less than ground may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7236/7236A be turned on first.
 This limit refers to the display output terminals only.

### ICM7236

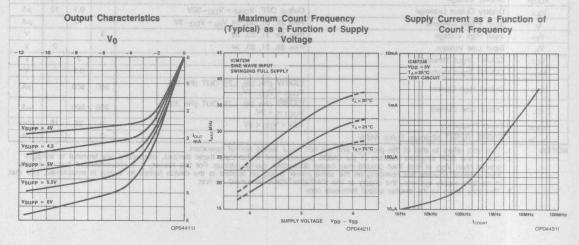
### **WINTERSIL**

### **OPERATING CHARACTERISTICS**

PRES H of O'CO INPUT ponsel and	TERMINAL	VOLTAGE	FUNCTION		
Leading Zero Blanking Input (LZB IN)	819QT 29 Q81018	V <sub>DD</sub> or Floating V <sub>SS</sub>	Leading Zero Blanking Enabled Leading Zeroes Displayed		
COUNT INHIBIT	31	V <sub>DD</sub> or Floating V <sub>SS</sub>	Counter Enabled Counter Disabled		
RESET Who applies seems are deeff some		V <sub>DD</sub> or Floating V <sub>SS</sub>	Inactive Counter Reset to 0000		
STORE	34	V <sub>DD</sub> or Floating V <sub>SS</sub>	Output Latches Not Updated Output Latches Updated		
Display ON/OFF	5	V <sub>DD</sub> V <sub>SS</sub>	Display Outputs Disabled Display Outputs Enabled		



### TYPICAL PERFORMANCE CHARACTERISTICS



### **DESCRIPTION OF OPERATION**

Both devices in the ICM7236 family provide twenty-nine outputs suitable for directly driving the anode terminals of  $4\,^{1\!\!/}2$  digit seven-segment non-multiplexed (static) vacuum-fluorescent displays. Each display output is the drain of high-voltage low-leakage P-channel transistor, capable of withstanding typically greater than -35 volts with respect to VpD. The output characteristics are shown graphically under ''Typical Characteristics.''

These chips also provide a display  $\overline{\text{ON}}/\text{OFF}$  input which may be used to disable all the segment outputs and thus blank the display. This input may also be used to control the display brightness by varying the duty cycle of a signal at the input swinging between  $V_{DD}$  and  $V_{SS}$ .

Note that these circuits have two terminals for V<sub>DD</sub>; both of these pins should be connected to the power supply positive terminal. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

These chips may also be used to directly drive non-multiplexed common-cathode LED displays, where each segment of the display is driven by one ICM7236 output, and the common cathode is connected to ground. With a 5V power supply and a 1.7V LED diode forward voltage drop, the current in an ''ON'' segment will be typically 3mA. This should provide sufficient brightness in displays up to about 0.3" character height.



Figure 4: Segment Assignment

G 3 4 5 5 6 9 (BLANK) LO20000 Figure 5: Display Font

#### COUNTER SECTION

The devices in the ICM7236 family implement a four-digit ripple-carry resettable counter, including a Schmitt trigger

COUNT input and a CARRY output. Also included is an extra D-type flip-flop, clocked by the carry signal, which controls the half-digit segment driver. This can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, and the CARRY output will provide a negative-going edge following the count which increments the counter from 9999 (or 5959) to 10000. Once half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the RESET terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent CARRY outputs will not be affected.

A negative level at the COUNT INHIBIT disables the first divide-by-two flip-flop in the counter chain without affecting its clock. This provides a true count inhibit which is not sensitive to the state of the COUNT input, and prevents false counts which can result from a normal logic gate forcing the state of the clock to prevent counting.

Each decade is fed directly into a four-to-seven line decoder which generates the seven-segment output code. Each decoder output corresponds to one-segment terminal of the device. The output data is latched at the driver. When the STORE pin is at a negative level, the latches are updated, and when the pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating, or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the Leading Zero Blanking INput is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, and can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, on an eight-decade counter with overflow using two ICM7236 devices, the Leading Zero Blanking OUTput of the high-order digit device would be connected to the Leading Zero Blanking INput of the low-order digit device. This will assure correct leading zero blanking for all eight digits.

The STORE, RESET, COUNT INHIBIT, and Leading Zero Blanking INputs are provided with internal pullup devices, so that they may be left open when a positive level is desired. The CARRY and Leading Zero OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7236 devices in four-digit blocks.

### **CONTROL INPUT DEFINITIONS**

In this table, V<sub>DD</sub> and V<sub>SS</sub> are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

Figure 6: Typical DC Vacuum Fluorescent Display Connection

VACUUM FLUORESCENT DISPLAYS (4½-DIGIT):

N.E.C. Electronics, Inc.
Model FIP5F8S

The decoders also include zero detect and blanking buttor of provide, leading zero blanking. When the Leading Zero lanking illiput is floating, or at a positive level, this circultry enabled and the device will blank leading zeroes. When expective level, or be failed zero Blanking illiput is at a negative level, or chall-digit is set leading zero blanking is arbititud, and lanking OUTput is provided to allow cabcaded devices to ark leading zeroes correctly. This output will assume a pative level only when all four digits are blanking librut is at a power when the Leading Zero Blanking librut is at a power level and the realing zeroes correctly.

For example, on an eight-decade counter with overflow safing two 10M7286 devices, the teading Zero Blanking OUTput of the high-order digit device would be connected to the Leading Zero Blanking flyuit of the fow-order digit fevice. This will assure cornect leading zero blanking for all septs digits.

The STORE, RESET, COUNT INHIBIT, and Leading Zero Blanking (Nouts are provided with internat pullup devices, so that they may be jett open when a positive level is desired. The CARRY and Leading Zero OUTputs are sulfable to interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7286 devices to four-field videous.

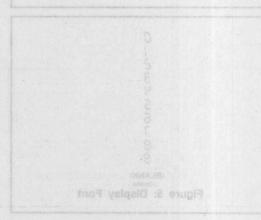
CONTROL HIPUT DEFINITIONS

In this table, Vpg and Vss are considered to be normal perating input logic levels. Actual input low and high levels the specified under Operating Characteristics. For lowest ower consumption, input signals should awing over the full

nd the common cathods is connected to ground. With a V power supply and a 1.7V LED diode forward voltage rop, the current if an "ON" segment will be typically 3mA, his should provide sufficient brightness in displays up to bout 0.3° character height.



Source 4: Seament Assignment



COUNTER SECTION

The devices in the ICM7286 family implement a four-digit tipger carry resettable counter, including a Schmitt trigger

### ICM7240/ICM7250 ICM7260 Programmable Timer

### GENERAL DESCRIPTION

The ICM7240/50/60 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICM8240/50/60 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. The ICM7260 is specifically designed for the time delays in seconds, minutes and hours. All three devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50/60 are packaged in 16 pin CERDIP packages.

Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.



#### FEATURES VE.O- 22V

- Replaces 8240/50/60, 2240 in Most Applications
- Timing From Microseconds to Days
- May Be Used As Fixed or Programmable
   Counter
- Programmable With Standard Thumbwheel Switches
- Select Output Count From

  1RC to 255RC (ICM7240)

  1RC to 99RC (ICM7250)

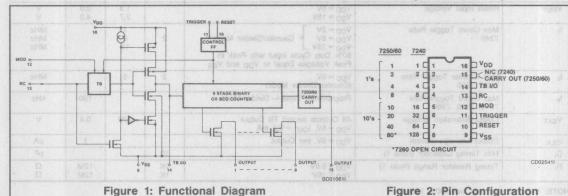
  1RC to 59RC (ICM7260)
- Monostable or Astable Operation
- Low Supply Current: 115μA @ 5 Volts
- Wide Supply Voltage Range: 2-16 Volts
- Cascadeable

### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7240IJE	-25°C to +85°C	16 Lead CERDIP
ICM7250IJE	-25°C to +85°C	16 Lead CERDIP
ICM7260IJE	-25°C to +85°C	16 Lead CERDIP
ICM7240/D	Sase Output—	DICE**
ICM7250/D	de con on	DICE**
ICM7260/D		DICE**

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

(Outline dwg JE) ICM7240/7250/7260



203403-002

ICM7240/50/60

### ICM7240/ICM7250/ICM7260



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD-VSS)	Power Dissipation <sup>[2]</sup>
Input Voltage <sup>[1]</sup>	Operating Temperature Range25°C to +85°
Terminals 10,11,12,13,14 Vss -0.3V to Vpp + 0.3V	Storage Temperature Range65°C to +150°
Maximum continuous output	Lead Temperature (Soldering, 10sec)300°

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V<sub>DD</sub> or less than V<sub>SS</sub> may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50/60 be turned on first.

2. Derate at -2mW/°C above 25°C.

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

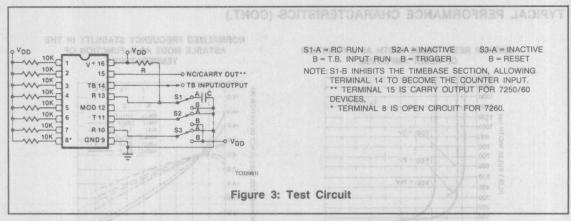
 $(V_{DD} = 5V, T_A = +25^{\circ}C, R = 10k\Omega, V_{DD} = 0V C = 0.1\mu\text{F}, unless otherwise specified.)$ 

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUPPLY	Guaranteed Supply Voltage (VDD-VSS)	k applied to the TB R Cascac	2 00	i në ba	16	ed varia
DO	Supply Current	Reset Operating, R = $10 k \Omega$ , C = $0.1 \mu F$ Operating, R = $1 M \Omega$ , C = $0.1 \mu F$ TB Inhibited, RC Connected to GND	OUTS! BIT!	125 300 120 125	800 600	μΑ μΑ μΑ μΑ
00000 8	Timing Accuracy	transistors, thereby	augluo ni	5000	6411 860	%
Δf/ΔT	RC Oscillator Frequency Temperature Drift	(Exclusive of RC Drift)	il prograti lard thur	250	AND-ING y the use	ppm/°C
VOTB DOO	Time Base Output Voltage	ISOURCE = 100μA   1500 × 10	M ? 240/	3.50 0.40	nnections HDIP pa	oc bevelore O mig 81
ITBLK **30IQ	Time Base Output Leakage Current	RC = Ground		a progra	25	μΑ
Vмор	Mod Voltage Level	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V	seques t	3.5 11.0	y oscillat	naup <mark>V</mark> it w
VTRIG	Trigger Input Voltage	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V		1.6 3.5	2.0 4.5	V
V <sub>RST</sub>	Reset Input Voltage	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V		1.3 2.7	2.0 4.0	V
ft	Max Count Toggle Rate 7240	V <sub>DD</sub> = 2V V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V <sub>DD</sub> and V <sub>SS</sub>	2	1 6 13		MHz MHz MHz
ft (DESCRESS) TUD')	Max Counter Toggle Rate 7250, 7260	V <sub>DD</sub> = 5V (Counter/Divider Mode)	2	5		MHz
ft	Max Count Toggle Rate 7240, 7250, 7260	Programmed Timer — Divider Mode	MIP		100	kHz
VSAT	Output Saturation Voltage	All Outputs except TB Output VDD = 5V, IOUT = 3.2 mA	HP	0.22	0.4	٧
lolk	Output Leakage Current	V <sub>DD</sub> = 5V, per Output		18 5	1	μΑ
Ct	MIN Timing Capacitor (Note 1)		10			pF
Rt	Timing Resistor Range (Note 1)	V <sub>DD</sub> ≤ 5.5V V <sub>DD</sub> ≤ 16V	1K 1K	*	12M 12M	Ω

Figure 1: Functional Diagram

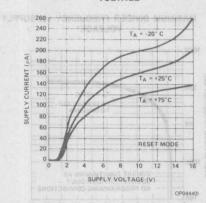
NOTE: 1. For Design only, not 100% tested.

Outline dwg JE

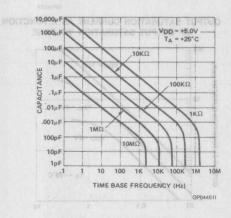


### TYPICAL PERFORMANCE CHARACTERISTICS

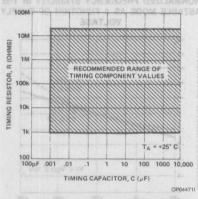
### SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



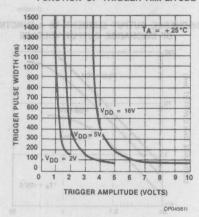
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



### RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

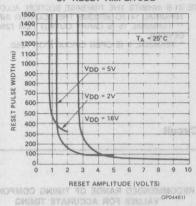


### MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE

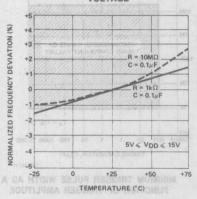


### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

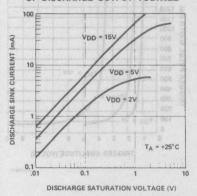
MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



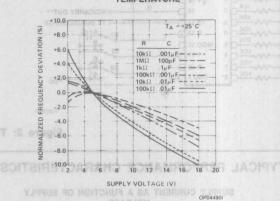
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



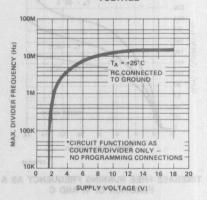
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



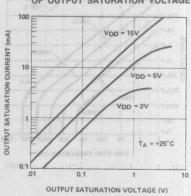
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF **TEMPERATURE** 



MAXIMUM DIVIDER FREQUENCY vs. SUPPLY **VOLTAGE\*** 



**OUTPUT SATURATION CURRENT AS A FUNCTION** OF OUTPUT SATURATION VOLTAGE



### ICM7240/ICM7250/ICM7260

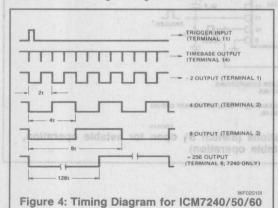
### CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state. and starts the time base oscillator. Then, external C is charged through external R from 20% to 70% of VDD-VSS, generating a timing waveform with period t, equal to 1RC. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250/60. The timing cycle terminates when a positive level is applied to RESET. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carry-out is also HIGH. Each of the three devices utilizes an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250/60 have CARRY outputs.

In most timing applications, one or more of the counter outputs are connected back to RESET the circuit will start timing when a TRIGGER is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the RESET (switch  $S_1$  open), the circuit operates in its astable, or free-running mode, after initial triggering.

# DESCRIPTION OF PIN FUNCTIONS COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 4). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.



#### Vss (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients.

### 

#### RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by a positive level applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

#### MODULATION AND SYNC INPUT (PIN 12)

The period, t, of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12.

#### TIMEBASE INPUT/OUTPUT PIN (PIN 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input if the RC pin is connected to Vss.

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50/60 is used to replace an 8240/50/60 or 2240.

#### CARRY OUTPUT (PIN 15, ICM7250/60 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 or 7260 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50/60 are shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive level on the RESET terminal (if TRIGGER is low), a positive level on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. (See Figure 6.)

#### PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain Nchannel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as any one of the outputs is low. Each output is capable of sinking ≈5mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) to would be 32t for a 7240 and 20t for a 7250/60. Similarly, if pins, 1, 5, and 6 were shorted to the output bus, the total time delay would be  $t_0 = (1 + 16 + 32)t$  for the 7240 or (1 + 10 + 20)t for the 7250/60. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

 $1t \le t_0 \le 255t \ (7240)$ 

 $1t \le t_0 \le 99t \ (7250)$ 

 $1t \le t_0 \le 59t \ (7260)$ 

WIII HOL SLOD.

The 7240/50/60 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see Figure 5. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

# GENERATION

In astable operation, as shown in Figure 5, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 4, which shows the phase relations between the counter outputs. Figure 6 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

#### THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 and ICM7260 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of 1<sub>RC</sub> to 99<sub>RC</sub>. Cascading two ICM7250's (using the carry out gate) would expand selection to 9999<sub>RC</sub>. For a

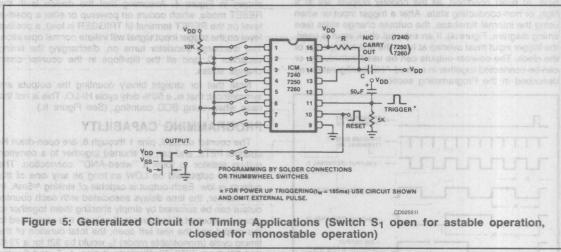
### NOTES ON THE COUNTER SECTION

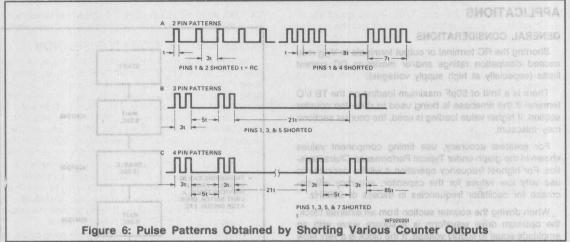
Used as a straight binary counter (ICM7240), as a ÷100 (ICM7250), or ÷60 (ICM7260) all devices are significantly faster than their bipolar equivalents. However, when using these devices as programmable counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), 100 (ICM7250), or 60 (ICM7260) the maximum input frequency must be limited to approximately 100kHz or less (with V<sub>DD</sub> equal to +5 volts). The reason for this is two-fold:

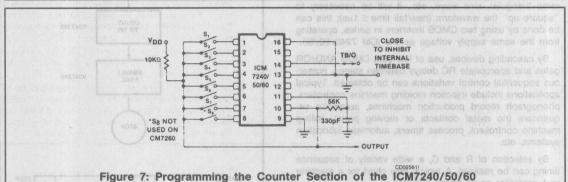
- a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter (8 counters for the ICM7240/50 and 7 for the ICM7260). Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the RESET/TRIGGER signal.
  - b. There must be a delay of the positive going output to RESET, (pin 10) and TRIGGER (pin 11). The RESET signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The TRIGGER overrides RESET.

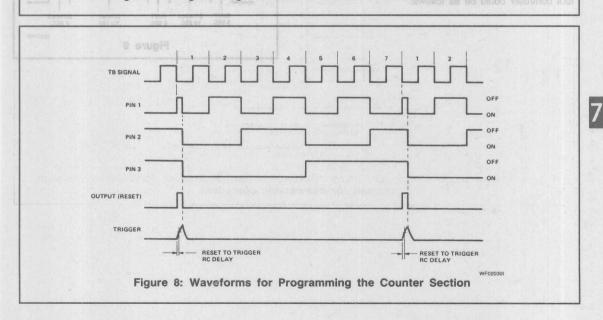
The delay between TRIGGER and RESET is generated by the signal RC network consisting of the  $56k\Omega$  resistor and the 330pF capacitor.

The delay caused by the counter ripple delays can be as long as  $2\mu s$  (5 volt supply), and the delay between RESET and TRIGGER should be at least  $2\mu s$ . The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 7 and 8.









# ICM7240/ICM7250/ICM7260



### **APPLICATIONS**

### GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to VDD may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time  $\leq 1 \mu s$ ); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50/60.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

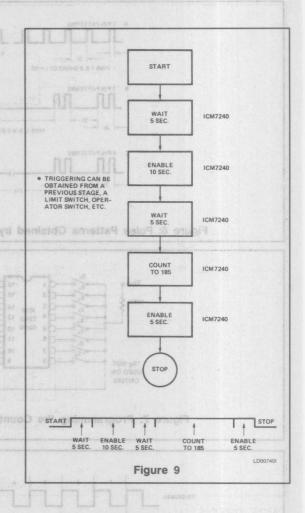
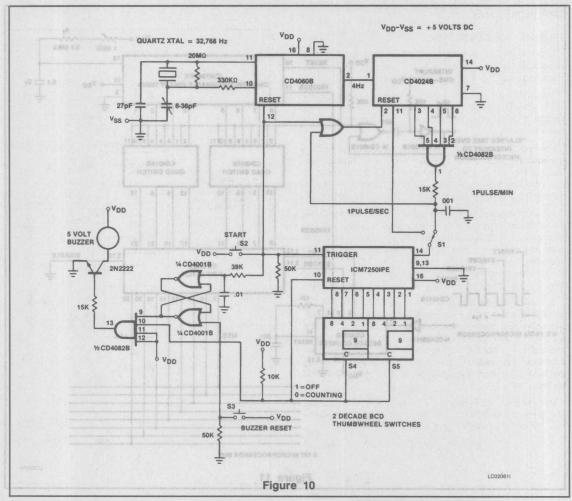


Figure 8: Waveforms for Programming the Counter Section



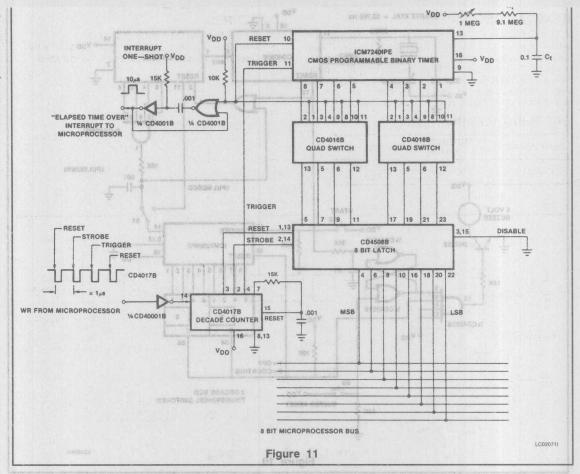
### **CMOS PRECISION PROGRAMMABLE** 0-99 SECONDS/MINUTES LABORATORY

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown in Figure 10, the timer can accurately measure preselected time intervals of 0-99 seconds or 0-99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0-99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the preprogrammed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.



# LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown in Figure 11, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four WRITE pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit

latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

With a resistor of approximately  $10M\Omega$  and capacitor of  $0.1\mu F$ , the time base of the ICM7240 is one second. Thus, a time of 1–255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.

### GENERAL DESCRIPTION

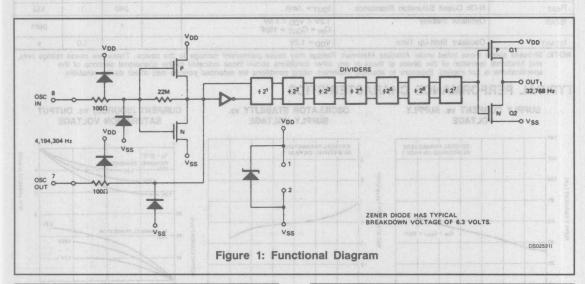
The ICM7241 is a fully integrated oscillator, 2 divider and output driver which efficiency converts 4.194304MHz to 32.768kHz using a minimum of power. Only three external components are necessary for complete oscillator operation; a 4.194304MHz crystal, a fixed input capacitor, and an output trimmer capacitor. The output has a low enough were flow 8.0 and least VO.S) enables virgue and account AA I. impedance to satisfy most drive requirements, a beneated ad for the line applicance and to fast of states inclinated beneat to asked \$17.5

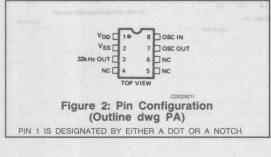
### FEATURES . [Short Circuit II] noits gize (C

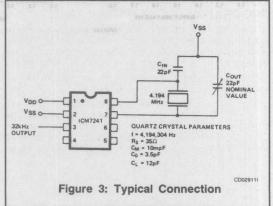
- Single Battery Operation (1.2 1.8V)
- Low Power Consumption Typ. 40μA @ 1.5V
- Oscillator Biasing Resistor Included On-Chip

### ORDERING INFORMATION

PART NUMBER	RT NUMBER TEMPERATURE RANGE	
ICM7241IPA	-20°C to +70°C	8-Lead Plastic







Timebase Generator

### NOTES:

1. All terminals may exceed the supply voltage (2.0V max) by ±0.3 volt provided that the currents in these terminals are limited to 2mA each care 2. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

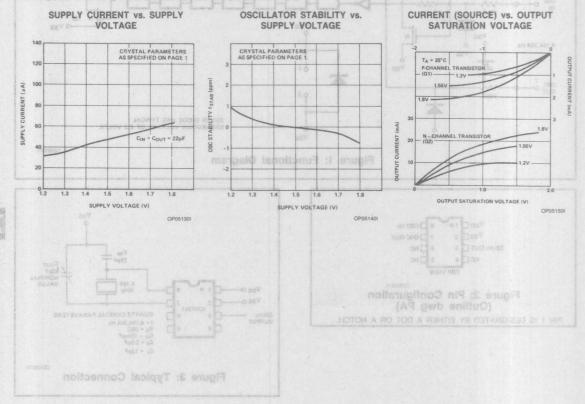
### **ELECTRICAL CHARACTERISTICS**

(VSS = 1.5V, VSS = 0V, fOSC = 4,194,304Hz, TA = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
IDD	Supply Current	GILLEGE ENDING	B-Lead	7070 A	40	70	μΑ
VSUPPLY	Guaranteed Operating Voltage Range	-20°C ≤ to ≤ 70°C	Plastic	1.2		1.8	V
RSAT	P-Ch Output Saturation Resistance	I <sub>OUT</sub> = .5mA			680	2	kΩ
RSAT	N-Ch Output Saturation Resistance	I <sub>OUT</sub> = .5mA			240	1	kΩ
fSTAB	Oscillator Stability	1.2V < V <sub>DD</sub> < 1.6V C <sub>IN</sub> = C <sub>OUT</sub> = 15pF			1		ppm
tstart and o	Oscillator Start-Up Time	V <sub>DD</sub> = 1.2V		9		1.0	S

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL PERFORMANCE CHARACTERISTICS





### GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

The ICM7242 is packaged in an 8-pin CERDIP.

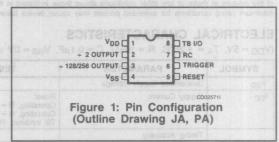
### ORDERING INFORMATION

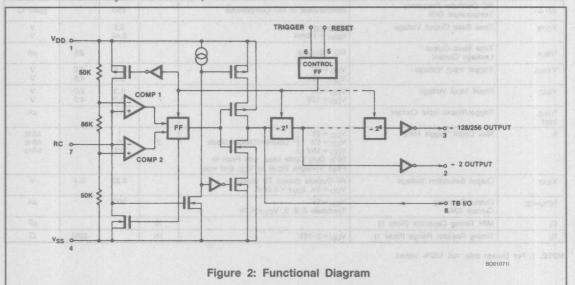
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CM7242D	gyr pasa	DICE**
CM7242IPA	-25°C to +85°C	8 pin MINI-DIP
CM7242IJA	-25°C to +85°C	8 pin CERDIP
CM7242CBA	0°C to +70°C	8 pin S.O.I.C.

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

### **FEATURES**

- Replaces The 2242 in Most Applications
- Timing From Microseconds to Days
- Cascadeable
- Monostable or Astable Operation
- Wide Supply Voltage Range: 2-16 volts
- Low Supply Current: 115μA @ 5 volts





7

Supply Voltage (V <sub>DD</sub> to V <sub>SS</sub> )	Power Dissipation <sup>[2]</sup>
(each output)	of an RC oscillator followed by an 8-bit binary counter. It will

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V<sub>DD</sub> or less than V<sub>SS</sub> may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.

2. Derate at -2mW/°C above 25°C.

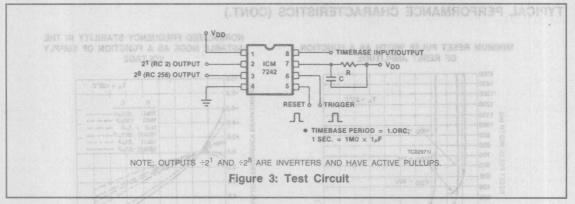
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

### **ELECTRICAL CHARACTERISTICS**

 $(V_{DD} = 5V, T_A = +25$ °C, R =  $10k\Omega$ , C =  $0.1\mu$ F,  $V_{SS} = 0V$  unless otherwise specified.)

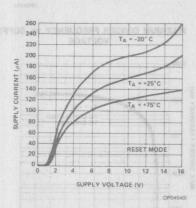
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Guaranteed Supply Voltage	S Du Miserials	2	01 0,67	16	V
	Supply Current	Reset Operating, R = $10k\Omega$ , C = $0.1\mu$ F Operating, R = $1M\Omega$ , C = $0.1\mu$ F TB Inhibited, RC Connected to Vs	3°88+	125 340 220 225	800 600	μΑ μΑ μΑ μΑ
	Timing Accuracy	C gridy for DICE cordina	land at 28	5	ni Limiti	%
Δf/ΔΤ	RC Oscillator Frequency Temperature Drift	Independent of RC Components		250		ppm/°C
Vотв	Time Base Output Voltage	ISOURCE = 100 µA		3.5 0.40		V
ITBLK	Time Base Output Leakage Current	RC = Ground			25	μΑ
VTRIG	Trigger Input Voltage	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V		1.6 3.5	2.0 4.5	V
V <sub>RST</sub>	Reset Input Voltage	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V	1.9500	1.3	2.0 4.0	V
ITRIG, IRST	Trigger/Reset Input Current		- I	10	Most	μΑ
fŧ	Max Count Toggle Rate	V <sub>DD</sub> = 2V V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V Counter/Divider Mode V <sub>DD</sub> = 15V Peak to Peak Voltages Equal to V <sub>DD</sub> and v <sub>SS</sub>	2	1 6 13		MHz MHz MHz
VSAT	Output Saturation Voltage	All Outputs except TB Output VDD = 5V, IOUT = 3.2mA		0.22	0.4	٧
ISOURCE	Output Sourcing Current 7242	V <sub>DD</sub> = 5V Terminals 2 & 3, V <sub>OUT</sub> = 1V		300		μΑ
Ct	MIN Timing Capacitor (Note 1)		10	The	Distance of	pF
Rt	Timing Resistor Range (Note 1)	V <sub>DD</sub> = 2-16V	1K		22M	Ω

NOTE: 1. For Design only, not 100% tested.

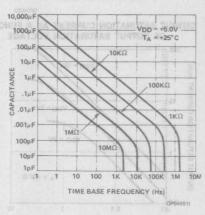


### TYPICAL PERFORMANCE CHARACTERISTICS

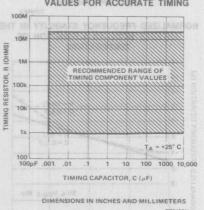
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



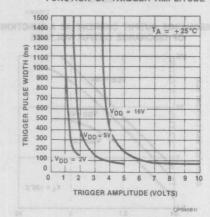
TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



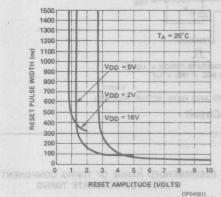
MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



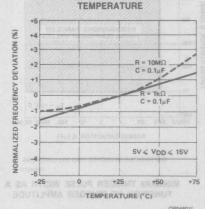
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### TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

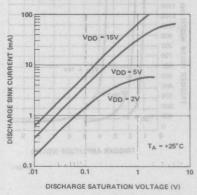
MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



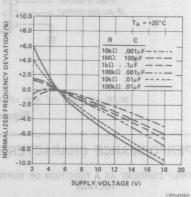
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF



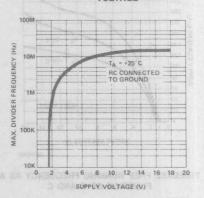
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



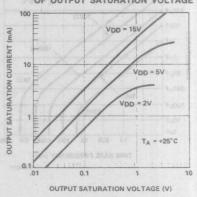
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



# OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



OP04631I

# 

### **OPERATING CONSIDERATIONS**

Shorting the RC terminal or output terminals to V<sub>DD</sub> may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200KHz.

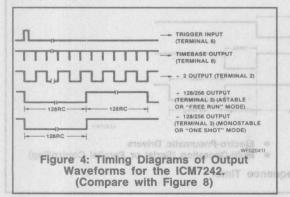
When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

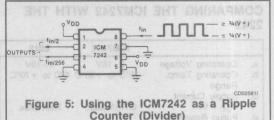
The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the onchip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

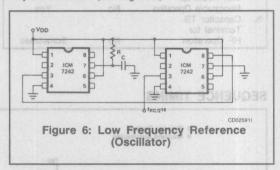
The timing diagram for the ICM7242 is shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor G, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the  $\div 2^8$  output returns to the high state.

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.



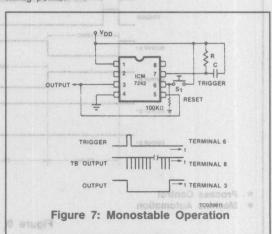


The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 6).

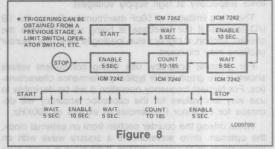


For monostable operation the  $\div 2^8$  output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

THE ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value presistors have been used on the ICM7242 to provide the comparator timing points.



timing can be realized. A typical flow chart for a machine tool controller could be as follows:



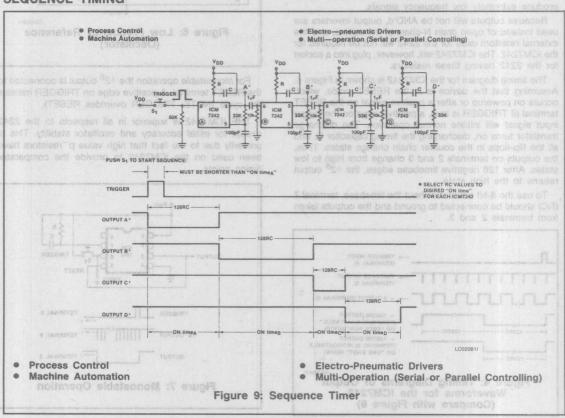
By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

### SEQUENCE TIMING

Capacitor TB

Terminal for

HF Operation



Sometimes

### GENERAL DESCRIPTION CONTROL OF THE PROPERTY OF

The ICM7245 is a very low current, low voltage microcircuit for use in analog watches. It consists of an oscillator, dividers, logic and drivers necessary to provide either bipolar or unipolar stepper motor drive for minimum-component count watches. The oscillator is extremely stable over wide ranges of voltage and temperature, and thus combines high accuracy with low system power. The ICM7245 is fabricated using Intersil's low threshold metal-gate CMOS process.

The inverter oscillator contains all components on-chip except for the tuning capacitor and quartz crystal. The binary divider consists of 15 stages, the last 5 of which may be reset. If a reset (stop) occurs during an output pulse, the duration of the pulse is not affected. When the reset is released, the first output occurs approximately 1 second later. For the bipolar version, memory reset logic is included to make sure the first pulse after a "stop" occurs on the opposite output from the one just before the "stop".

The bipolar bridge output consists of two large inverters, normally high. The output ON resistance of the P and N channel devices in series is  $200\Omega$  maximum @ 1mA. In unipolar operation, the output is made up of a single normally high inverter. The ON resistance of the N-channel device is  $50\Omega$  maximum @ 3mA.

### **FEATURES**

- Very Low Current Consumption: 0.4μA at 1.55
   Volt Typical
- 32kHz Oscillator Requires Only Quartz Crystal and Trimming Capacitor
- Bipolar Stepper Drive With Low Output On Resistance: 200ohms Maximum (7245 A/B/D/E/F)
- Unipolar Stepper Drive With Very Low Output
   On Resistance: 50ohms Maximum (7245U)
- Extremely Accurate: Oscillator Stability Typically
   0.1ppm
- STOP Function for Easy Time Synchronization
- Wide Temperature Range: -25°C to +85°C
- On Chip Fixed Oscillator Capacitor: 20pF ±20%

ORDE	RING	INFORM	ATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE		
ICM7245AIPA	-25°C to +85°C	8 pin Plastic DIP		
ICM7245BIPA	-25°C to +85°C	8 pin Plastic DIP		
ICM7245DIPA	-25°C to +85°C	8 pin Plastic DIP		
ICM7245EIPA	-25°C to +85°C	8 pin Plastic DIP		
ICM7245FIPA	-25°C to +85°C	8 pin Plastic DIP		
ICM7245UIPA	-25°C to +85°C	8 pin Plastic DIP		

DEVICE NUMBER	BIPOLAR/ UNIPOLAR	PULSE WIDTH (ms)	PULSE	OSCILLATOR CAPACITOR
ICM7245A	В	9.7	1Hz	COUT
ICM7245B	В	7.8	1Hz	CIN
ICM7245D	В	7.8	0.1Hz (1 pulse/ 10 seconds)	Cout
ICM7245E	В	7.8	0.0833Hz (1 pulse/ 12 seconds)	CIN
ICM7245F	В	7.8	0.05Hz (1 pulse/ 20 seconds)	CIN
ICM7245U	U	3.9	1Hz	CIN

MOTOR 2 2
MOTOR 1 3
STOP 4

8 OSC OUT

7 OSC IN
6 TEST
5 V-

Figure 1: Pin Configuration (Outline dwg PA)



### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (VDD-VSS)	3.0V
Input Voltages VSS-0.3 < VIN < VDD +	-0.3
Power Dissipation (Note 1)	mW

Storage Temperature	-60°C to +150°C
Operating Temperature	25°C to +85°C
Lead Temperature (Soldering, 10sec)	300°C

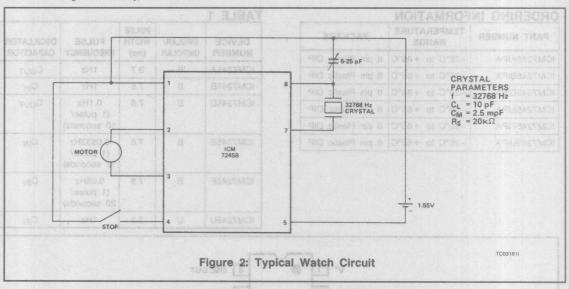
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

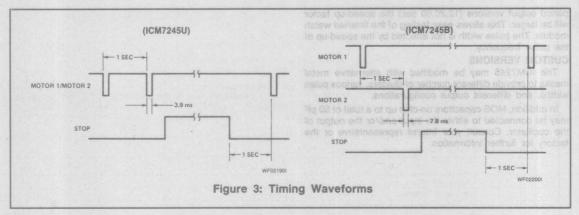
Note 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

# **ELECTRICAL CHARACTERISTICS** ( $V_{DD} = 1.55V$ , $V_{SS} = 0V$ , $f_{OSC} = 32,768Hz$ , circuit in Figure 2, $T_A = 25^{\circ}C$ , unless otherwise stated. Numbers are in absolute values.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD AND AND	Supply Current	No Load	The HOSTAGE	0.4	0.8	μΑ
VSUPPLY	Operating Voltage (VDD-VSS)	0°C < T <sub>A</sub> < 50°C	1.2	CONTRACTOR	1.8	V
9m	Oscillator Transconductance	Start-up (Note 1)	15	re pi med	er adi te	μs
Cosc	Oscillator Capacitance	(Note 1) Propose of Westernburger	16	20	24	pF
ISTOP	STOP Input Current	rieser legic is instituted	nomem.,	toletay ti	0.3	μА
ITEST	TEST Input Current	edi no ealogo "gole"	o terle s	elugi teril	10	μΑ
fSTAB .	Oscillator Stability	$\Delta(V_{SUPPLY}) = 0.6V$	1901 9710	0.1	III. JUKI BUQ	ppm
IDD	Supply Current During Stop	'STOP' Connected to VDD	stalenca !	maino el	1.0	μΑ
Ro	Output Saturation Resistance	Bipolar (N-CH. + P-CH) IL = 1mA	SIZEN INC	tualisa	200	Ω
R <sub>O-P</sub>	Output Saturation Resistance P-CH	Unipolar I <sub>L</sub> = 3mA	ANTES B	BUTTER !	200	Ω
Ro-N	Output Saturation Resistance N-CH	Unipolar I <sub>L</sub> = 3mA	GI Philips	FOR 191102 1	50	Ω

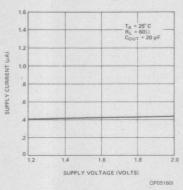
NOTE 1: For design reference only, not 100% tested.



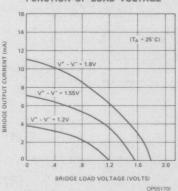


### TYPICAL PERFORMANCE CHARACTERISTICS

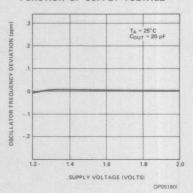




# BRIDGE OUTPUT CURRENT AS A FUNCTION OF LOAD VOLTAGE



# OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



### **APPLICATION NOTES**

### **OSCILLATOR**

The oscillator of the ICM7245 is designed for low frequency operation at very low current from a 1.55 volt supply. The oscillator is of the inverter type, using a nonlinear feedback resistor having maximum resistance under start-up conditions. The nominal load capacitance of the crystal should be less than 12pF, with a preferred range of 7-10pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure start-up and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_{\text{m}}}{2(C_{\text{O}} + C_{\text{L}})}; C_{\text{L}} = \frac{C_{\text{IN}} C_{\text{OUT}}}{C_{\text{IN}} + C_{\text{OUT}}}$$

gm required for start-up

$$g_{\text{m}} = 4\pi 2 f2 \text{ C}_{\text{IN}} \text{ C}_{\text{OUT}} \text{ Rs} \left(1 + \frac{C_{\text{O}}}{C_{\text{L}}}\right)^2$$

where

Rs = Series Resistance of Crystal

f = Frequency of the Crystal

Δf = Frequency Shift from Series Resonance Frequency

CO = Static Capacitance of Crystal

CIN = Input Capacitance

C<sub>OUT</sub> = Output Capacitance

C<sub>I</sub> = Load Capacitance

C<sub>m</sub> = Motional Capacitance of Crystal

The  $g_{\rm m}$  required for start-up calculated should not exceed 50% of the  $g_{\rm m}$  guaranteed for the device.

TEST POINT

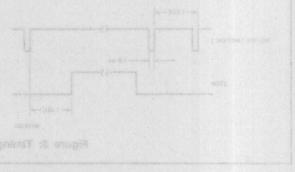
The TEST input, when connected to V<sup>-</sup>, causes the ICM7245B/U to speed-up the outputs by 16 times. On long

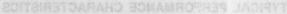
the pulse frequency.

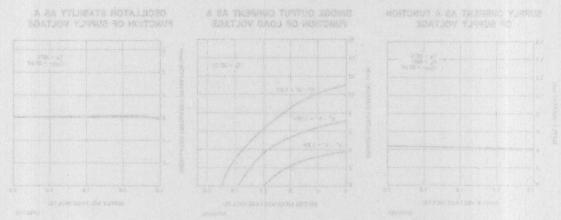
### **CUSTOM VERSIONS**

The ICM7245 may be modified with alternative metal masks to provide different number of dividers, various pulse widths, and different output configurations.

In addition, MOS capacitors on-chip up to a total of 50 pF may be connected to either the input and/or the output of the oscillator. Consult your Intersil representative or the factory for further information.







PPLICA ROW NOTES souls contact the souls contactions of

frequency orientation at very low carried from a 1.55 voll supply. The usualization is of the invertor type, using a non-linear feedback resistor having maximum resistance under swinty conditions. The nominal load palacitance of the crystal should be lead than 120F, with a preferred range of 7-10F. In specifying the crystal, the motional capacitance, with the characteristics of the circuit is insure start up and pocaracteristics of the circuit is insure start up and operation cover a vide voltage range under warslicese.

The tellowing expressions can be used to arrive at a veral especialization.

 $\frac{d}{2(O_0 + O_1)} = \frac{O_{1N} + O_{00T}}{O_{1N} + O_{00T}}$   $= \frac{O_{2N} + O_{2N}}{O_{2N} + O_{2N}} = \frac{O_{2N} + O_{2N}}{O_{2N} + O_{2N}}$   $= \frac{O_{2N}}{O_{2N} + O_{2N}} = \frac{O_{2N}}{O_{2N}} 

The gm required for start-up calculated should no come of the gm gluarenteed for the covice.

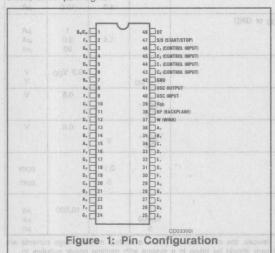
The TEST input, when connected to V° causes the CM726567U to speed-up the outputs by 15 times. On long

# 5½ Digit LCD μ-Power Manage Without Meter 20 Change W

### GENERAL DESCRIPTION

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1 µA during active timing or counting, due to Intersil's special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48-lead device, powered by a single DC voltage source and controlled by a 32.768kHz guartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard LCD segments. The chip is available in dice and in ceramic side-brazed packages.



### **FEATURES**

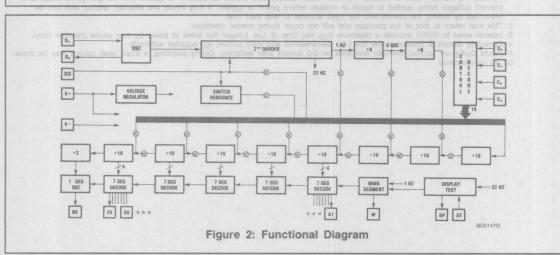
- Hour Meter Requires Only 4 Parts Total
- Micropower Operation: < 1µA at 2.8V Typical
- 10 Year Operation On One Lithium Cell 21/2 Year Battery Life With Display Connected
- Directly drives 5½ Digit LCD
- 14 Programmable Modes of Operation
  - Times Hrs., 0.1 Hrs., .01 Hrs., .1 Mins.
  - Counts 1's, 10's, 100's, 1000's
  - **Dual Funtion Input Circuit:** 
    - Selectable Debounce for Counter
    - High-Pass Filter for Timer
  - Direct AC Line Triggering With Input Resistor
  - Winking "Timer Active" Display Output
  - Display Test Feature

### **APPLICATIONS**

- AC or DC Hour Meters
- AC or DC Totalizers
- Portable Battery Powered Equipment
- Long Range Service Meters

### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7249IDM	-40°C to +85°C	48-Pin Ceramic
ICM7249/D	25°C	Die



# ICM7249



### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage6	V
Input Voltage	
Pins 43-48 (Note 1)(VSS -0.3V) to (VDD +0.3V	/)
Power Dissipation (Note 2) 200ml	N

Operating Temperature Range40°C to	85°C
Storage Temperature Range65°C to 1	50°C
Lead Temperature (Soldering, 10sec)3	00°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Temperature = -40°C to +85°C, VDD = 2.2V to 5.5V, VSS = 0V, unless otherwise noted. Typical specifications measured at temperature = 25°C and VDD = 2.8V unless otherwise noted.

	unts 1's, 10's, 100's, 1000's		solveb ba	DI ent		
SYMBOL	PARAMETER SOUTH AS THE PARAMETER SOUTH AS THE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Operating Voltage	Note 3 bushness avid should	2.2	Lecomps	5.5	V
I <sub>DD</sub>	Operating Current		sidslibvs	1.0	3.0 10.0	μA μA
I <sub>IN</sub> Iss I <sub>DT</sub>	Input Current: Co-C3, S/S DT		min p	1.5	3.0 90	μΑ μΑ μΑ
V <sub>IL</sub> V <sub>IH</sub>	Input Voltage: C <sub>0</sub> -C <sub>3</sub> , DT, S/S		0.7 V <sub>DD</sub>		0.3 V <sub>DD</sub>	V
VoL	Segment Output Voltage	I <sub>OL</sub> = 1μΑ	1 1 2 1		0.8	٧
VOH	T MINISE TEMPERATURE	$I_{OH} = 1\mu A$	V <sub>DD</sub> - 0.8			
V <sub>OL</sub>	Backplane Output Voltage	$I_{OL} = 10\mu A$ $I_{OH} = 10\mu A$	V <sub>DD</sub> - 0.8	٧	0.8	٧
-	Oscillator Stability: Temp. = 25°C, V <sub>DD</sub> = 2.2V to 5.5V Temp. = -40°C to +85°C, V <sub>DD</sub> = 2.2V to 5.5V	NO.	ACIN ACIN ACIN ACIN	0.1	3 4 3	ppm
T <sub>HP</sub> T <sub>DE</sub> T <sub>DE</sub>	S/S Pulse Width: High-pass Filter (Modes 0-3) Debounce (Modes 4, 6, 8, 10) w/o Debounce (Modes 5, 7, 9, 11)		5 10,000 5	100	10,000	μs μs μs

NOTES:

- 1. Due to the SCR structure inherent in junction-isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs or outputs before power is applied. If only inputs are affected, latchup also can be prevented by limiting the current into the input terminal to less than 1mA.
- 2. This limit refers to that of the package and will not occur during normal operation.
- 3. Internal reset to 00000 requires a maximum VDD rise time of 1 µs. Longer rise times at power-up may cause improper reset.
- Operating current is measured with the LCD disconnected and input current ISS supplied externally.
- 5. Inputs C<sub>0</sub>-C<sub>3</sub> are latched internally and draw no DC current after switching. During switching, a 90 μA peak current may be drawn for 10 nanoseconds.

33

34

35

36

D<sub>1</sub>

C<sub>1</sub>

B<sub>1</sub>

A<sub>1</sub>

PIN	NAME	DESCRIPTION	PIN	NAME	DESCR	RIPTION
1	B <sub>6</sub> /C <sub>6</sub>	Half-digit LCD segment output.	37	W	Wink-segment or	utput.
2	F <sub>5</sub>	tomic lawered stones	38	BP	Backplane for Li	CD reference.
3	G <sub>5</sub>	0 ) hour interval tenar	39	V+	Positive supply	voltage.
4	E <sub>5</sub>	nemil levisini suori 10.0	40	OSCI	Quartz Crystal	
5	D <sub>5</sub>	nemit levestri siunim 1.0	41	OSC <sub>O</sub>	connections	0
6	C <sub>5</sub>	eonuodelo rittiw tetriuog s't	42	GND	Chip GRouND.	
7	B <sub>5</sub>	retriugo a'T	43	C <sub>0</sub>	0	
8	A <sub>5</sub>	- onwodeb risk with debound	44	C <sub>1</sub>	Mode-select	
9	F <sub>4</sub>	tetruop e'Of	45	C <sub>2</sub>	control inputs.	
10	G <sub>4</sub>	100's counter with deboun	46	C <sub>3</sub>		86
11	E <sub>4</sub>	Seven-segment	47	S/S	Start / Stop	9
12	D <sub>4</sub>	LCD outputs.	48	DT	Display Test	
13	C <sub>4</sub>	1000's counter				
14	B <sub>4</sub>	Test display digits				
15	A <sub>4</sub>	teat (aduato)				
16	F <sub>3</sub>	last lament				
17	G <sub>3</sub>	Resot				
18	E <sub>3</sub>					
19	D <sub>3</sub>	with an input frequency between 4 ndeterminate effect on the timing.			ESCRIPTION	
20	C <sub>3</sub>	The timing intervals are different				
21	B <sub>3</sub>	example, in Mode 6 the display is in while in Mode 3 the display is incom-				
22	A <sub>3</sub>	atuner				
23	o Fampea	Winile timing is active, the wint-				
24	G <sub>2</sub>	hash, as seen in Figure 1. On the up- the wink output turns off. It remain				
25	E <sub>2</sub>	cycles and turns back on for another				
26	D <sub>2</sub>	titi active, the wink segment repert				
27	C <sub>2</sub>	unis timing begins equin. In counting				
28	B <sub>2</sub>	a registered and latched on each co				
29	A <sub>2</sub>	is counter mode, the display is				
30	F <sub>1</sub>	2월 발생님은 10일 발생님은 10일 시간 10일 10일 10일 10일 10일 10일 10일 10일 10일 10일				
31	G <sub>1</sub>	Jhuod yseve tests				
32	E <sub>1</sub>					

MOITHIRD		Control Pi	n Inputs		DESCRIPTION	BMAN	MIS
Mode	namp <sub>C3</sub> -xintW	C <sub>2</sub> W	C <sub>1</sub>	C <sub>0</sub>	Juquo Inempse GOJ tigil Functio	n <sub>ed Ge</sub>	
LCD regrence	O COLORE	0 48	0	0	1 hour interval timer		18
fagetlov v	dans Ownson	0 + 4	0	1	0.1 hour interval timer	10 ac	. 6
2	Quartz0Crystell	080	108	0	0.01 hour interval timer	. ad	
3	and o sano	0.80	1 1	1	0.1 minute interval timer	аG	
4	divino, 0, divin	13/0	0	0	1's counter with debounce	39	1.0
5	0	1.00	0	1	1's counter	85	
6	rools0-shot	1 19	1 1	0	10's counter with debounce	38	
7	toniro inputs	1 50	1	1	10's counter	17.7	8
8	1	0.80	0	0	100's counter with debounce	, ac)	0
9	Start / Stop	08/8	0	1	100's counter	3.5	
10	Piaplay Test	0 19	481	0	1000's counter with debound	e NO	2
11	1	0	1	1	1000's counter	į,Ū	€
12	1	1	0	0	Test display digits	18	
13	1	1	0	1	Internal test	L.A.	
14	1	1	1	0	Internal test	6-1	1.0
15	1	1	1	1	Reset	69	

### **DETAILED DESCRIPTION**

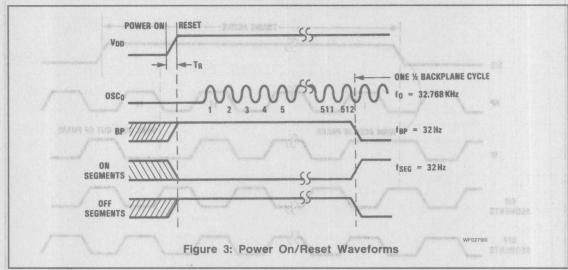
After power is applied, the ICM7249 requires a rise time of  $t_{\rm R}$  to become active and for oscillation to begin, as seen in Figure 3. Initially the backplane output BP is a logic '1' level, but then changes after every 512 crystal oscillation cycles, giving BP a square-wave frequency of 32Hz. Segments are turned off when the voltage levels of the segment drive pins are the same as and in phase with BP. Segments are turned on by having the drive pin voltages out of phase with BP.

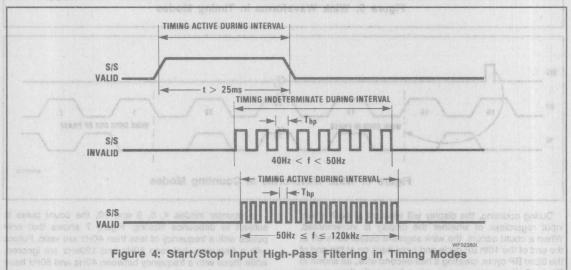
The 16 modes are selected by placing the binary equivalent of the mode number on inputs  $C_0$ – $C_3$  (Table 2). In the four timer modes, timing is controlled by the Start/Stop input S/S. Because of internal high-pass filtering, timing is active when either S/S is held high for more than 25ms, or the input signal has a frequency of at least 50Hz and less than 120kHz as shown in Figure 4. Driving S/S

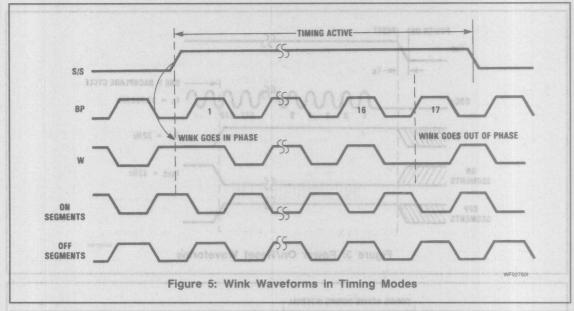
with an input frequency between 40Hz and 50Hz has an indeterminate effect on the timing.

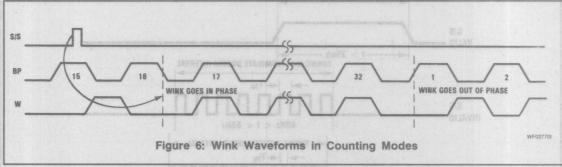
The timing intervals are different for each mode. For example, in Mode 0 the display is incremented every hour, while in Mode 3 the display is incremented every tenth of a minute.

While timing is active, the wink-segment output W will flash, as seen in Figure 1. On the upward transistion of S/S, the wink output turns off. It remains off for 16 backplane cycles and turns back on for another 16 cycles. If timing is still active, the wink segment repeats this process, giving it a flash rate of 1Hz: otherwise the wink output remains on until timing begins again. In counting modes 4-11, the count is registered and latched on each positive transition of S/S. The display is keyed to the specific counting mode. In the 1's counter mode, the display is incremented for each count; in the 10's counter mode, the display is incremented after every count.





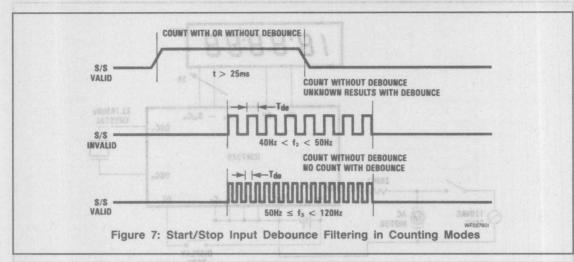


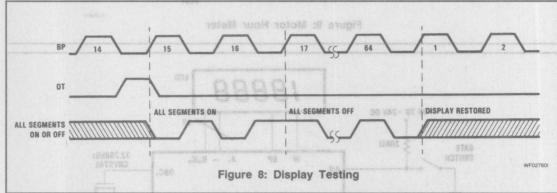


During counting, the display will wink off at each count input regardless of whether the display is incremented. When a count occurs, the wink segment output turns off at the end of the 16th BP cycle and turns back on at the end of the 32nd BP cycle, creating a half-second wink, as shown in Figure 6. If counting occurs more frequently than once a second, the wink output will default to a constant 1Hz flash rate.

In counter modes 4, 6, 8 and 10, the count pulse is subject to debounce filtering. Figure 7 shows that only pulses with a frequency of less than 40Hz are valid. Pulses with a frequency between 50Hz and 120kHz are ignored, while those with a frequency between 40Hz and 50Hz have an indeterminate effect on the count.







The display may be tested at any time without disturbing operation by pulsing DT high, as seen in Figure 8. On the next positive transition of BP, all the segments turn on and remain on until the end of the 16th BP cycle. This takes a half-second or less. All the segments then turn off for an additional 48 BP cycles (the end of the 64th cycle), after which valid data returns to the display. As long as DT is held high, the segments will remain on.

Additional display testing is provided by using mode 12. In this mode each displayed decade is incremented on each positive transition of S/S. Modes 13 and 14 are for manufacturer testing only.

Mode 15 resets all the decades and internal counters to zero, essentially bringing everything back to power-up status.

### **APPLICATION NOTES**

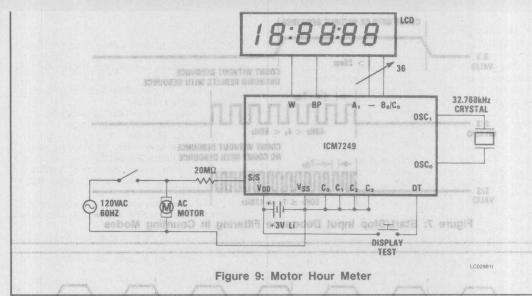
A typical use of the ICM7249 is seen in Figure 9, the Motor Hour Meter. In this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The 20M $\Omega$  resistor and high-pass filtering allow AC line activation of the S/S input. This configuration, which is powered by a 3V

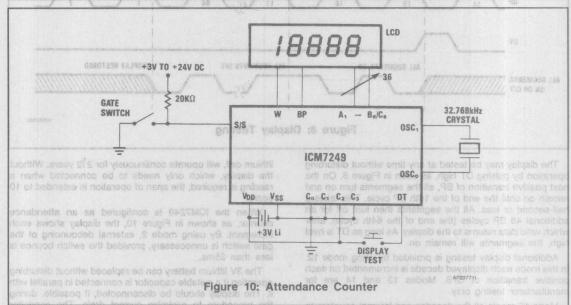
lithium cell, will operate continuously for  $2^{1/2}$  years. Without the display, which only needs to be connected when a reading is required, the span of operation is extended to 10 years.

When the ICM7249 is configured as an attendance counter, as shown in Figure 10, the display shows each increment. By using mode 2, external debouncing of the gate switch is unnecessary, provided the switch bounce is less than 35ms.

The 3V lithium battery can be replaced without disturbing operation if a suitable capacitor is connected in parallel with it. The display should be disconnected, if possible, during the procedure to minimize current drain. The capacitor should be large enough to store charge for the amount of time needed to physically replace the battery ( $\Delta t = \Delta VC/I$ ). A  $10\mu F$  capacitor initially charged to 3V will supply a current of  $1.0\mu A$  for 8 seconds before its voltage drops to 2.2V, which is the minimum operating voltage for the ICM7249.

Before the battery is removed, the capacitor should be placed in parallel, across the  $V_{DD}$  and GND terminals. After the battery is replaced, the capacitor can be removed and the display reconnected.





should be large enough to store charge for the amount of time needed to physically replace the battery ( $\Delta t = \Delta VC$ ). A 10 $\mu$ F capacitor initially charged to 3V will supply a current of 1.0 $\mu$ A for 8 seconds before its voltage drops to the minimum operating voltage for the

Before the battery is removed, the capacitor should be placed in parallel, across the Vog and GND reminets. After the battery is replaced, the capacitor can be removed and the display reconnected.

### APPLICATION MOTES

A typical use of the ICM7249 is seen in Figure 9, the Motor Hour Meter, in this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The 20M30 resistor and high-cass riftening allow AC line activation of the S/S input. This configuration, which is powered by a SV.

# GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIG-GER and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLT-AGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V + and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

### ORDERING INFORMATION

PART NUMBER	TEMPERATURE	PACKAGE
ICM7555CBA ICM7555IPA ICM7555ITV ICM7555MTV* ICM7556IPD ICM7556MJD*	0°C to +70°C -25°C to +85°C -25°C to +85°C -55°C to +125°C -25°C to +85°C -55°C to +125°C	8 Lead S.O.I.C. 8 Lead MiniDip TO-99 Can TO-99 Can 14 Lead Plastic DIP 14 Lead CERDIP
ICM7555/D ICM7556/D	三	DICE**

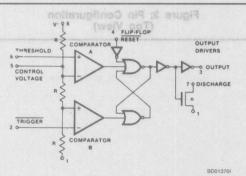
\*Add /883B to part number if 883B processing is desired.

### **FEATURES**

- Exact Equivalent in Most Cases for SE/NE555/ 556 or TLC555/556
- Low Supply Current 60 µA Typ. (ICM7555) 120µA Typ. (ICM7556)
- Extremely Low Trigger, Threshold and Reset Currents - 20pA Typical
- High Speed Operation 1MHz Typical
- Wide Operation Supply Voltage Range Guaranteed 2 to 18 Volts
- Normal Reset Function No Crowbarring of Supply During Output Transition
- Can Be Used With Higher Impedance Timing Elements Than Regular 555/6 for Longer RC **Time Constants**
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Output Source/Sink Driver Can Drive TTL/
- Typical Temperature Stability of 0.005% Per °C at 25°C
- Outputs Have Very Low Offsets, HI and LO

### APPLICATIONS BANAGE BALLETOO

- **Precision Timing**
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- **Pulse Position Modulation**
- Missing Pulse Detector



This Functional Diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.  $R = 100k\Omega$ ,  $\pm 20\%$  typ.

Figure 1: Functional Diagram

<sup>\*\*</sup>Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.

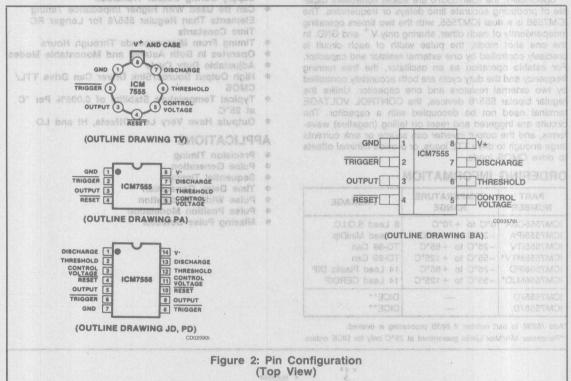
# ICM7555/ICM7556

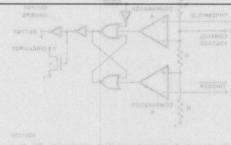
### ABSOLUTE MAXIMUM RATINGS

Supply VoltageInput Voltage: Trigger,	+ 18 Volts
Control Voltage, Threshold, ≤ V + + 0.3	3V to $\geq V^ 0.3V$
Output Current	O VIGGE 100mA
Power Dissipation <sup>[2]</sup> ICM7556	300mW
Storage Temperature	
Lead Temperature (Soldering, 10sec) .	+300°C

Operating Temperature Range <sup>[2]</sup>	25°C to +85°C
ICM7555ITV	AND STREET OF THE STREET, SAN ASSESSMENT OF THE STREET, SAN ASSESS
ICM7556IPD	25°C to +85°C
ICM7555MTV	55°C to +125°C
ICM7556MJD	
netude low supply current, wide	

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





ELECTRICAL CHARACTERISTICS ICM7555 TA = 25°C, unless otherwise specified.

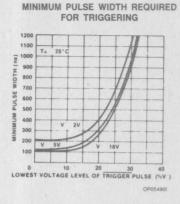
SYMBOL	PARAMETER	TEST CONDITIONS	BRITALAG	MIN	TYP	MAX	UNIT
Au 000	Static Supply Current	T <sub>A</sub> = -55°C to 125°C V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V	Manul	uppiy (	40 60	200 300	μΑ μΑ
30	Monostable Timing Accuracy	RA = 10k, C = $0.1\mu$ F V <sub>DD</sub> = 5V	YORWAYOA DISE	all elds	2		%
5°\maq 9°\maq 9°\maq	Drift with Temp*	T <sub>A</sub> = -55 to 125°C V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		into T d	150 200 250		ppm/°( ppm/°( ppm/°(
THE STREET	Drift with Supply*	V <sub>DD</sub> = 5 to 15V		200	0.5		%/V
230	Astable Timing Accuracy	$RA = RB = 10k, C = 0.1 \mu F, V_{DD} = 5V$		Vernilla S	2		%
orlanda Orlanda Orlanda	Drift with Temp*	T <sub>A</sub> = -55°C to 125°C V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		h Tem	150 200 250		ppm/°0 ppm/°0 ppm/°0
	Drift with Supply*	V <sub>DD</sub> = 5 to 15V			0.5	-	%/V
VTH	Threshold Voltage	V <sub>DD</sub> = 15V		Market Box	67	· Special Control	% VDI
VTRIG	Trigger Voltage	V <sub>DD</sub> = 15V		and the same	- 32	-	% VD
ITRIG	Trigger Current	V <sub>DD</sub> = 15V				10	nA
I <sub>TH</sub>	Threshold Current	V <sub>DD</sub> = 15V				10	nA
Vcv	Control Voltage	V <sub>DD</sub> = 15V		S OR OV	67	-	% VDI
VRST	Reset Voltage	V <sub>DD</sub> = 2 to 15V		0.4	10000	1.0	V
<sup>1</sup> RST	Reset Current	V <sub>DD</sub> = 15V		Locara		10	nA
IDIS	Discharge Leakage	V <sub>DD</sub> = 15V		la a la an		10	nA
V <sub>OL</sub>	Output Voltage Drop	V <sub>DD</sub> = 15V I <sub>sink</sub> = 20mA V <sub>DD</sub> = 5V I <sub>sink</sub> = 3.2mA	qosi	Voltage	0.4	1.0	V V
VOH	Output Voltage Drop	V <sub>DD</sub> = 15V l <sub>source</sub> = 0.8mA V <sub>DD</sub> = 5V l <sub>source</sub> = 0.8mA	Drop	14.3	14.6		V V
V <sub>DIS</sub>	Discharge Output Voltage Drop	V <sub>DD</sub> = 5 to 15V	od opanov su	two eg	0.2	0.4	٧
V +	Supply Voltage*	Functional Oper.		2.0		18.0	٧
tR	Output Rise Time*	RL = 10M, CL = 10pF, V <sub>DD</sub> = 5V	*80	7 pair	75		ns
t <sub>E</sub> n	Output Fall Time*	RL = 10M, CL = 10pF, V <sub>DD</sub> = 5V	1	of its	75		ns
fMAX	Oscillator Frequency*	V <sub>DD</sub> = 5V RA = 470ohm, RB = 270ohm C =	200pF		1	-	MHz

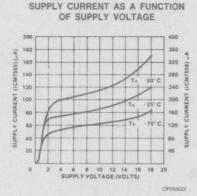
<sup>\*</sup> This parameter not tested. The majority of all parts meet this specification.

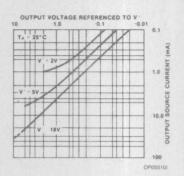
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
140 006	Static Supply Current	T = -55°C to 125°C V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V	AP VIGEO	80 120	400 600	μΑ μΑ
	Monostable Timing Accuracy	$RA = 10k, C = 0.1 \mu F$ $V_{DD} = 5V$	810	2		%
9°\maq 9°\maq maq	Drift with Temp*	T = -55 to 125°C VDD = 5V VDD = 10V VDD = 15V	mer	150 200 250		ppm/°C ppm/°C ppm/°C
and the same of th	Drift with Supply*	V <sub>DD</sub> = 5 to 15V	Addres t	0.5		%/V
	Astable Timing Accuracy	$RA = RB = 10k$ , $C = 0.1 \mu F$ , $V_{DD} = 5V$	CLEARIN	2		%
2"\ragg 2"\ragg 2"\ragg	Drift with Temp*	T = -55°C to 125°C V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	pans i a	150 200 250		ppm/°C ppm/°C
	Drift with Supply*	V <sub>DD</sub> = 5 to 15V	leading t	0.5	J.	% V
VTH	Threshold Voltage	V <sub>DD</sub> = 15V	DIDY G	67	- Internal A	% VDD
VTRIG	Trigger Voltage	V <sub>DD</sub> = 15V.	PIPERIOY	32		% VDD
ITRIG	Trigger Current	V <sub>DD</sub> = 15V	DOLLA	reogn	10	nA
Ітн	Threshold Current	V <sub>DD</sub> = 15V	BALL ES	HERENT!	10	nA
Vcv	Control Voltage	V <sub>DD</sub> = 15V	HORHOY	67		% VDD
VRST	Reset Voltage	V <sub>DD</sub> = 2 to 15V	0.4	19897	1.0	V
IRST	Reset Current	V <sub>DD</sub> = 15V	3223117	78297	10	nA
IDIS	Discharge Leakage	V <sub>DD</sub> = 15V	MED N	SE SON	10	nA
VOL	Output Voltage Drop	V <sub>DD</sub> = 15V   <sub>sink</sub> = 20mA V <sub>DD</sub> = 5V   <sub>sink</sub> = 3.2mA	apenov	0.4	1.0	V V
Voн	Output Voltage Drop	V <sub>DD</sub> = 15V  source = 0.8mA V <sub>DD</sub> = 5V  source = 0.8mA	14.3	14.6		V
V <sub>DIS</sub>	Discharge Output Voltage Drop	V <sub>DD</sub> = 5 to 15V I <sub>sink</sub> = 15mA	APUC 61	0.2	0.4	٧
V +	Supply Voltage*	Functional Oper.	2.0	BIR AND	18.0	V
t <sub>R</sub>	Output Rise Time*	RL = 10M, CL = 10pF, V <sub>DD</sub> = 5V	T Gen	75		ns
tF	Output Fall Time*	RL = 10M, CL = 10pF, V <sub>DD</sub> = 5V	111 115	75		ns
fMAX	Oscillator Frequency*	V <sub>DD</sub> = 5V RA = 470ohm, RB = 270ohm C = 200pF	1 20 17 30	1		MHz

<sup>\*</sup> This parameter not tested. The majority of all parts meet this specification.

### TYPICAL PERFORMANCE CHARACTERISTICS





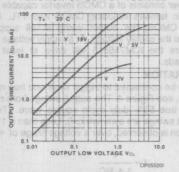


OUTPUT SOURCE CURRENT AS A

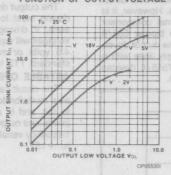
**FUNCTION OF OUTPUT VOLTAGE** 

# TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

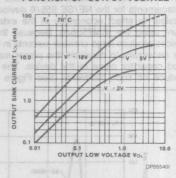
**OUTPUT SINK CURRENT AS A** FUNCTION OF OUTPUT VOLTAGE



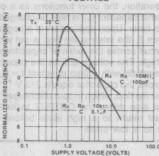
**OUTPUT SINK CURRENT AS A** FUNCTION OF OUTPUT VOLTAGE



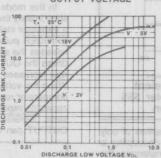
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



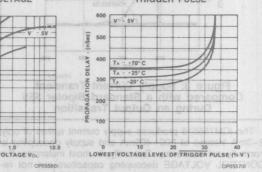
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



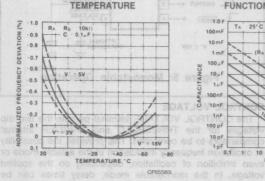
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE **OUTPUT VOLTAGE** 



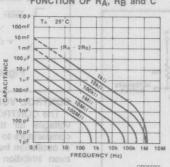
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



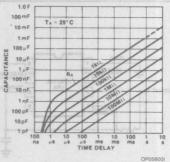
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF



FUNCTION OF RA, RB and C



FREE RUNNING FREQUENCY AS A TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C



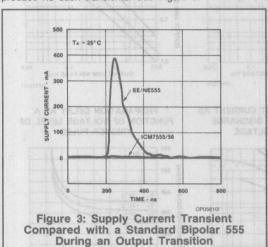
# ICM7555/ICM7556

# **WINTERSIL**

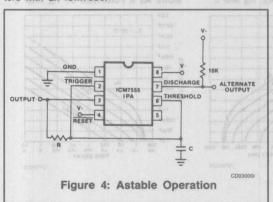
### **APPLICATION NOTES**

### GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 3.



The ICM7555/6 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.



### POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. There-

fore, use high values for R and low values for C in Figures 4 and 5.

### **OUTPUT DRIVE CAPABILITY**

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

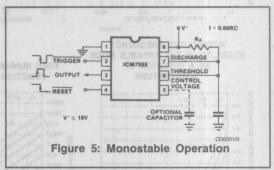
### ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4 \text{ RC}}$$

### MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative TRIGGER pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant  $t=R_AC$ . When the voltage across the capacitor equals 2/3 V  $^+$ , the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. TRIGGER must return to a high state before the OUTPUT can return to a low state.



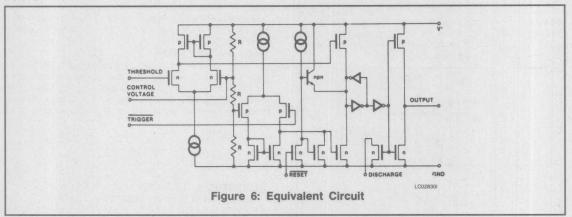
### CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

### RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the RESET

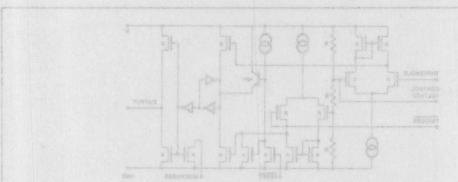
function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.



### TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
> 2/3(V <sup>+</sup> )	> 1/3(V <sup>+</sup> )	HIGH	LOW	ON
V <sub>TH</sub> < 2/3	V <sub>TR</sub> > 1/3	HIGH	STABLE	STABLE
DON'T CARE	< 1/3(V <sup>+</sup> )	HIGH	HIGH	OFF

NOTE: RESET will dominate all other inputs: TRIGGER will dominate over THRESHOLD.



		TRIGGER	
			BRAD TIMES
	HOH	(*V)C\1 <	
		Vrg > 1/3	



# Section 8 — Display Drivers

Section 8 - Display Drivers

# ICM7211/12 4-Digit LCD/LED Display Driver



### GENERAL DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive commonanode LED displays, providing 28 current-controlled, low leakage, open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7211/D		DICE
ICM7211M/D		DICE
ICM7211AIJL	-40°C to +85°C	40 Pin CERDIP
ICM7211AMIJL	-40°C to +85°C	40 Pin CERDIP
ICM7211IJL	-40°C to +85°C	40 Pin CERDIP
ICM7211IPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AMIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211MIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211MIJL	-40°C to +85°C	40 Pin CERDIP
ICM7211AEV/KIT		EVALUATION KIT
ICM7212/D		DICE

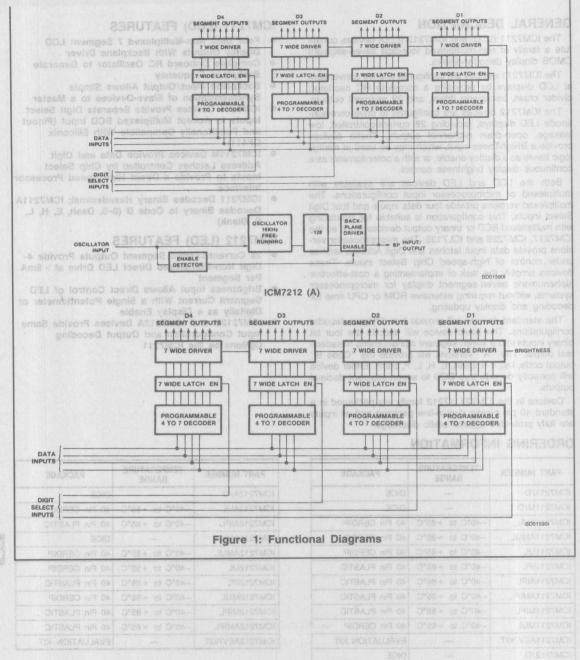
### ICM7211 (LCD) FEATURES

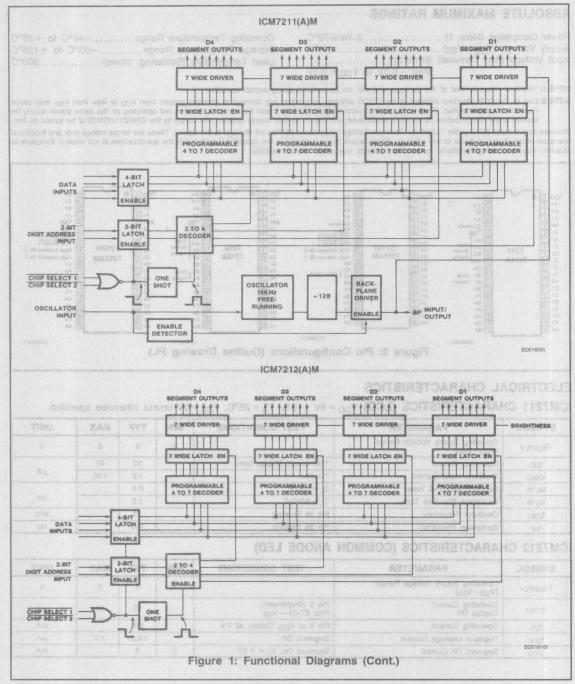
- Four Digit Non-Multiplexed 7 Segment LCD
   Display Outputs With Backplane Driver
- Complete Onboard RC Oscillator to Generate
   Backplane Frequency
- Backplane Input/Output Allows Simple
   Synchronization of Slave-Devices to a Master
- ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible With Siliconix DF411)
- ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface
- ICM7211 Decodes Binary Hexadecimal; ICM7211A Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)

### ICM7212 (LED) FEATURES

- 28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at > 5mA Per Segment
- Brightness Input Allows Direct Control of LED Segment Current With a Single Potentiometer or Digitally as a Display Enable
- ICM7212M and ICM7212A Devices Provide Same Input Configuration and Output Decoding Options as the ICM7211

PART NUMBER	TEMPERATURE RANGE	PACKAGE	
ICM7212A/D		DICE	
ICM7212AIJL	-40°C to +85°C	40 Pin CERDIP	
ICM7212AIPL	-40°C to +85°C	40 Pin PLASTIC	
ICM7212AM/D	-	DICE	
ICM7212AMIJL	-40°C to +85°C	40 Pin CERDIP	
ICM7212IJL	-40°C to +85°C	40 Pin CERDIP	
ICM7212IPL	-40°C to +85°C	40 Pin PLASTIC	
ICM7212MIJL	-40°C to +85°C	40 Pin CERDIP	
ICM7212MIPL	-40°C to +85°C	40 Pin PLASTIC	
ICM7212AMIPL	-40°C to +85°C	40 Pin PLASTIC	
ICM7212AEV/KIT	_	EVALUATION KIT	





# ICM7211/12



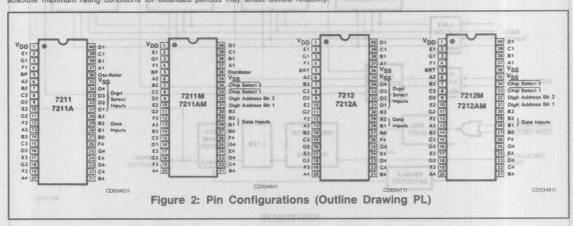
### **ABSOLUTE MAXIMUM RATINGS**

Power Dissipation (Note 1)	Operating Temperature Range40°C to +85°C Storage Temperature Range55°C to +125°C Lead Temperature (Soldering, 10sec)300°C
Voc 03V to Voc + 03V	Lead Temperature (Soldering, Tosec)

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than VDD or less than VSS may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



### **ELECTRICAL CHARACTERISTICS**

ICM7211 CHARACTERISTICS (LCD) VDD = 5V ±10%, TA = 25°C, VSS = 0V unless otherwise specified.

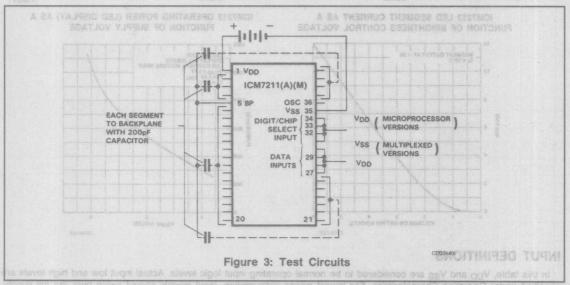
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUPPLY	Operating Supply Voltage Range (VDD - VSS)		3	5	6	٧
IDD	Operating Current	Test circuit, Display blank	- Value and a second	10	50	
losci	Oscillator Input Current	Pin 36	-Libertalian	±2	±10	μΑ
t <sub>R</sub> , t <sub>F</sub>	Segment Rise/Fall Time	C <sub>L</sub> = 200pF	0000 1 01 a 1	0.5		
t <sub>R</sub> , t <sub>F</sub>	Backplane Rise/Fall Time	C <sub>L</sub> = 5000pF	Insurance or page	1.5		μs
fosc	Oscillator Frequency	Pin 36 Floating		19	17	kHz
fBP	Backplane Frequency	Pin 36 Floating		150	A STATE OF THE PARTY OF THE PAR	Hz

### ICM7212 CHARACTERISTICS (COMMON ANODE LED)

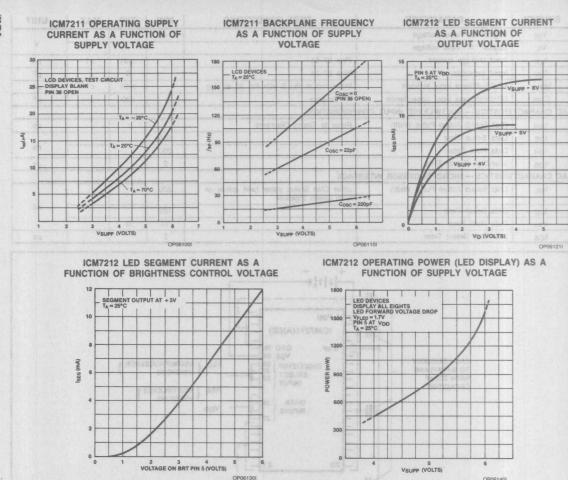
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>SUPPLY</sub> Operating Supply Voltage Range (V <sub>DD</sub> – V <sub>SS</sub> )			4	5	6	V	
ISTBY Operating Current Display Off		Pin 5 (Brightness), Pins 27–34 — VSS	L	10	50	μА	
IDD Operating Current Pin 5 at VDD, Display		Pin 5 at V <sub>DD</sub> , Display all 8's	LL	200		mA	
I <sub>SLK</sub> Segment Leakage Current		Segment Off	and the	±0.01	±1	μΑ	
ISEG	Segment On Current	Segment On, VO = +3V	5	8		mA	

### INPUT CHARACTERISTICS (ICM7211 AND ICM7212) HRETOARARO BOMAMRORRES DADISTT

SYMBOL	PARAMETER VO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH	Logical "1" input voltage	AS A FUNCTION OF SUPPLY	10410	DIRECT A	SA THE	RUD
VIL	Logical "0" input voltage	SOALIOV		BALLIOY	Solber	V
lilk	Input leakage current	Pins 27-34		±.01	±1 (	μА
CIN	Input capacitance	Pins 27–34		5		pF
IBPLK	BP/Brightness input leakage	Measured at Pin 5 with Pin 36 at VSS		±.01	± 1000.20	μА
CBPI	BP/Brightness input capacitance	All Devices		200		pF
AC CHARACT	TERISTICS - MULTIPLEXED INPUT COI	NFIGURATION	-			
twH	Digit Select Active Pulse Width	Refer to Timing Diagrams	1			μs
tos	Data Setup Time		500			
tDH	Data Hold Time	1700 1701	200	NA.		ns
tiDS	Inter-Digit Select Time	<b>建新创建的</b> 《范围制建设保证》	2	MAN		μs
AC CHARACT	TERISTICS - MICROPROCESSOR INTER	RFACE				
twL	Chip Select Active Pulse Width	other Chip Select either held active, or both driven together	200		86	
tos	Data Setup Time		100			ns
tDH	Data Hold Time		10	0		
tics	Inter-Chip Select Time	(KODI) esuga	2	(INTADA) N	WAY TO THE	μs



		TUSH	
	Onds (Least Significant)	Vgp = Logicat One Vgs = Logical Zero	96
		Vpp = Logical One Vpp = Logical Zero	
	Oscillator imput Disables SP output devices, allow	Floating or extr. so- ternal capacitor to Vpp Vpc	(LOD Dayloes Only)



### INPUT DEFINITIONS

In this table, VDD and VSS are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

OP06140I

INPUT	TERMINAL	TEST CONDITIONS	FUNCTION			
B0	27	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Ones (Least Significant)			
B1	28	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Twos	Data Input Bits		
B2	29	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Fours			
B3	30	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Eights (Most significant)			
OSC (LCD Devices Only)	36	Floating or with ex- ternal capacitor to V <sub>DD</sub>	Oscillator input			
Vss Disables BP output devices, allo synchronized to an external sign		ing segments to be input at the BP terminal (Pin 5)				

	INPUT	TERMINAL	TEST CONDITIONS	ad yen yoneuped FUNCTION on on now earl notalised
D1	8838	31	2 (2002-0300)	D1 Digit Select (Least significant) PTI 2 A PT
D2		32	V <sub>DD</sub> = Active V <sub>SS</sub> = Inactive	D2 Digit Select
D3		33		D3 Digit Select benset it nevelbrovo ad oals year notalizad on?
D4		34		D4 Digit Select (Most significant)

### ICM7211M/ICM7212M MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	TEST CONDITIONS	neewind Judni Tulian Jol FUNCTION TO YO SHOD SO HAD BIC
DA1	Digit Address Bit 1 (LSB)	31 MTAGUO	V <sub>DD</sub> = Logical One	DA1 & DA2 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4
DA2	Digit Address Bit 2 (MSB)	32	V <sub>SS</sub> = Logical Zero	DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
CS1	Chip Select 1	33	Vnn = Inactive	When both CS1 and CS2 are taken low, the data at the Data
CS2	Chip Select 2		V <sub>SS</sub> = Active	and Digit Select code inputs are written into the input latches.  On the rising edge of either Chip Select, the data is decoded and written into the output latches.

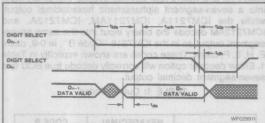


Figure 4: Multiplexed Input Timing Diagram

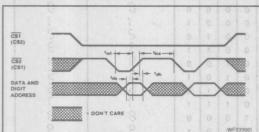


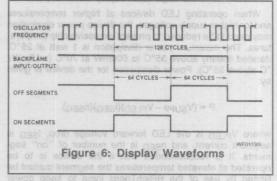
Figure 5: Microprocessor Interface Input Timing Diagram

### DESCRIPTION OF OPERATION LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to VSS. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 onehalf-inch characters. It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2 µs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures. depending on the display used.



The onboard oscillator is designed to free run at approximately 19kHz at microampere power levels. The oscillator 8

frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and Vpp.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above Vss). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

#### LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit, seven-segment common-anode LED displays. These devices include 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain, n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for ''on'' segments, and thus directly modulates the transistor's ''on'' resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 7. The potentiometer should be a high value (100K $\Omega$  to 1M $\Omega$ ) to minimize power consumption, which can be significant when the display is off.

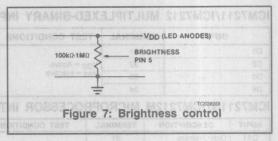
The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED devices have two connections for V<sub>SS</sub>; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (-15mW/°C above 35°C). Power dissipation for the device is given by:

#### P = (VSUPP - VFLED)(ISEG)(nSEG)

where V<sub>FLED</sub> is the LED forward voltage drop, I<sub>SEG</sub> is segment current, and n<sub>SEG</sub> is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.



# INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211MI (CM7212, and ICM7212MI devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AMI decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E. H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

TABLE 1: Output Codes

BINARY				BINARY HEXADECIMAL					
ВЗ	B2	B1	80	ICM7235M	ICM7235A ICM7235AM				
0	0	0	0	0	0				
0	0	0	1	1	1				
0	0	1	0	5	3				
0	0	1	1	j.	3				
0	1	0	0	4	4				
0	1	0	1	5	5				
0	1	1	0	8	5				
0	1	1	1	7	7				
1	0	0	0	8	8				
1	0	0	1	9	9				
1	0	1	0	oroproquesor I	M to singly				
1	0	1	1	6	8				
1	1	0	0	E	Н				
1	1	0	DIC	OF OPERATE	HOLLHON				
1	1	1	0	E	and Pan				
1	1	1	1	F	(BLANK)				

TB000701

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For large quantity orders custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level

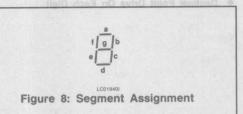
ICM7211/12

decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30.

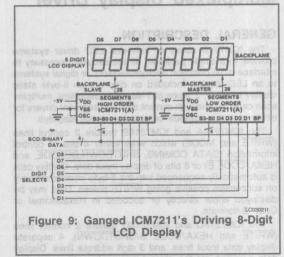
The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

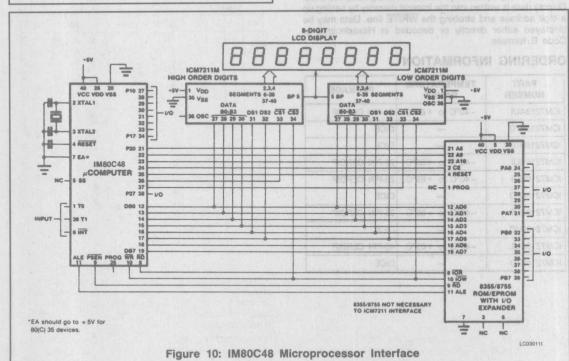
In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

An address of 00 writes into D4, DA2 = 0, DA1 = 1 writes into D3, DA2 = 1, DA1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 5, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.



#### **APPLICATIONS**





8-9

## Multiplexed Display Driver

#### GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, 2 types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7218A and ICM7218B feature 2 control lines (WRITE and MODE) which write either 4 bits of control information (DATA COMING, SHUTDOWN, DECODE, and HEXA/CODE B) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going WRITE pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7218C and ICM7218D feature 2 control lines (WRITE and HEXA/CODE B/SHUTDOWN), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the WRITE line low. Only Hexadecimal and Code B formats are available for display outputs.

The ICM7218E provides 4 input lines for control information (WRITE, HEXA/CODE B, DECODE and SHUTDOWN), 8 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the WRITE line. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

#### FFATURES are of behavior are as a selection of the

- Microprocessor Compatible C. D. E Versions
- Total Circuit Integration On Chip Includes:
- a) Digit and Segment Drivers of TAC semble for
- b) All Multiplex Scan Circuitry
  - d) 7 Segment Hexadecimal and Code B

    Decoders (Pin Selectable)
- Output Drive Suitable for Large LED Displays
- Common Anode and Common Cathode Versions
- Single 5 Volt Supply Required
- Data Retention to 2 Volts Supply
- Shutdown Feature Turns Off Display and Puts Chip Into Low Power Dissipation Mode
- Sequential and Random Access Versions
- Decimal Point Drive On Each Digit

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7218AIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218A/D	American property	DICE
ICM7218B/D	AN ALIE	DICE
ICM7218BIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218CIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218C/D		DICE
ICM7218DIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218D/D	202 07 0	DICE
ICM7218EIJL	-40°C to +85°C	40-PIN CERDIP
ICM7218E/D	-	DICE

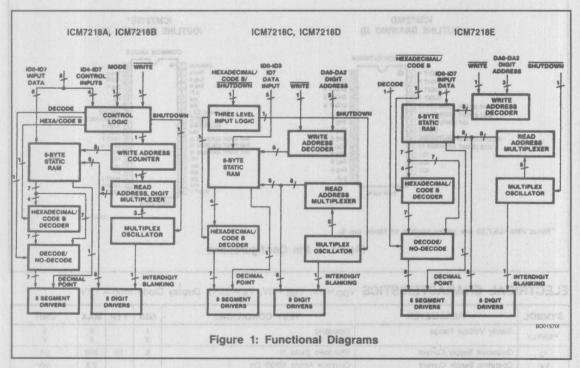
#### ABSOLUTE MAXIMUM RATINGS

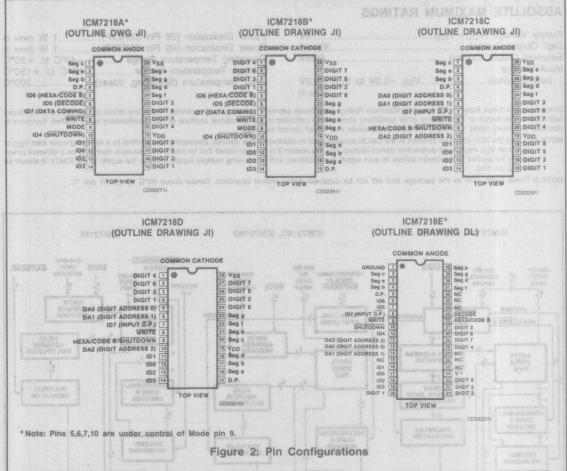
Supply Voltage (VDD - VSS)	6V	Power Dissipation
Digit Output Current		Power Dissipation
Segment Output Current		Operating Tempera
Input Voltage		Storage Temperatu
(any terminal)VSS -0.3	V to $V_{DD} + 0.3V$	Lead Temperature
Total life Table Name of Tables Agents  (Note 1)		

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V<sub>DD</sub> or less than V<sub>SD</sub> may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.





## ELECTRICAL CHARACTERISTICS VDD = 5V, VSS = 0V, TA = 25°C, Display Diode drop = 1.7V

SYMBOL	PARAMETER	TEST CONDITI	MIN	TYP	MAX	UNIT	
VSUPPLY	Supply Voltage Range	Operating Power Down Mode	mpi3	4 2		6	V
la	Quiescent Supply Current	Shutdown (Note 3)		6	10	300	μΑ
IDD	Operating Supply Current	Common Anode SEGS On SEGS Off Common Cathode SEGS On SEGS Off Note 4	Outputs Open Circuit			2.5 500 700 250	mA μA μA μA
IDIG	Digit Drive Current	Common Anode V <sub>out</sub> = V <sub>DD</sub> -2.0V Common Cathode V <sub>out</sub> = V <sub>SS</sub> +1.0V			200		mA mA
I <sub>DLK</sub>	Digit Leakage Current	Shutdown Mode Common Anode V <sub>out</sub> = 2V Common Cathode V <sub>out</sub> = 5V				100 100	μΑ μΑ
ISEG	Peak Segment Drive Current	Common Anode Vout = VSS + Common Cathode Vout = VDD	20 -10	40 -20		mA mA	
ISLK	Segment Leakage Current	Shutdown Mode Common Anode V <sub>out</sub> = V <sub>DD</sub> Common Cathode V <sub>out</sub> = V <sub>SS</sub>			100 100	μΑ μΑ	
fmux	Display Scan Rate	Per Digit			250	185	Hz

#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	PARAMETER	TEST CONDITI	ONS JAMMARET	MIN	TYP	MAX	UNIT
VIH VIF VIL ZIN	Three Level Input: Pin 9 ICM7218C/D Logical "1" Input Voltage Floating Input Logical "0" Input Voltage Three Level Input Impedance	Hexadecimal Code B Shutdown Note 3	© 01	4.5 2.0	100	3.0 0.4	V V V kΩ
V <sub>I</sub> H V <sub>I</sub> L	Logical "1" Input Voltage Logical "0" Input Voltage	rigin	33	3.5		0.8	V
t <sub>WL</sub>	Write Pulse Width (Low)	7218A, B		550	400		ns
twL	Write Pulse Width (Low)	7218C, D, E		400	250		ns
tмн	Mode Hold Time	7218A, B	C+ S+ C+	150			SANS GAG
tms	Mode Set Up Time	7218A, B		500		1871	ns
tps	Data Set Up Time		9,7,17,187,00,30	500			ns
tDH	Data Hold Time	7218 A,B 7218 C,D,E		50 125			ns ns
t <sub>AS</sub>	Digit Address Set Up Time Digital Address Hold Time	ICM7218C, D, E ICM7218C, D, E		500 0			ns ns
ZIN	Data Input Impedance	5-10 pF Gate Capacitance	497	A-81 - 64	1010		Ohms

# TABLE 1: INPUT DEFINITIONS ICM7218A and B

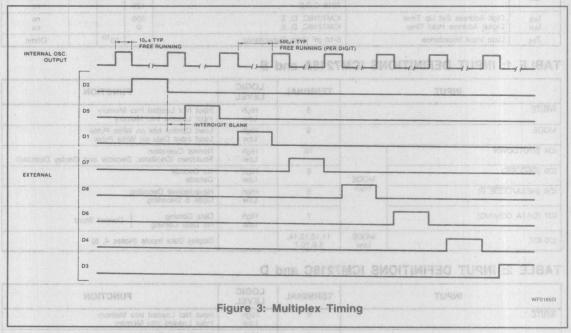
INPUT	TERMINAL	LOGIC	FUNCTION			
WRITE		8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory		
MODE		9	High Low	Load Control bits on Write Pulse Load Input Data on Write Pulse		
ID4 SHUTDOWN		10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Display Disabled)		
ID5 (DECODE)	MODE	6	High Low	No Decode Decode		
ID6 (HEXA/CODE B)	High	5	High Low	Hexadecimal Decoding Code B Decoding		
ID7 (DATA COMING)	1	7	High Low	Data Coming No Data Coming Control Word		
ID0-ID7	MODE Low	11,12,13,14, 5,6,10,7		Display Data Inputs (Notes 4, 5)		

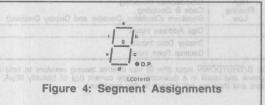
#### TABLE 2: INPUT DEFINITIONS ICM7218C and D

TIMPUT	TERMINAL	LOGIC LEVEL	FUNCTION
WRITE	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
HEXA/CODE B/SHUTDOWN	9 (Note 3)	High Floating Low	Hexadecimal Decoding Code B Decoding Shutdown (Oscillator, Decoder and Display Disabled)
DAO - DA2 amplied as attrofulo entrino vision	10,6,5	FIRST LEFT	Digit Address Inputs
ID0, -ID3 ID (INPUT D.P.) SQLAGI EQI EQI VQI	14,13,11,12 7		Display Data Inputs Decimal Point Input

NOTE 3: In the ICM7218C and D (random access versions) the HEXA/CODE B/SHUTDOWN Input (Pin 9) has internal biasing resistors to hold it NOTE 3: In the ICM7218C and D (random access versions) the HEXA/CODE B/SHUTDOWN Input (Pin 9) has internal biasing resistors to hold it at V<sub>DD/2</sub> when Pin 9 is open circuited. These resistors consume power and result in a quiescent supply current (I<sub>Q</sub>) of typically 50μA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.
 NOTE 4: ID0-ID3 = Don't care when writing control data ID4-ID6 = Don't care when writing Hex/Code B data (The display blanks on ICM7218A/B versions when writing in data)
 NOTE 5: In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents an "on" segment, (i.e. segment, are positive true, decimal point is negative true).
 NOTE 6: Common Anode segment drivers and Common Cathode Digit Drivers have 20kΩ pullup resistors.

	design.		LEVEL	IONOTION
WRITE		9	High Low	Input Latches Not Updated Input Latches Updated
SHUTDOWN	300	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
DECODE		33	High Low	No Decode Decode
HEXA/CODE B	850	004 32	High Low OBIST	Code B Decoding Hexadecimal Decoding
DA0 - DA2 Digit Address (0,1,2)	12.2	13,14,12	7218A, B	Digit Address Inputs
IDO – ID6 ID7 (INPUT D.P.)		17,16,18,19,11,7,6 8		Display Data Inputs (Note 5) Display Data/Decimal Point Input





# DECODE Operation

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary code plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

The 7 segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data:

ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: D.P. a b c e g f d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "zero" represents an "on" segment.

#### HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (-), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

A Second	Deci- mal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	HEXA CODE	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
Section of the second	CODE B	0	1	2	3	4	5	6	7	8	9	-	E	Н	L	P	(BLANK)

#### SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically  $10\mu A$  at  $V_{DD}=5V$ ), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown — only the display output sections of the device are disabled in this mode.

#### Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2 volts without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4 volts.

#### **Output Drive**

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With segment peak drive current of 40mA typically, this results in 5mA average drive. The common cathode drive capability is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

#### Inter Digit Blanking

A blanking time of approximately  $10\mu s$  occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

#### **Driving Larger Displays**

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drives together to drive a 4 digit display, 5mA average segment drive current can be obtained.

#### **Power Dissipation Considerations**

Assuming common anode drive at V<sub>DD</sub> = 5 volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will therefore be 640mW, rising to about 900mW, for all '8' 's displayed. Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.

# Sequential Addressing Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and WRITE low. The instructions occur on 4 lines and are — DECODE/no Decode, type of Decode (if desired), SHUTDOWN/no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going WRITE pulse. After all 8 digit memory locations have been written to, additional transitions of the WRITE input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

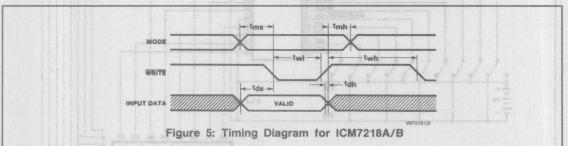
# Random Access Input Drive Considerations (ICM7218C/D/E)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the WRITE pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the WRITE pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 7).

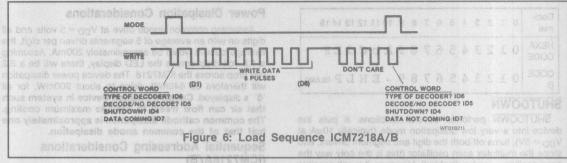
#### **Supply Capacitor**

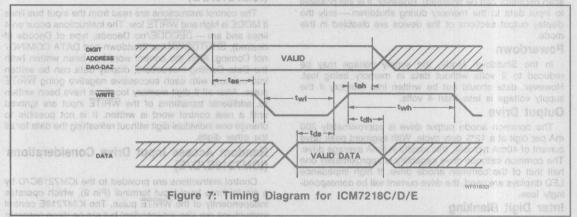
A  $0.1\mu F$  capacitor is recommended between  $V_{DD}$  and  $V_{SS}$  to bypass multiplex noise.

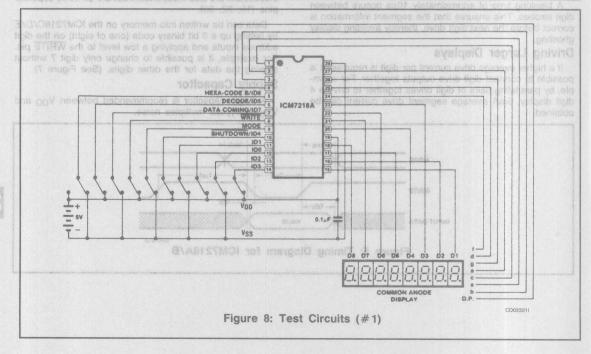


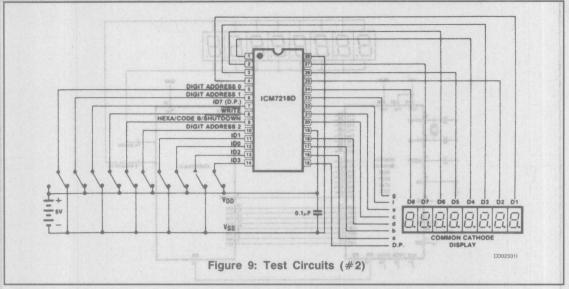
Q

ICM7218

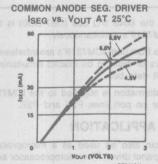




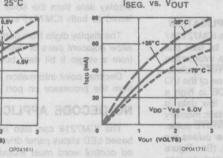




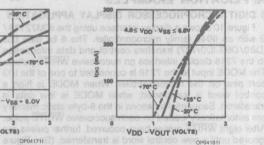
#### TYPICAL PERFORMANCE CHARACTERISTICS



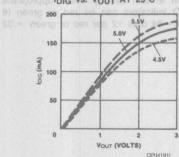
COMMON ANODE SEG. DRIVER ISEG. VS. VOUT



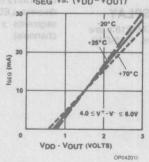
COMMON ANODE DIGIT DRIVER IDIG vs. (VDD-VOUT)



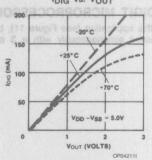
COMMON CATHODE DIGIT DRIVER COMMON CATHODE SEG. DRIVER COMMON CATHODE DIGIT DRIVER

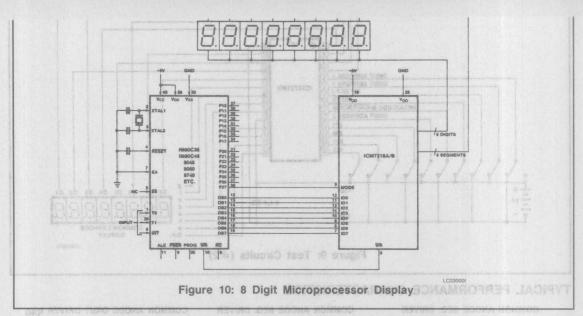


IDIG VS. VOUT AT 25°C



IDIG VS. VOUT





#### APPLICATION EXAMPLES

#### 8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Figure 10 shows a display interface using the ICM7218A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7218 display interface on successive WRITE pulses. The MODE input to the 7218 is connected to one of the I/O port pins on the microcontroller. When MODE is high a control word is transferred; when MODE is low data is transfered. Sequential locations in the 8-byte static memory are automatically loaded on each successive WRITE pulse. After eight WRITE pulses have occurred, further pulses are ignored until a new control word is transferred. (See Figure 6). This also allows writing to other peripheral devices without disturbing the ICM7218A/B.

#### 16 DIGIT MICROPROCESSOR DISPLAY

In this application (see Figure 11), both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218's simultaneously.

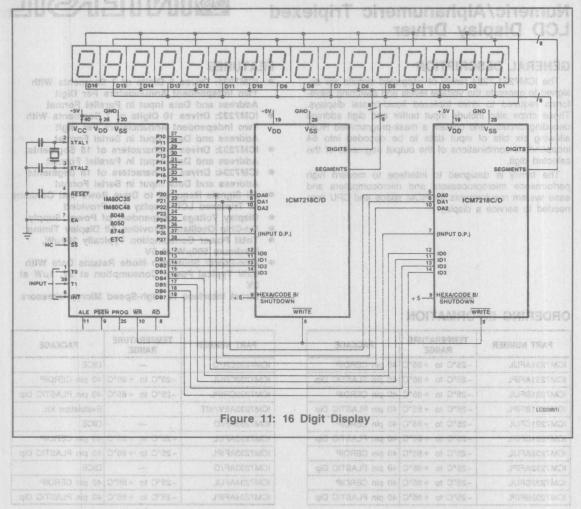
The display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7218's from the processor on port lines P26 and P27.

#### NO DECODE APPLICATION

The ICM7218 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments x 8 digits = 64 dots ÷2 per red or green = 32 channels).





# ICM7231-ICM7234 Numeric/Alphanumeric Triplexed LCD Display Driver



#### GENERAL DESCRIPTION

The ICM7231-7234 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry and contain a mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

#### **FEATURES**

- ICM7231: Drives 8 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Parallel Format
- ICM7232: Drives 10 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Serial Format
- ICM7233: Drives 4 Characters of 18 Segments Address and Data Input in Parallel Format
- ICM7234: Drives 5 Characters of 18 Segments Address and Data Input in Serial Format
- All Signals Required to Drive Rows and Columns of Triplexed LCD Display Are Provided
- Display Voltage Independent of Power Supply
- On-Chip Oscillator Provides All Display Timing
   Total Power Consumption Typically 200μW,
- Maximum 500μW at 5V

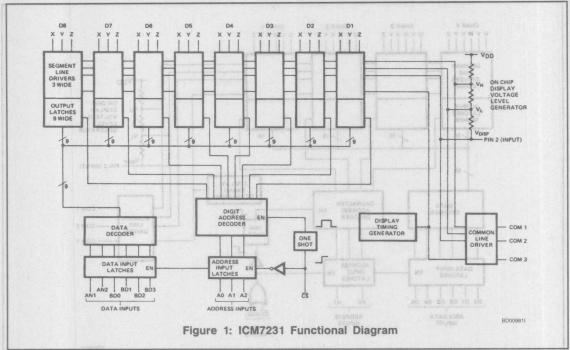
  Name of the state of t
- Low-Power Shutdown Mode Retains Data With  $5\mu W$  Typical Power Consumption at 5V,  $1\mu W$  at 2V
- Direct Interface to High-Speed Microprocessors

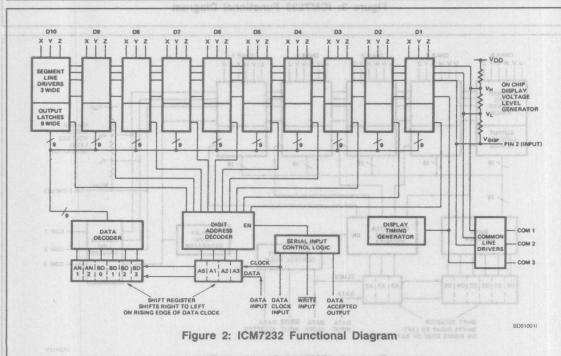
#### ORDERING INFORMATION

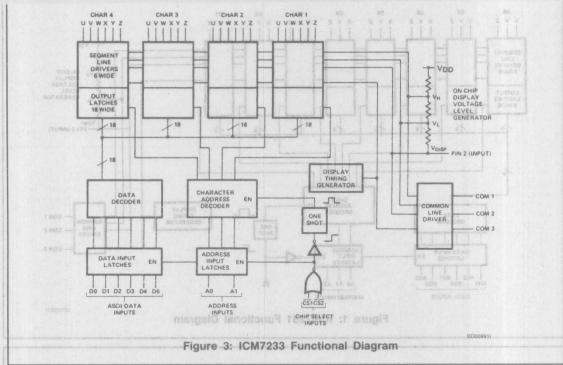
PART NUMBER	TEMPERATURE RANGE	PACKAGE					
ICM7231AFIJL	-25°C to +85°C	40 pin CERDIP					
ICM7231AFIPL	-25°C to +85°C	40 pin PLASTIC Dip					
ICM7231BFIJL	-25°C to +85°C	40 pin CERDIP					
ICM7231BFIPL	-25°C to +85°C	40 pin PLASTIC Dip					
ICM7231CFIJL	-25°C to +85°C	40 pin CERDIP					
ICM7231CFIPL	-25°C to +85°C	40 pin PLASTIC Dip					
ICM7232AFIJL	-25°C to +85°C	40 pin CERDIP					
ICM7232AFIPL	-25°C to +85°C	40 pin PLASTIC Dip					
ICM7232EFIJL	-25°C to +85°C	40 pin CERDIP					
ICM7232BFIPL	-25°C to +85°C	40 pin PLASTIC Dip					

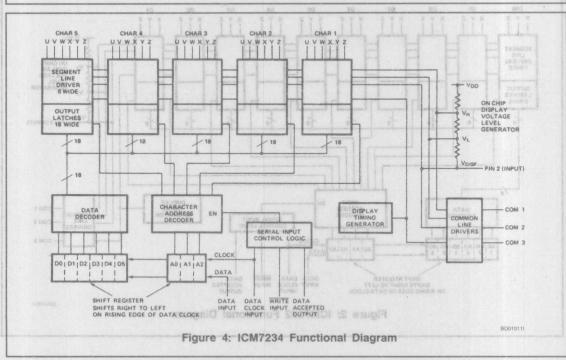
PART NUMBER	TEMPERATURE RANGE	PACKAGE				
ICM7232CR/D		DICE				
ICM7232CRIJL	-25°C to +85°C	40 pin CERDIP				
ICM7232CRIPL	-25°C to +85°C	40 pin PLASTIC Dip				
ICM7233AEV/KIT		Evaluiation Kit.				
ICM7233AF/D		DICE				
ICM7233AFIJL	-25°C to +85°C	40 pin CERDIP				
ICM7233AFIPL	-25°C to +85°C	40 pin PLASTIC Dip				
ICM7233AF/D		DICE				
ICM7234AFIJL	-25°C to +85°C	40 pin CERDIP				
ICM7234AFIPL	-25°C to +85°C	40 pin PLASTIC Dip				

8









## ICM7231-ICM7234

# **BINTERSIL**

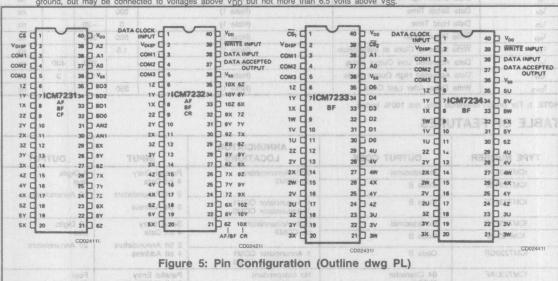
#### ABSOLUTE MAXIMUM RATINGS + 2 AT 2 O'GS - NO = 28V ROTEVE - OOV) EDITERACTERACTOR

	Power Dissipation <sup>[1]</sup>
Input Voltage <sup>[2]</sup> $V_{SS} = 0.3 \le V_{IN} \le 6.5$ Display Voltage <sup>[2]</sup> $-0.3 \le V_{DISP} \le +0.3$	Operating Temperature Range25°C to +85°C Storage Temperature Range65°C to +150°C
(Note 1) 200	Lead Temperature (Soldering, 10sec)300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. This limit refers to that of the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above VDD but not more than 6.5 volts above VSS.



#### ELECTRICAL CHARACTERISTICS (V + 5 V± 10%, VSS = 0V, TA = -25°C to +85°C unless otherwise specified)

SYMBOL	PARAMETER No. 8	TEST CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	fasedhu	4.5	>4	5.5	V
V <sub>DD</sub>	Data Retention Supply Voltage	Guaranteed Retention at 2V	2	1.6		TANGSTENVI
IDD	Logic Supply Current IDSA nd 3	Current from V <sub>DD</sub> to Ground excluding Display. V <sub>DISP</sub> = 2V	(ISC)R) Sagmy	30	100	μА
Is	Shutdown Total Current	V <sub>DISP</sub> Pin 2 Open	and the same	1	10	μА
VDISP	Display Voltage Range	V <sub>SS</sub> ≤ V <sub>DISP</sub> ≤ V <sub>DD</sub>	0	A)	VDD	V
IDISP	Display Voltage Setup Current	V <sub>DISP</sub> = 2V Current from V <sub>DD</sub> to V <sub>DISP</sub> On-Chip	Segme		30	μΑ
RDISP	Display Voltage Setup Resistor Value	One of Three Identical Resistors in String	40	75		kΩ
	DC Component of Display Signals	(Sample Test only)		1/4	1	% (VDD - VDISP
fDISP	Display Frame Rate	See Figure 7	60	90	120	Hz
VIL	Input Low Level	ICM7231, ICM7233			0.8	V
VIH	Input High Level	Pins 30-35, 37-39, 1	2.0			V
lilk	Input Leakage	ICM7232, ICM7234	LE FILM	0.1	1	μΑ
CIN	Input Capacitance	Pins 1, 38, 39 (Note 1)		5		pF
VOL	Output Low Level	Pin 37, ICM7232, ICM7234, I <sub>OL</sub> = 1mA,			0.4	V
VOH	Output High Level	$V_{DD} = 4.5V$ , $I_{OH} = -500\mu A$	4.1			V
TOP	Operating Temperature Range	Industrial Range	-25		+85	°C

## ICM7231-ICM7234



AC CHARACTERISTICS ( $V_{DD} = 5V \pm 10\%$   $V_{SS} = 0V$ ,  $-20^{\circ}C \le T_{A} \le +85^{\circ}C$ ) TAR MUMIXAM BTULIOSEA

PARALLEL INPUT (ICM7231, ICM7233) See Figure 13

SYMBOL	PARAMETER	desent TES	T CONDITIONS	MIN	TYP	MAX	UNIT
)°(tcs' + of 0°28	Chip Select Pulse Width	Storage	(Note 1)	500	350	out a thry	ns
t <sub>ds</sub>	Address/Data Setup Time	T basU	(Note 1)	200			ns
t <sub>dh</sub>	Address/Data Hold Time	námsao panto vari	(Note 1)	0	-20	otes beside	ns
ostics ton at anottac	Inter-Chip Select Time	balmalani eenit ev	od (Note 1) op vedlo yna to seed	ta 3one	b and to	nottered	μς

SERIAL INPUT (ICM7232, ICM7234) See Figures 16, 17, 18

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tci ani edisano eo	Data Clock Low Time	(Note 1)	350	SE HOG	SHE OF SE	ns
tcl	Data Clock High Time	a.a gard seem for to (Note 1) unds assessment of beat	350	d yem h	id boue	ns
t <sub>ds</sub>	Data Setup Time	(Note 1)	200	(L. 18)		ns
tdh	Data Hold Time	(Note 1)	0	-20	one proper	ns
twp the	Write Pulse Width	(Note 1)	500	350		ns
twill to the Care	Write Pulse to Clock at Initialization	(Note 1)	1.5	20 [] 40		μs
todl	Data Accepted Low Output Delay	(Note 1)		200	400	ns
todh	Data Accepted High Output Delay	(Note-1)		1.5	3	μs
t <sub>cws</sub>	Write Delay After Last Clock	(Note 1)	350	100 E BE	de de side e de d	ns

NOTE 1: For design reference only, not 100% tested.

#### TABLE OF FEATURES

ADLL OF I	LAI	OHLO		30 C) 18	ar [3]	VI VI III		2017	30	THE
TYPE NUMB		11 D 13		CODE	EL CO	ANNUNCIATOR		INPUT		PUT
ICM7231AF		Hex	adecimal	27 E . OR		h Annunciators		Parallel Entry	8 Digits	1 3 34
ICM7231BF		er Cod		MA CONS	10000000	COM3	E-12	4 bit Data	plus	0 5 94
ICM7231CF		Cod		Vo. I'd ec		annunciator COM1		2 bit Annunciators	16 Annuncia	
10W1723TCF		Cou		SA CLAS	1 A	Innunciator COM3		3 bit Address		11 G 38
ICM7232AF		Hex	adecimal	vic. EZ iss	Bot	h Annunciators		Serial Entry	10 Digits	
ICM7232B		Cod		m Gra	on	COM3		4 bit Data	plus	
ICM7232CR	are outer	Cod		wh enline		nnunciator COM1		2 bit Annunciators 4 bit Address	20 Annuncia	ators
ICM7233AF		(AS)	Character		Ann	Independent nunciators		Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters	702
ICM7233BF	MAM	TY (AS	Character CII) Segment	OESCHIPTIC	No	Independent nunciators		Parallel Entry 6 bit (ASCII) Data	Four Characters	-
			ridth number	rs)				2 bit Address	Power Su	
ICM7234AF	100	18 S	Segment		Ann	Independent nunciators		Serial Entry 6 bit (ASCII) Data	Five	0
A.,	0.0		vidth numbe	ers)		Voiew Fig 2 Open		3 bit Address	meaninford?	
ICM7234BF		64 (AS	Character		No	Independent		Serial Entry 6 bit (ASCII) Data	Five Characters	
Ац	06	18 5	Segment vidth number	rs) of aa'	/ men	VOISP = 2V Current I		3 bit Address		718
	1.					(Simplie Test only)		onent of Display Signate		
38		96				See Figure 7		ame Rate	Display Fa	
						ICM7231, ICM7233				
									foirt bigni	
						ICM7232, ICM7234			lineJ tugni	
						Pins 1, 38, 39 (Note				
V				Ant = Jol 4	Mizza			leve.) w	od augusti I	

## ICM7231-ICM7234

#### TERMINAL DEFINITIONS

#### ICM7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL			PTION serving of bea		NCTION SEROV SOL
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	pangata tar arevar dogni m	High = ON Low = OFF	See Table 3
BD0 BD1 BD2 BD3 minutes 10	32 33 34 35	Least Significant	4 Bit Binary Data Inputs	Input Data (See Table 1)	HIGH = Logical One (
A0 A1 A2	37 38 39	Least Significant Most Significant	3 Bit Digit Address Inputs	Input Address (See Table 2)	LOW = Logical Zero
CS	1	Data Input Strobe/Chip Si	elect (Note 3)	Trailing (Positive going data input to be decoraddressed digit	edge latches data, cau ded and sent out to

NOTE: 3.  $\overline{\text{CS}}$  has a special" mid-level" sense ci rcuit that establishes a test mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

#### ICM7233 PARALLEL INPUT ALPHA DISPLAY

TO of TERMINAL OFFI		PIN NO.	relgition E\1 DESCR		Negt input. The data	ction a vd bellound
00 (810 - D0 8 5 8 8 9 8 9 9 9 9 9 9 9 9 9 9 9 9 9 9	m i	31	Least Significant  Most Significant	6 Bit (ASCII) Data Inputs	See Table 4	HIGH = Logical One (1) LOW = Logical Zero (0)
3-multiplex1A displays in	NI.	37 38	Least Significant Most Significant	Address Inputs	Input Add. See Table 5	mitten to the display
of anged to CS2 to each who had been sent with the control of the	age		Chip Select Inputs (Note 3)	e similar to the are organized actors. The six	Both inputs LOW load of Rising edge of either in latched, decoded and si character.	put causes data to be

NOTE: CS1 has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided either by pulling it high when inactive, or ensuring frequent activity.

#### ICM7232 and ICM7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL SOLONS	PIN NO.	DESCRIPTION TTZ 1 900 00	and the still second of the claver such the like second of Function of the claver of t
Data Input of (48(gV) in	igni 938 flov	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
uld be the turn attney and attney attney used. Also e driven below Vss. The estruction of the chip.	he liquid crys pin 2 never b	MAXCMOS® is very important that	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of WRITE triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic. ICM7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output A fabigyt a not bluow as hous	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits ICM7234 9 bits

8

example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 7 also shows the waveform of the "Y" segment line for four

## ICM7231-ICM7234



#### ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	CM7231 PARALITE MUNERIC DIS
Display Voltage V <sub>DISP</sub>	U7 2	Negative end of on-chip resistor string used to generate intermediate and ovoltage levels for display.  Shutdown Input.	Display voltage control. When open (or less than 1V from Vpp) chip is shutdown; oscillator stops, all display pins to Vpp.
Common Line Driver Outputs	3,4,5	Good - Bit Blang Costs Costs Costs	Drive display commons, or rows.
Segment	6–29	(On ICM7231/33)	Drive display segments, or columns.
Line Driver Outputs	6–35	(On ICM7232/34)	ng least 10 Least 2gn
V <sub>DD</sub>	40/5 6/6	Chip Positive Supply	Most Squit
V <sub>SS</sub> so ,stab serialal egbe i	prior 36	Chip Negative Supply	

#### **ICM7231 FAMILY DESCRIPTION**

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

The ICM7234 uses a serial input structure like that of the ICM7232, and drives five 18-segment characters. Again, the input bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPT-ED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string. and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static dis-

#### TRIPLEXED (1/3 MULTIPLEXED) LIQUID CRYSTAL DISPLAYS

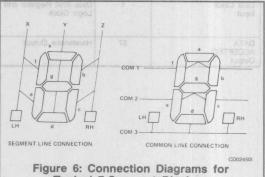
Figure 6 shows the connection diagram for a typical 7segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 7 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 7 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 8. Figure 9 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments in Figure 7.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 4 that the RMS OFF voltage is always Vp/3 and that the RMS ON voltage is always 1.92 Vp/3.

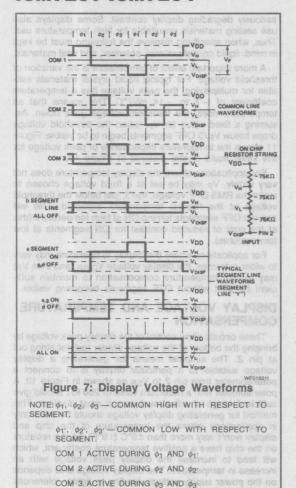
For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

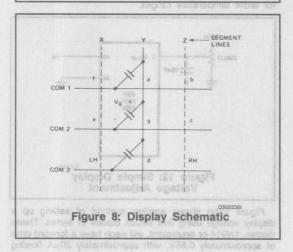
Figure 10 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for Vp = 3.1V, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage Vp/3≈1V is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

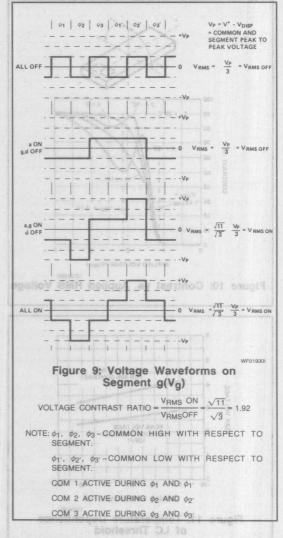
All members of the ICM7231/ICM7234 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to VDD and the other end (user input) is available at pin 2 (VDISP) on each chip. This allows the display voltage input (VDISP) to be optimized for the particular liquid crystal material used. Remember that Vp = VDD - VDISP and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below Vss. This can cause device latchup and destruction of the chip.



Typical 7-Segment Displays



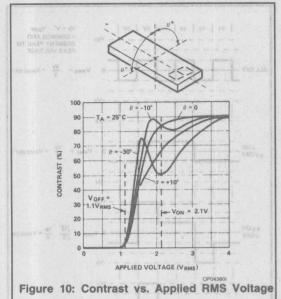


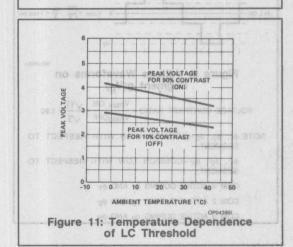


TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is effected by temporature in two ways. The response time of the display temporature in two ways. The response time of the display to obtaines in applied RMS voltage gots longer as the display temperature drops. At very low temperatures to change a new displays may take several seconds to change a new displays may take several seconds to this will not be a problem with available multiplaxed LCD the will not be a problem with available multiplaxed LCD materials, and for low-temperature applications, ingli-speed field crystal materials are available. One ingli temperature offset to consider deals with plastic materials used to make polarizer. Some polarizer become soft at high tempera-

## ICM7231-ICM7234





# TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby

seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for Vp, when the threshold voltage drops below Vp/3 OFF segments begin to be visible. Figure 11 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 10.

For applications where the display temperature does not vary widely, Vp may be set at a fixed voltage chosen to make the RMS OFF voltage, Vp/3, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V<sub>DISP</sub> (and thus V<sub>P</sub>) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

# DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to Vss as shown in Figure 12. A potentiometer with a maximum value of 200 k $\Omega$  should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than  $\pm 5^{\circ}\text{C}$  ( $\pm 9^{\circ}\text{F}$ ), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

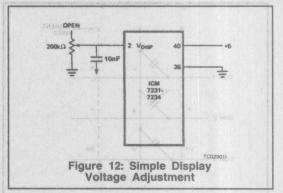


Figure 13(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20µA flowing

2.7880

DATA BUS

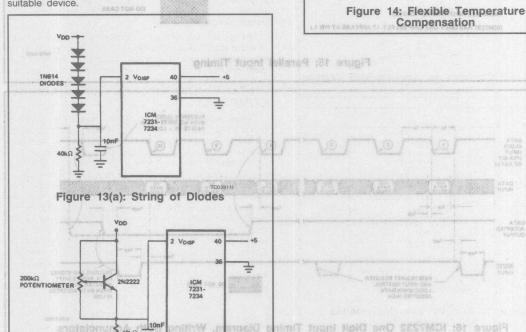
ICM7233

AF031911

## ICM7231-ICM7234

through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 10 and 11. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of -2 mV/°C; five in series gives -10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 13(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about  $-2~{\rm mV/^\circ C})$  is also multipled. The transistor should have a beta of at least 100 with a collector current of 10  $\mu{\rm A}$ . The inexpensive 2N2222 shown in the figure is a suitable device.



+5V

LOGIC SYSTEM,

ROCESSO ETC. ICL7663

incroprocessors, (see functional diagrams Figures 1 and 3), in the ICM7231, address and data bits are written into the input latches on the raing edge of the Chip Select input, in the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.

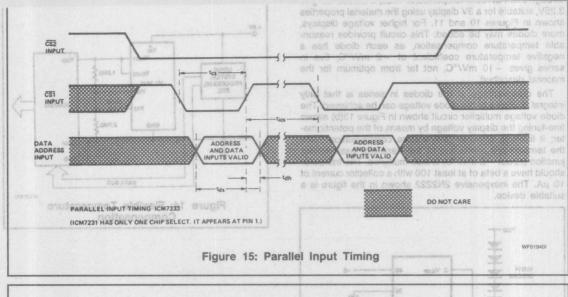
Figure 13(b): Transistor-Multiplier
Figure 13: Diode-based Temperature

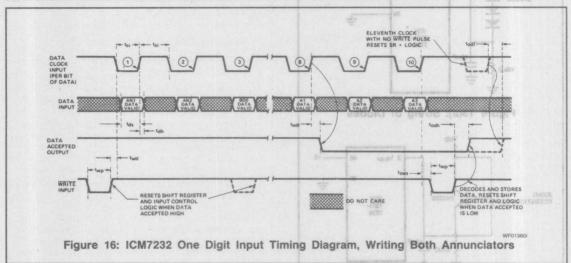
Compensation

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-6.5V), the crip may be operated at the display voltage, with Vogo connected to Vsg. The inputs of the chip are designed such that they may be driven above Vsg. without demagning the chip. This allows for example, the chip and display to operate at a regulated 3V, and a microprocessor divirig its inputs to operate with a less well controlled 5V supply. (The inputs though not be driven more than 5.5V above GND under any circumstances.) This also allows temperature this crown in Figure 14. This circumstances in the division of both voltage and for the consequence of the consequence of the consequence.

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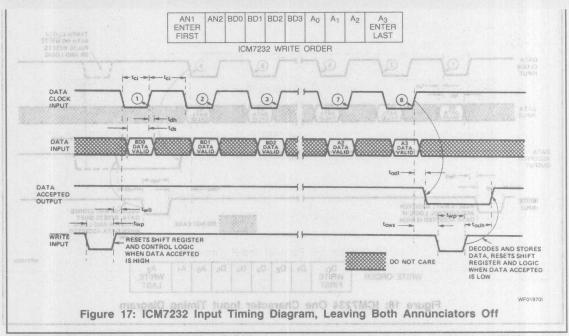


For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with  $V_{DISP}$  connected to  $V_{SS}$ . The inputs of the chip are designed such that they may be driven above  $V_{DD}$  without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663, as shown in Figure 14. This circuit allows independent adjustment of both voltage and temperature compensation.

#### DESCRIPTION OF OPERATION

#### PARALLEL INPUT OF DATA AND ADDRESS (ICM7231, ICM7233)

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, (see functional diagrams Figures 1 and 3). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input. In the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.



The rising edge of the Chip Select also triggers an onchip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input devices are shown in Figure 15, with the values for setup, hold, and pulse width times shown in the AC Characteristics section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

# SERIAL INPUT OF DATA AND ADDRESS (ICM7232, ICM7234)

The ICM7232 and ICM7234 trade six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits (ICM7232) or one more 18-segment character (ICM7234). This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to functional diagrams, Figures 2 and 4 and timing diagrams, Figures 16, 17, and 18. The interface consists of four pins: DATA Input, DATA CLOCK Input, WRITE Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232, 9 in the ICM7234), the DATA ACCEPTED Output goes low, Following this, a low-going pulse at the WRITE input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the WRITE input will not change the

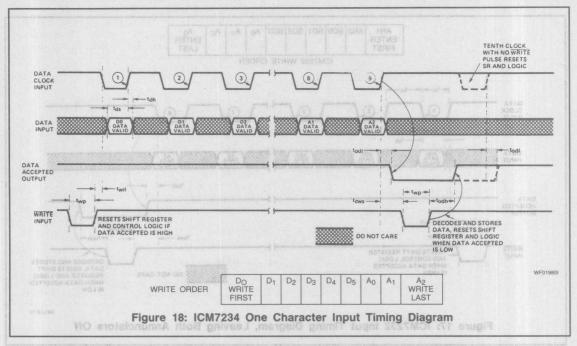
outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic, while in the ICM7234 it is the tenth.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 16. First, when DATA ACCEPTED is high, send a WRITE pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at WRITE will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 17.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.



In the ICM7234, nine bits are always required; the control logic is similar, but allows only a WRITE (DATA ACCEPTED Low) with nine bits entered in the shift register, as shown in Figure 18.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a WRITE pulse, none of the outputs will be changed.

#### DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 19. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1). (See Figure 20). The "C" devices provide only a "Code B" output for the 7-segments.

The ICM7233 and ICM7234 are supplied in "A" and "B" versions. Both versions decode an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and two "dots". The "A" devices have numbers which are half width and the "B" devices have full width numbers. The layout for a single character is shown in Figure 21 with output decoding shown in Table 4.

TABLE 1. BINARY DATA DECODING (ICM7231/32)

PLAY		hs.	DE		1:12
CODI	HEX	BD 0	BD 1	BD 2	BD 3
0	0	0	0	0	0
T.	1	1	0	0	0
102	2	0	130	0	0
19	olp o	Nh B	10	0	0
4	4	0	0	1	0
5	5	1	0	1	0
E	6	0	1	1	0
181	and	3	1	E.	0
8	8	0	0	0	1
3	3	1	0	0	1
aci n	8	0	1	0	1
E	6	1	1	0	1
SP	1	0	0	1	1
L	d	1	0	1	1
P	E	0	1	1	1
BLANK	150	19	1	1	19

TB00080

## ICM7231-ICM7234

TABLE 2. ADDRESS DECODING (ICM7231/32)

co	DE IN	PUT		DISPLAY OUTPUT
ICM7232 ONLY A3	NLY		A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

CO	DE	DISPLAY	ОИТРИТ
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0	8	8
0	1	8	8
1	0	8	8
1	1	8	18

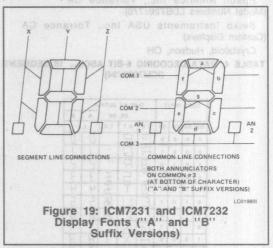
TB00090

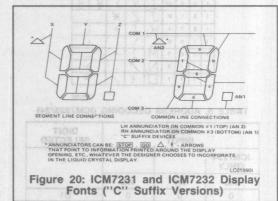
#### **EVALUATION KITS**

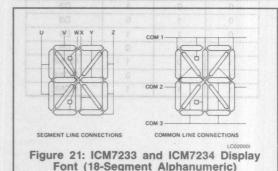
After purchasing a sample of the ICM7231/32/33/34, the majority of users will want to build a sample display. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering kits which contain all the necessary components to build 8 character displays. With the

help of such a kit, an engineer or technician can have the system "up and running" in about half an hour.

The ICM7233EV/KIT contains the appropriate ICs, a circuit board, a Multiplexed LCD display 16/18 segment, passive components, and miscellaneous hardware.







18

(Model Numbers LDB726/7/8).
Seiko Instruments USA Inc., Torrance CA

Crystaloid, Hudson, OH

(Custom Displays)

TABLE 4. DATA DECODING 6-BIT ASCII ... 18 SEGMENT (ICM7233/34)

CC	DE	INPL	IT	Di	SPLAY	OUTP	JT.		TH
	54	0			05,	D4	A	8	1
03	D2	Di	DO	0,0	0, 1	1, 0	1	1/	qual
0	0	0	0	P	P		0	10	
0	0	0	1	H		1	1		SOLI TS
0	0	al.	0	H	R	11	2	15	2012 13
0	0	040	1		5	Ŧ	E	13	10 62
0	18	0	0	D	T	5	4	14	
0	1	0	1	E	L	另	5	5	
0	4	1	0	F	V	B	6	16	TEN S
0	1	T	1	6	W	1000	7	197	19
1	0	0	0	H	X	(	IB	IB	
1	0	. 0	1	I	Y	>	9	19	er Accession
1	0	1	0	J	Z	*			
1	0	1	1	K	LE	+		;	
1	1	0	0	L	1	1	10	4	- FI
1	1	0	1	M		1	A.	FI	IV
2	1	1	0	N	1			7	
1	1	1	1	In	1	1	V.P	7	1973

TABLE 5. ADDRESS DECODING (ICM7233/34)

IS HAT PROTESS OF H	DIGIT		
ICM7234 ONLY	n or esaceru n	MONTH DESIGNA	CHARGE TRACE TRACE TENRAL SEE ENBERTO TOTAL SEE ENBERTO TOTAL SEE ENBERTO
A2	NAT D	AO V	Figure 20: IC
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	n 1 7	D4
1	0	0	D5
1	9/10	1	NONE
1/2		0	NONE
1 //	1 - 5 %	00 1	NONE

PARTY PARTY STORY OF THE PARTY OF

Figure 21: IOM7233 and ICM7234 Displ

DIGIT	OA			CHT/232 ONLY A3		
		1	0			
80						
			1			
		1				
		1				
	1	1				
	0					
		0				
NONE						

TABLE 3. ANNUNCIATOR DECODING

DIFFERENCE STATE OF THE STATE O	CAPTEST AND CONTROL OF COM S AND COM S		
		1	

STIN MOSTALLIAVE

After purchasing a sample of the IOM7231/32/38/34, the majority of users will want to build a sample display. The parts can then be evaluated against the data cheef specifications, and thed out in the intended application. However, locating and purchasing even the small number of additional components required, then wring a breadboard, can often cause delays of days or sometimes weeks. To evoid this problem and facilitate evaluation of these unique circuits intend is offering this which contain all the necessary components to build 6 character displays. With the

#### TYPICAL APPLICATIONS

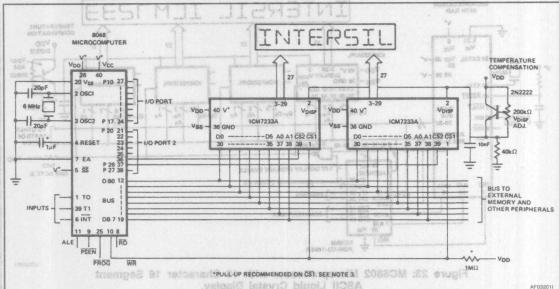


Figure 22: 8048/IM80C48 Microcomputer with 8 Character 16 Segment

alions are addressed via the address bus. Note that VMA is not

The two bit character address is merged with the data and written to the display driver under the control of the  $\overline{WR}$  line. Port lines are used to either select the target driver, or deselect all of them for other bus operations.

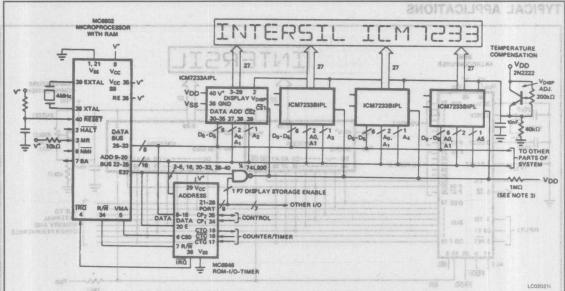
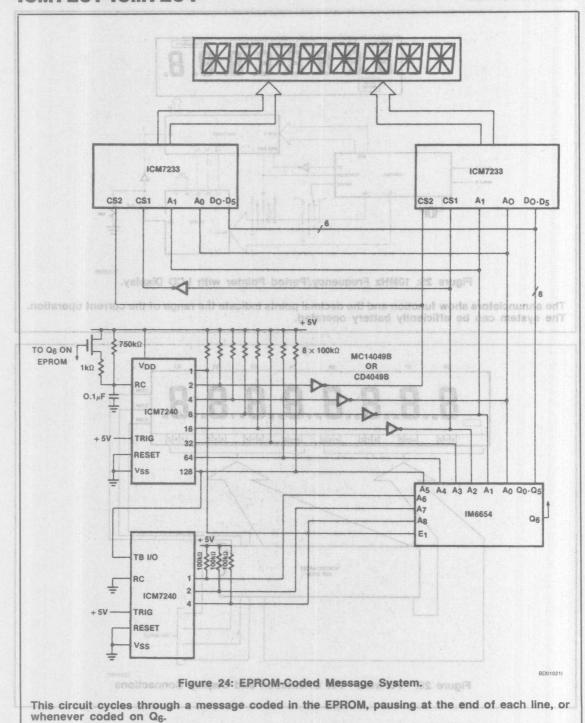


Figure 23: MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

The peripheral device provides ROM and Timer functions in addition to port line control of the display bank. Individual character locations are addressed via the address bus. Note that VMA is not decoded on these lines, which could cause problems with the TST instruction.



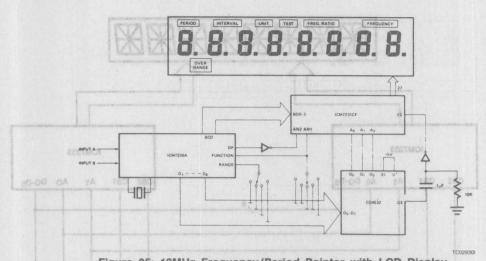
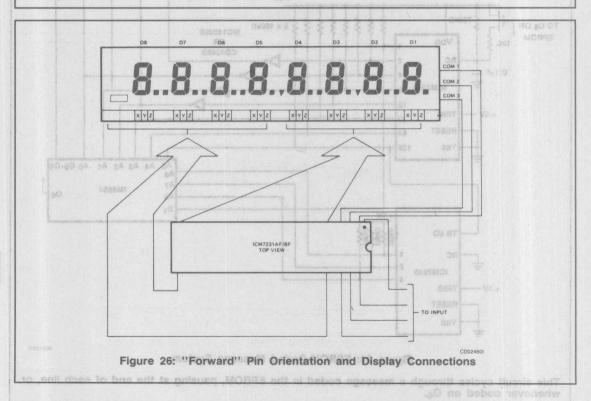
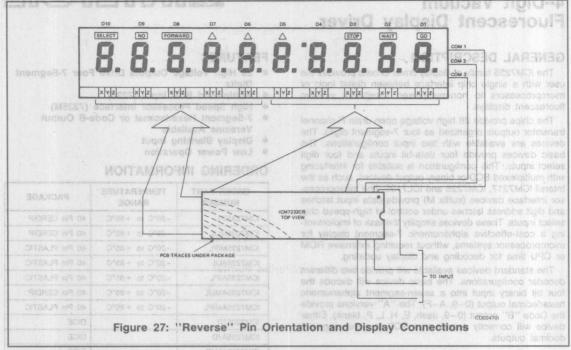


Figure 25: 10MHz Frequency/Period Pointer with LCD Display.

The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.





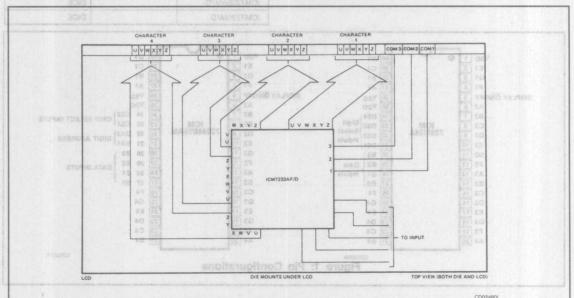


Figure 28: "Forward" Die Pad Orientation and Typical Triplex Alphanumeric Display Connections

## ICM7235 4-Digit Vacuum

# Fluorescent Display Driver



#### GENERAL DESCRIPTION

The ICM7235 family of display driver circuits provides the user with a single chip interface between digital logic or microprocessors to non-multiplexed 7-segment vacuum fluorescent displays.

The chips provide 28 high voltage open drain P-channel transistor outputs organized as four 7-segment digits. The devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the Intersil ICM7217, ICM7226 and ICL7135. The microprocessor interface devices (suffix M) provide data input latches and digit address latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexadecimal output (0-9, A-F). The "A" versions provide the Code "B" output (0-9, dash, E, H, L, P, blank). Either device will correctly decode true BCD to seven-segment decimal outputs.

#### **FEATURES**

- 28 High Voltage Outputs Drive Four 7-Segment Digits
- Multiplexed BCD Input (7235)
- High Speed Processor Interface (7235M)
- 7-Segment Hexadecimal or Code-B Output Versions Available
- Display Blanking Input
- Low Power Operation

#### ORDERING INFORMATION

ORDER PART NUMBER		
ICM7235IPL	-20°C to +85°C	40 Pin CERDIP
ICM7235MIJL	-20°C to +85°C	40 Pin CERDIP
ICM7235MIPL	-20°C to +85°C	40 Pin PLASTIC
ICM7235AIJL	-20°C to +85°C	40 Pin PLASTIC
ICM7235AIPL	-20°C to +85°C	40 Pin PLASTIC
ICM7235AMIJL	-20°C to +85°C	40 Pin CERDIP
ICM7235AMIPL	-20°C to +85°C	40 Pin PLASTIC
ICM7235/D	THE ANIMATE	DICE
ICM7235A/D		DICE
ICM7235AM/D		DICE
ICM7235M/D		DICE

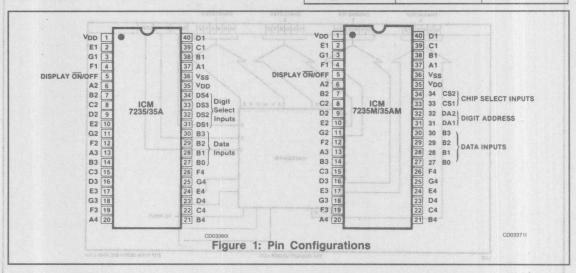


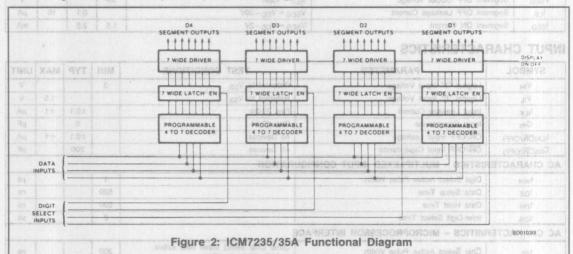
Figure 28: "Forward" Die Pad Orientation and Typical Triplex

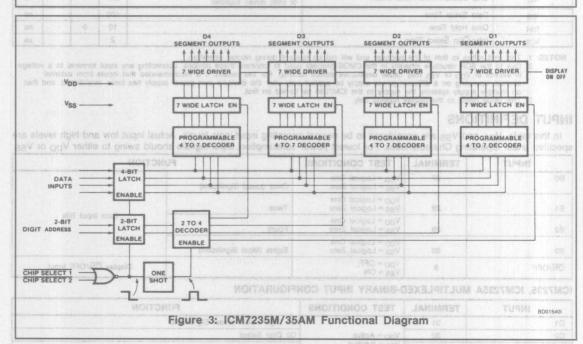
#### ABSOLUTE MAXIMUM RATINGS of the Decision of the Control of the Con

Power Dissipation (Note 1)	0.5W @ +70°C
Supply Voltage (VDD-VSS)	awoawo.6.5 Volts
Input Voltage (Note 2)VSS	$_{\rm S}$ -0.3V to V <sub>DD</sub> + 0.3V
Output Voltage (Note 3)	V <sub>DD</sub> -35V

Operating Temperature Range	20°C to +85°C
Storage Temperature Range	
Lead Temperature (Soldering, 10sec)	300°C

Stresses above listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





128 - 011	perating Lemperature Hange -20"C	() () () () () () () () () () () () () (	CITHE	Loois	R155E1	ROWN
SYMBOL	O'888 Temper STAMARA PARAMETER TEMPER TO PER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUPP	Operating Supply Voltage Range (VDD-VSS)	7 VEO + 00 V OF VE O- 85 V	4	DICHA)	6	V
ISTBY	Supply Current	Measured V <sub>DD</sub> to V <sub>SS</sub> Test circuit; display blank or OFF	edA" est	10	50	μΑ
IDD I	Supply Current of another body and to another land	Measured V <sub>DD</sub> to Display	to yna	o eastt	100	mA in
VSEG	Segment OFF Output Voltage	ISLK = 10µA	30	SHIDHOD	demay u	V
ILS	Segment OFF Leakage Current	V <sub>SEG</sub> = V <sub>DD</sub> -30V		0.1	10	μΑ
ISEG	Segment ON Current	V <sub>SEG</sub> = V <sub>DD</sub> -2V	1.5	2.5		mA

#### INPUT CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH	Logical "1" Input Voltage	Referred to V <sub>SS</sub>	3			V
VIL	Logical "0" Input Voltage	Referred to V <sub>SS</sub>			1.5	V
lilk	Input Leakage Current	Pins 27-34		±0.1	±1	μΑ
CIN	Input Capacitance	Pins (27-34		5		pF
IILK(ON/OFF)	ON/OFF Input Leakage	All Devices		±0.1	±1	μΑ
CIN(ON/OFF)	ON/OFF Input Capacitance	All Devices		200		pF
AC CHARACTE	RISTICS - MULTIPLEXED INPUT CON	FIGURATION			ATAG	
twH	Digit Select Active Pulse Width		1			μs
t <sub>DS</sub>	Data Setup Time		500		3/11/11	ns
tDH	Data Hold Time		200		Tible	ns
t <sub>IDS</sub>	Inter-Digit Select Time		2		25789 85789	μs
AC CHARACTE	ERISTICS - MICROPROCESSOR INTERF	ACE				
t <sub>WL</sub>	Chip Select Active Pulse Width	Other Chip Select either held active, or both driven together	200			ns
t <sub>DS</sub>	Data Setup Time	The second state of the se	100	evenoù romoy	and wines	ns
tDH	Data Hold Time		10	0		ns
tics	Inter-Chip Select Time	PO TREBUSE AYURTU OF THE PROPERTY OF THE PROPE	2			μs

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any input terminal to a voltage in excess of VDD or VSS may cause destructive device latch-up. For this reason, it is recommended that inputs from external sources operating on a different power supply be applied only after the device's own power supply has been established, and that on multiple supply systems the supply to the ICM7235 be turned on first.

3. This value refers to the display outputs only.

#### INPUT DEFINITIONS

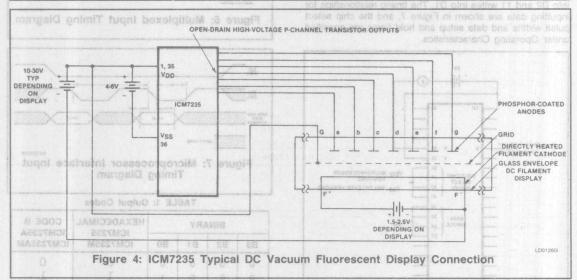
In this table, VDD and VSS are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing to either VDD or VSS.

INPUT	TERMINAL	TEST CONDITIONS	1	FU	NCTION	
В0	27	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Ones (Least	Significant)	LAYON	ATAG ETURNE
B1	28	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Twos	priservine man	Jarana I	
B2	29	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Fours	# 07 S	Data Input	Bits
В3	30	V <sub>DD</sub> = Logical One V <sub>SS</sub> = Logical Zero	Eights (Most	Significant)	B.HAM2	
ON/OFF	5	V <sub>DD</sub> = OFF, V <sub>SS</sub> = ON			Display ON/O	FF Input

#### ICM7235, ICM7235A MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	TEST CONDITIONS	FUNCTION
D1	31 7161	M Functional Dia	D1 Digit Select (Least Significant)
D2	32	V <sub>DD</sub> = Active	D2 Digit Select
D3	33	V <sub>SS</sub> = Inactive	D3 Digit Select
D4	34		D4 Digit Select (Most Significant)

INPUT	DESCRIPTION	TERMINAL	TEST CONDITIONS	
DA1	Digit ADDRESS Bit 1 (LSB)	31	V <sub>DD</sub> = Logical One	DA2 & DA1 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4
DA2	Digit ADDRESS Bit 2 (MSB)	32	V <sub>SS</sub> = Logical Zero	DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
CS1	Chip Select 1	33	V <sub>DD</sub> = Inactive	When both CS1 and CS2 are taken to VSS the data at
CS2	Chip Select 2	34	V <sub>SS</sub> = Active	the Data and Digit Address inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.



VACUUM FLUORESCENT DISPLAYS (4 DIGIT) AVAILABLE FROM:

N.E.C. Electronics, Inc.
Models FIP4F8S and FIP5F8S

#### CIRCUIT DESCRIPTION

Each device in the ICM7235 family provides signals for directly driving the anode terminals of a four-digit, 7-segment non-multiplexed vacuum fluorescent display. The outputs are taken from the drains of high-voltage, low-leakage P-channel FETs. Each is capable of withstanding > –35V with respect to V $_{\rm DD}$ . In addition, the inclusion of an  $\overline{\rm ON/OFF}$  input allows the user to disable all segments by connecting pin 5 to V $_{\rm DD}$ ; this same input may also be used as a brightness control by applying a signal swinging between V $_{\rm DD}$  and V $_{\rm SS}$  and varying its duty cycle.

The ICM7235 may also be used to drive nonmultiplexed common cathode LED displays by connecting each segment output to its corresponding display input, and tying the common cathode to Vss. Using a power supply of 5V and an LED with a forward drop of 1.7V results in an "ON" segment current of about 3mA, enough to provide sufficient brightness for displays of up to 0.3" character height.

Note that these devices have two V<sub>DD</sub> terminals, and each should be connected to the positive supply voltage. This double connection is necessary to minimize the effects of bond wire resistance, which could be a problem due to the high display currents.

### Input Configurations and Output Codes

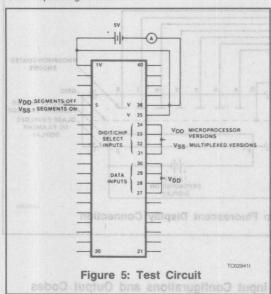
The standard devices in the ICM7235 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 through 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7235 and ICM7235M decode this binary input into a 7-segment alphanumeric hexadecimal output, while the ICM7235A and ICM7235AM decode the binary input into the same 7-segment output as the ICM7218 "Code B," i.e., 0–9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a 7-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the 7-segment outputs decoded from the four input bits. For larger quantity orders, (10K pcs. minimum) custom decoder options can be arranged. Contact your Intersil Sales Office for details.

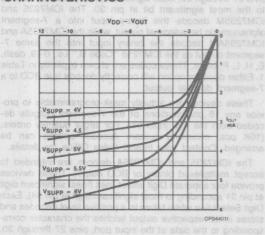
The ICM7235 and ICM7235A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate Digit select lines (least significant digit at pin 31 ascending to most significant digit at pin 34). Each Digit Select line when taken to a positive level decodes and stores in its respective output latches the character corresponding to the data at the input port, pins 27 through 30.

The ICM7235M and 7235AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the 2-bit Digit Select code (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both Chip Select inputs (CS1 pin 33, CS2 pin 34) are taken to Vss. On the rising edge of either Chip Select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches. A select code of 00 writes into D4, 01 writes into D3, 10 writes into D2 and 11 writes into D1. The timing relationships for inputting data are shown in Figure 7, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.



#### TYPICAL PERFORMANCE CHARACTERISTICS



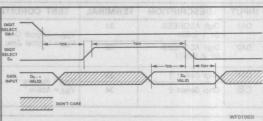


Figure 6: Multiplexed Input Timing Diagram

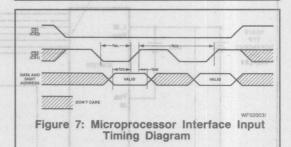


TABLE 1: Output Codes

	BIN	ARY		HEXADECIMAL ICM7235	CODE B
В3	B2	B1	B0 ICM7235M		ICM7235AM
0	0	0	0	Figure 4:	0
0	0	0	-1-	1	1
0	0	VA TE	0	VALISEN 2 WEDENA	
0	0	1	1	3	3 3
0	1	0	0	4	4
0	1	0	1	0179510830	1150AI
0	a teb	v010 v	0	ESTIMO Gent in a	avera 6 and
0	109	19 8	BOHT T	of ebon7 and g	niviro 7 diseni
1	0	0	0	nintiple8eq Area	18 mag
1	0	0	eniso	munipleged visct aken from the torrel Fig. 5. Each	9
s tolono	0	oni1no	0	ogy A roogso	ettina tratamen
				eau artb wolle t	
perfed	06 k V	0	0	and CV of a r	iq yo Homo
Tug wa	9	0	ny giqu	vd lordroo ass	mulpi L a s
1	1	1	0	bna sev bna	P
oxequal	maon	evanb	1 900	ed os Fyam de	(BLANK)

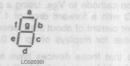


Figure 8: Segment Assignment

## ICM7243 8-Character LED

# μP-Compatible Display Driver

#### GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8 x 6 memory, high power character and segment drivers, and the multiplex scan circuitry.

Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either Serial (MODE = 1) or Random (MODE = 0). In the Serial Access mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading. A CLeaR pin is provided to clear the memory and reset the location counter. The Random Access mode allows the processor to select the memory address and display digit for each input word.

The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

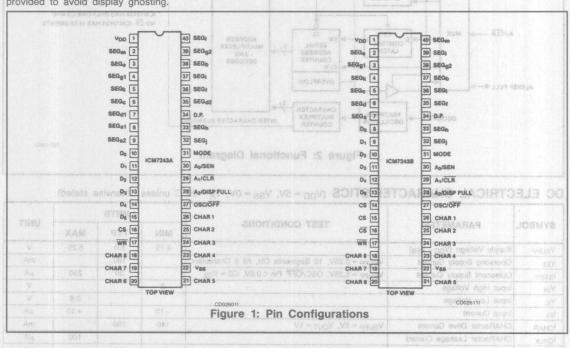


#### **FEATURES**

- 14- and 16-Segment Fonts With Decimal Point
- Mask Programmable For Other Font-Sets Up to 64 Characters
- Microprocessor Compatible
- Directly Drives Small Common Cathode Displays
- Cascadable Without Additional Hardware
- Standby Feature Turns Display Off; Puts Chip in Low Power Mode
- Serial Entry or Random Entry of Data Into Display
- Single +5V Operation
- Character and Segment Drivers, All MUX Scan Circuitry, 8 x 6 Static Memory and 64-Character ASCII Font Generator Included On-Chip

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	
ICM7243AIJL	-20°C to +85°C	CERDIP	
ICM7243BIJL	-20°C to +85°C	CERDIP	
ICM7243B EV/KIT			
ICM7243BIPL	-20°C to +85°C	PLASTIC	
ICM7243B/D		DICE	
ICM7243BCPL	0°C to +70°C	PLASTIC	

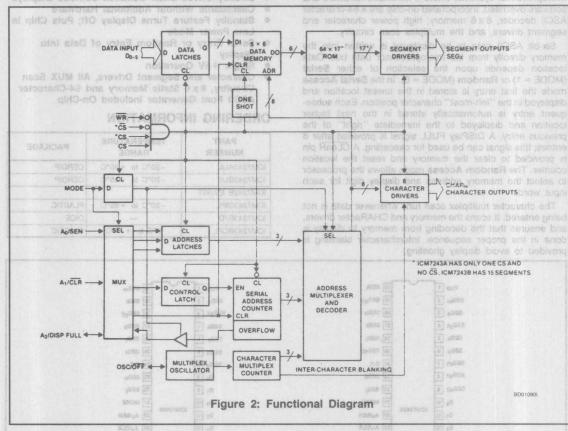


8

Supply voltage (VDD - VSS)	6V
CHARacter Output Current	
SEGment Output Current	30mA
Input Voltage (Any Terminal) (VDD+0.3V) to	(Vss-0.3V)
Power Dissipation	1W

Operating Temperature Range (I) .....-25°C to +85°C (C) .......0°C to 70°C Storage Temperature Range ......-55°C to +125°C Lead Temperature (Soldering, 10sec) ......300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



#### DC ELECTRICAL CHARACTERISTICS (VDD = 5V, VSS = 0V, TA = 25°C unless otherwise stated)

SYMBOL	1840 [8]	E course				
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>SUPP</sub>	Supply Voltage (VDD - VSS)	E	4.75	5.0	5.25	٧
IDD	Operating Supply Current	V <sub>SUPP</sub> = 5.25V, 10 Segments ON, All 8 Characters		180		mA
ISTBY	Quiescent Supply Current	V <sub>SUPP</sub> = 5.25V, OSC/OFF Pin < 0.5V, CS = V <sub>SS</sub>		30	250	μΑ
VIH	Input High Voltage	- CHANGE - CHANGE	2	And a series		V
VIL	Input Low Voltage				0.8	V
IIN	Input Current	Figure 1: Pin Conflourations	-10	SURE SET S	+10	μΑ
ICHAR	CHARacter Drive Current	V <sub>SUPP</sub> = 5V, V <sub>OUT</sub> = 1V	140	190		mA
ICHLK	CHARacter Leakage Current				100	μΑ
ISEG	SEGment Drive Current	V <sub>SUPP</sub> = 5V, V <sub>OUT</sub> = 2.5V	14	19		mA

OVALDOL	DADAMETER	TEST CONDITIONS		LIADE				
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	re TYP	MAX	UNIT	
İSLK	SEGment Leakage Current	THEMSON			0.01	10	μΑ	
VOL	DISPlay FULL Output Low	IOL = 1.6mA		1.22%	Viel .	0.4	V	
VOH	DISPlay FULL Output High	I <sub>IH</sub> = 100μA		2.4	No. 1		V	
fds	Display Scan Rate				400		Hz	

#### AC ELECTRICAL CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V. $V_{DD} = 5V$ , $T_A = 25$ °C unless otherwise stated).

SYMBOL	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT
twpi	WR, CLeaR Pulse Width Low	40		250	Z DIS	FIELD-L	1011
twph	WR, CLeaR Pulse Width High (Note 1)			250			
t <sub>DH</sub>	Data Hold Time			0	-100		
tos	Data Setup Time			250	150	A 3 1 2 1 0 1	
t <sub>AH</sub>	Address Hold Time			125			ns
tas	Address Setup Time			40	15		
tcs	CS, CS Setup Time		1011000	0			
t <sub>T</sub>	Pulse Transition Time			den average (2)	Ar Arace	100	mi3
tsen	SEN Setup Time			0	-25	cter Four	Charle
twDF	Display Full Delay	en anno de colta	To the second	600	480	1000	and the same of th

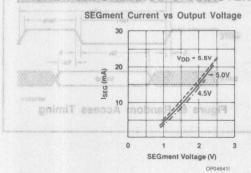
#### CAPACITANCE

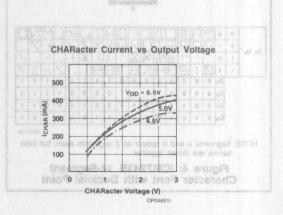
SYMBOL	TEST	MIN	TYP	MAX	UNIT
CIN	Input Capacitance (Note 2)		5		pF
CO.	Output Capacitance (Note 2)		5	103.00	pF

\*Not tested. (Guaranteed)

NOTES: 1. In Serial mode WR high must be ≥ T<sub>SEN</sub> +T<sub>WDF</sub>.
2. For design reference only, not 100% tested.

#### TYPICAL PERFORMANCE CHARACTERISTICS

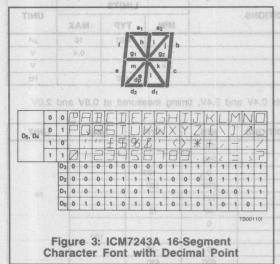


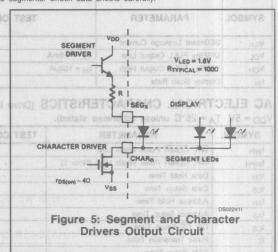


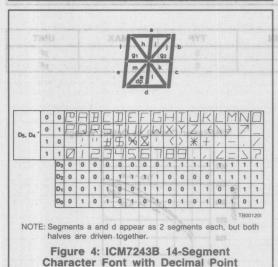


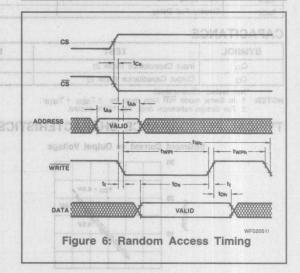
#### ICM7243A/B DISPLAY FONT AND SEGMENT ASSIGNMENTS TO ARABO JACKETO ALE OF

Note: Some display manufacturers use different designations for some of the segments. Check data sheets carefully.









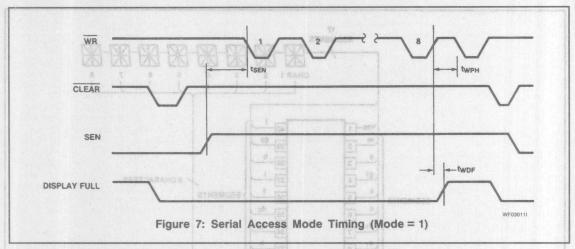


TABLE 1: PIN DESCRIPTIONS, ICM7243A(B)

SIGNAL	O PIN 30084	FUNCTION
D <sub>0</sub> – D <sub>5</sub>	10 –15 (8 – 13)	Six-Bit ASCII Data input pins (active high).
CS, CS	16 (14–16)	Chip Select for decoding from $\mu P$ address bus, etc.
WR POLL OUTPLAW	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and WR can be used as CS.
DOM SE SE SE SE SE SE SE SE SE SE SE SE SE	O CHARLES OF CHARLES	Selects data entry MODE. High selects <b>Serial Access</b> (SA) mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the <b>Random Access</b> (RA) mode where data is displayed on the character addressed via A <sub>0</sub> – A <sub>2</sub> Address pins.
A <sub>0</sub> /SEN	30 AAHO 55	In RA mode it is the LSB of the character Address. In SA mode it is used for cascading display driver/controllers for displays of more than characters (active high enables driver controller).
A <sub>1</sub> /CLeaR	29	In RA mode this is the second bit of the address. In SA mode, a low inpu will CLeaR the Serial Address Counter, the Data Memory and the display
A <sub>2</sub> /DISPlay FULL	28 (SANO)	In RA mode this is the MSB of the Address. In SA mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/OFF	27 Hugyl Clycuit	OSCillator input pin. Adding capacitance to V <sub>DD</sub> will lower the internal oscillator frequency. An external oscillator is also applied to this pin. A low puts the display controller/driver into a quiescent mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG <sub>a</sub> – SEG <sub>m</sub> , D.P.	2-9 (7), 32-40	SEGment driver outputs.
CHARacter 1 – 8	18 – 21, 23 – 26	CHARacter driver outputs.

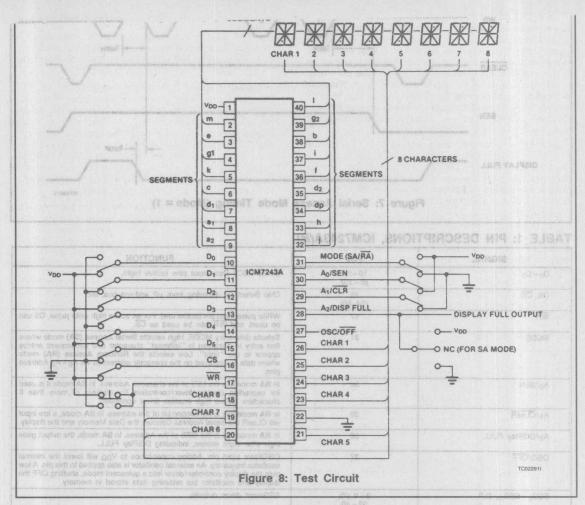
Sevial Access Mode. If the internal latch is sold or Serial Access (SA), (MODE latched high), the Serial Exiable input on SEN will be latched on the failing edge of WR (or its equivalent). The CLR input is asynchronous, and will force clear the Serial Address Counter to address 000 (CHAREC later), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output is always active in SA mode also, and indicates the overflow status of the Serial Address Counter if this output is tow, and SEN is (latched as) high, the centents of the Counter will be used to establish the Data Memory location for the Data input. The SERIAL COUNTER is then incremented on the rising edge of WPT.

use of a multiplexed 6-bit bus controlling both address a

ANDed, so all actions described as occurring on an edge of WR, with CS and CS enabled, will occur on the equivalent flast) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (ebout 5ns) greater than from WR or CS due to the additional inventor contributed on the former.

MODE. The MODE pin input is latched on the falling edge of WR (or its equivalent, see above). The location in Sata Mamory where incoming data will be placed is determined either from the Address pins or the Serial Address Counter, ander concol of this latch which also controls the function of AA/SEN. AA/CER, and AA/SISRIAY FULL.

Random Access Mode. When the internal mode latch is set for Random Access (RA) (MODE latched low), the latched low), the highest input on An An and An will be latched by the falling



#### **DETAILED DESCRIPTION**

 $\overline{WR}$ ,  $\overline{CS}$ ,  $\overline{CS}$ . These pins are immediately functionally ANDed, so all actions described as occurring on an edge of  $\overline{WR}$ , with  $\overline{CS}$  enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from  $\overline{CS}$  pins are slightly (about 5ns) greater than from  $\overline{WR}$  or  $\overline{CS}$  due to the additional inverter required on the former.

**MODE.** The MODE pin input is latched on the falling edge of  $\overline{\rm WR}$  (or its equivalent, see above). The location in Data Memory where incoming data will be placed is determined either from the Address pins or the Serial Address Counter, under control of this latch, which also controls the function of A<sub>0</sub>/SEN, A<sub>1</sub>/ $\overline{\rm CLR}$ , and A<sub>2</sub>/DISPlay FULL.

**Random Access Mode.** When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on  $A_0$ ,  $A_1$  and  $A_2$  will be latched by the falling

edge of WR (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by WR.

Serial Access Mode. If the internal latch is set for Serial Access (SA), (MODE latched high), the Serial ENable input on SEN will be latched on the falling edge of  $\overline{\text{WR}}$  (or its equivalent). The  $\overline{\text{CLR}}$  input is asynchronous, and will forceclear the Serial Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output is always active in SA mode also, and indicates the overflow status of the Serial Address Counter. If this output is low, and SEN is (latched as) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of  $\overline{\text{WR}}$ . If SEN is low, or DISPlay FULL is high, no action will occur.

This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Serial Access** mode.

Changing Modes. Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of WR (or its equivalent). When changing mode from Serial Access to Random Access, note that A2/DISPlay FULL will be an output until WR has fallen low, and an Address drive here could cause a conflict. When changing from Random Access to Serial Access, A1/CLR should be high to avoid inadvertent clearing of the Data Memory and Serial Address Counter. DISPlay FULL will become active immediately after the falling edge of WR.

Data Entry. The input Data is latched on the rising edge of WR (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in Random Access mode. Timing is controlled by the WR input.

OSC/OFF. The device includes a one-pin relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V<sub>DD</sub> at the OSC/OFF pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter strobe lines (see Display Output). An intercharacter blanking signal is derived from the pre-divider. An additional comparator on the OSC/OFF input

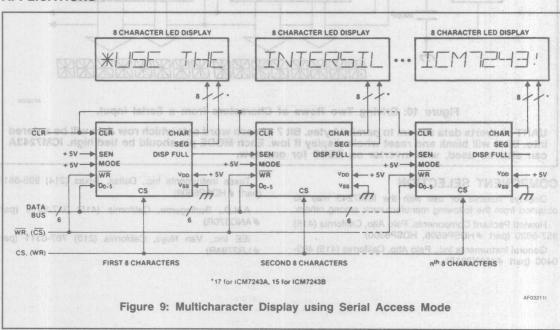
detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Muttiplex Counter. This puts the circuit in a low-power-dissipation mode in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output. The address output of the Multiplex Counter is multiplexed into the address input of the Data Memory, except during  $\overline{\text{WR}}$  operations (in Serial Access mode, with SEN high and DISPlay FULL low), to control display operations. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about  $5\mu$ s). Each CHARacter output lasts nominally about  $300\mu$ s, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during WR operations (with SEN high and DISPlay FULL Low for **Serial Access** mode). The outputs may also be disabled by pulling OSC/OFF low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

#### **APPLICATIONS**



#### APPLICATIONS (CONT.)

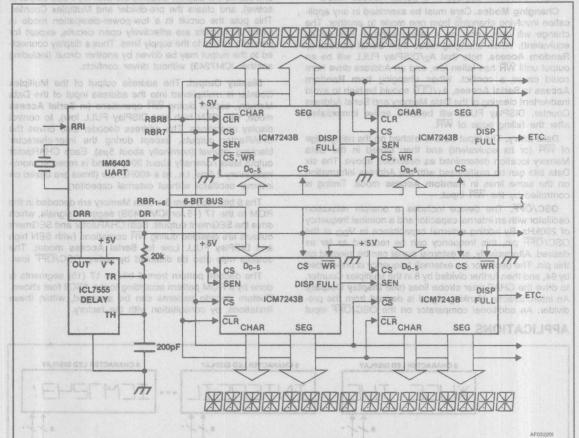


Figure 10: Driving Two Rows of Characters from a Serial Input.

UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

#### COMPONENT SELECTION

Displays suitable for use with the ICM7243 may be obtained from the following manufacturers; among others:

Hewlett Packard Components, Palo Alto, California (415) 857-6620 (part #HDSP6508, HDSP6300)

General Instruments Inc., Palo Alto, California (415) 493-0400 (part #MAN2815)

Texas Instruments Inc., Dallas, Texas (214) 995-6611 (part #HDSP6508)

A.N.D., Burlingame, California (415) 347-9916 (part #AND370R)

IEE Inc., Van Nuys, California (213) 787-0311 (part #LR3784R)

Figure 9: Multicharacter Display using Serial Access Mode

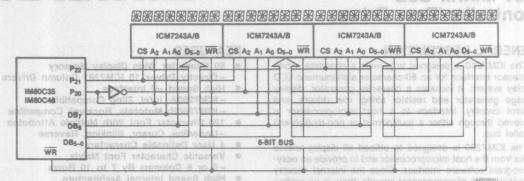
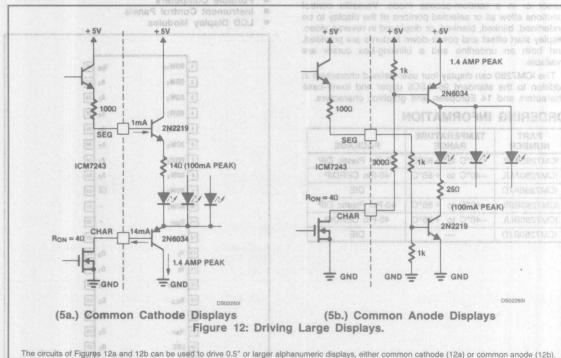


Figure 11: Random Access 32-Character Display in IM80C48 system.

One port line controls A2, other two are CS lines. 8-bit data bus drives 6 data and 2 address lines. MODE should be GrouNDed on each part.





#### GENERAL DESCRIPTION

The ICM7280 is designed to provide a complete microprocessor interface for an 80-character alphanumeric LCD display system. It includes a character generator, display voltage generator and resistor string, row drivers, and control circuitry. Interface to a host microprocessor is achieved through either a multiplexed or non-multiplexed parallel bus.

to As As Days Well CS As As As De-

The ICM7280 is designed to offload all display-related tasks from the host microprocessor and to provide an easy-to-program software interface. Since the internal circuitry operates at full microprocessor speeds, there is no waiting for completion of internal operations. Testing of a "Busy" flag, when characters or commands are written, is not required.

Character data can be loaded with an auto-incremented cursor or in a random-access mode. Versatile control functions allow all or selected portions of the display to be underlined, blinked, blanked, or displayed in reverse video. Display start offset and power-down features are provided, and both an underline and a blinking-box cursor are available.

The ICM7280 can display four user-defined characters in addition to the standard 96 ASCII upper and lower-case characters and 14 European and graphics characters.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE		
ICM7280AIPL	-40°C to +85°C	40-Pin Plastic DI		
ICM7280AIJL	-40°C to +85°C	40-Pin CERDIP		
ICM7280A/D	nac §	DIE		
ICM7280BIPL	-40°C to +85°C	40-Pin Plastic DIP		
ICM7280BIJL	-40°C to +85°C	40-Pin CERDIP		
ICM7280B/D	- 34	DIE		

#### FEATURES A A SO

- 80 Character Wide Display Memory
   Directly Drives 10 ICM7281 Column Drivers
- High Speed μP Interface
  - ICM7280A: Intel, Zilog Compatible
- ICM7280B: Motorola, Rockwell Compatible
- 120 Character Font With Multiple Attributes
   Underline, Cursor, Blinking, Reverse
- 4 User Definable Characters
- Versatile Character Font Matrix
   5 or 6 Columns By 7 to 10 Rows
- High Speed Internal Architecture
   No Busy Flag Needed

#### APPLICATIONS to .. A stortings entil frog and

- Battery Hand-Held Terminals
- Portable Computers
- Instrument Control Panels
- LCD Display Modules

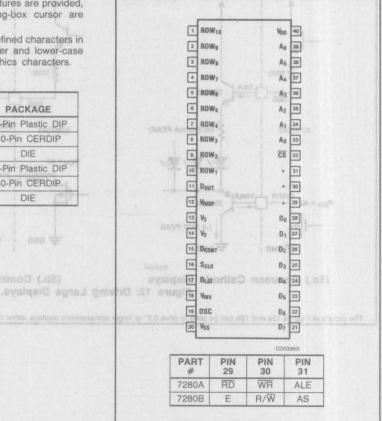
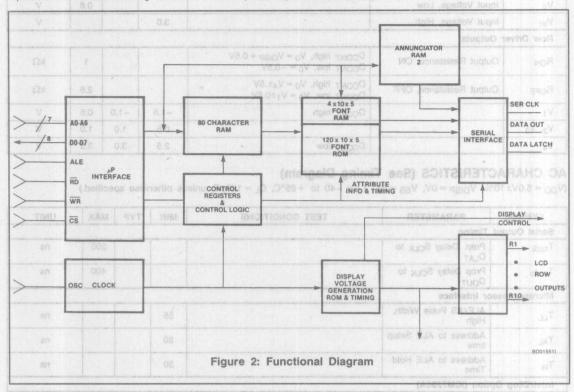


Figure 1: Pin Configuration

Supply Voltage (VDD - VSS)+6.5V	Opera
Display Voltage (VDD - VDISP)+ 12V	Storag
Input VoltageVSS-0.5V to VDD+0.5V	Lead
Power Dissipation500mW @ 70°C	

......

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## ELECTRICAL CHARACTERISTICS

 $(V_{DD} = 5.0V \pm 10\%, T_A = -40 \text{ to } \pm 85^{\circ}\text{C}, V_{DISP} = V_{DD} - 8V, V_{SS} = 0V, \text{ unless otherwise specified.})$ 

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
IIL sa	Input Leakage 06	Address/Data pins high impedance 0 < V <sub>IN</sub> < V <sub>DD</sub>		-10	W of at	+10	μΑ
Iss an	Supply Current	Osc open ckt, V <sub>IL</sub> = 0V, V <sub>IH</sub> = V <sub>DD</sub>	H	stsC bils	V of CA	2.5	mA
ISTBY	Shutdown Current	V <sub>IL</sub> = 0V, V <sub>IH</sub> = V <sub>DD</sub>		bloH sis	90 UA	100	μΑ
VSUPP	Operating Voltage Range		7	4.5	E Setup	1.5.5	Ves
fosc	Osc. Frequency	Osc. open ckt.	(80)	0.2	oifqO (f	1.00	MHz
Serial Out	outs da			guta8 3	dress to	hА	bel
VOL	Output Voltage, Low	I <sub>OL</sub> = 1mA	1	Note 3	of seaso	1.0	V
8/1	- 06				90	niT	da

## ICM7280



#### **ELECTRICAL CHARACTERISTICS (CONT.)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH OF	Output Voltage, High		V <sub>DD</sub> - 1.0	10V - (	(V) et	splay Valds
Data I/O,	uP Interface Inputs	SOOWAN @ 19.0			noits	are vollege were Diago
VOL and the	Output Voltage, Low	I <sub>OL</sub> = 1.6mA	Josed A" your	se listed	0.4	V
VOH	Output Voltage, High	I <sub>OH</sub> = 400μA seedl avode anobilindo usdo	2.4	device a	int to not	V
VIL	Input Voltage, Low		A THE STATE OF THE		0.8	٧
VIH	Input Voltage, High		3.0			V
Row Drive	r Outputs	<b>特别是他的现在分词是是是一种的</b>	Y			
RON	Output Resistance, ON	$D_{CONT}$ high, $V_0 = V_{DISP} + 0.5V$ $D_{CONT}$ low, $V_0 = -0.5V$			1	kΩ
ROFF	Output Resistance, OFF	DCONT high, $V_0 = V_4 \pm .5V$ DCONT low, $V_0 = V_1 \pm 0.5V$			2.5	kΩ
V <sub>1</sub>	.	DCONT high	-1.5	-1.0	0.5	V
V <sub>2</sub> , V <sub>3</sub>	JAIRSQ	ARTOARAN OR SAN	0.5	1.0	1.0	V
VATALATAD	BORNERS	DCONT low	2.5	3.0	3.5	V

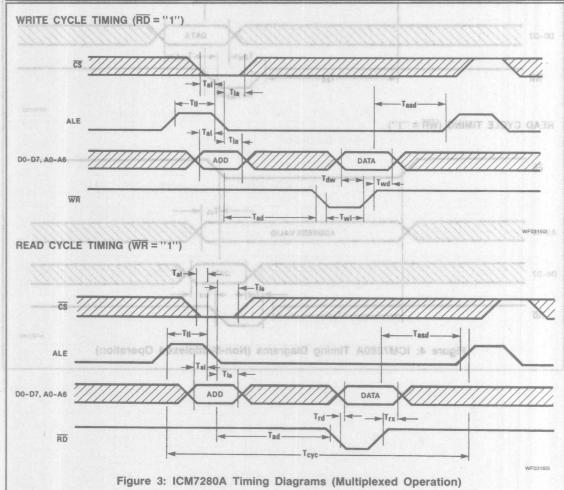
### AC CHARACTERISTICS (See Timing Diagram)

 $(V_{DD} = 5.0V \pm 10\%, V_{DISP} = 0V, V_{SS} = 0V, T_A = -40 \text{ to } +85^{\circ}\text{C}, C_L = 150 \text{pF, unless otherwise specified.})$ 

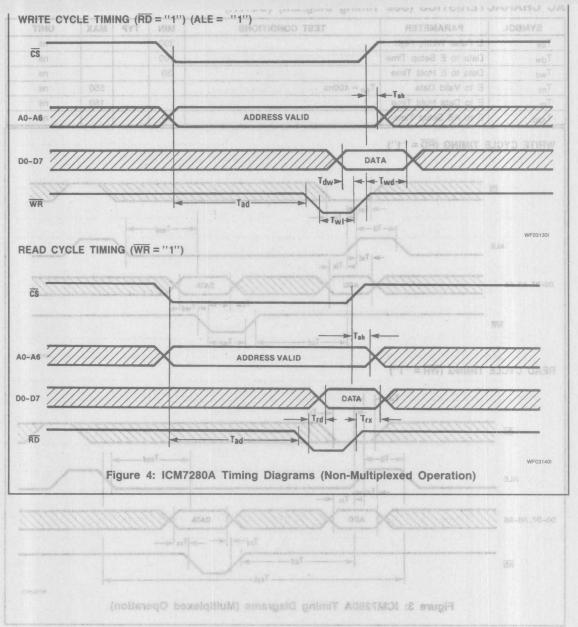
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Output	Timing					
T <sub>scdl</sub>	Prop. Delay S <sub>CLK</sub> to D <sub>LAT</sub>	, and an arrang			200	ns
T <sub>scdo</sub>	Prop Delay S <sub>CLK</sub> to D <sub>OUT</sub>	YAJERI BOATRON			400	ns
Microprocess	sor Interface	ORBET & BOR				
TLL	ALE/AS Pulse Width, High	Lanca de la constanta de la co	55			ns
T <sub>AL</sub>	Address to ALE Setup time		30			ns
T <sub>la</sub>	Address to ALE Hold Time	Figure 2: Functional Disgram	30			ns
Intel/Zilog O	ption (ICM7280A)					
Tad	Address Setup Time	201	50	DARA	MO I	An inshall
Tah	Address Hold Time		30	ROTTE	BETS	AGA NS
Twl	WRITE Pulse Width, Low	VDISP = VDD - BV, VSS = QV, unless o	100	) Ob=	AT.N	ot #Vons= gaV
T <sub>dw</sub>	Data to WRITE Setup	TEST CONDITIONS	150	ARAME		Johns
Twd	Data to WRITE Hold Time	Address/Data pins high impedence	30	skage	eJ Juq	ns ji
Trd	READ to Valid Data	Osc open old V <sub>n</sub> = 0V V <sub>n</sub> = V <sub>O</sub>		leterani d	550	ns
T <sub>rx</sub>	READ to Data Hold Time	Vit = 0V, Vit( = Vit)		remail r	150	ns
Tasd	ALE Setup Time	William Control of the Control of th	60	patieV s	repratin	nsusV
Motorola/Ro	ckwell Option (ICM7280B	Osc. open ckt. (		quency	isc. Fre	oant-
Tad	Address to E Setup Time		50		= =	Serian Output
Tah	Address to E Hold Time	Ant = 101	30	onage,	/ Jugion	ns

#### AC CHARACTERISTICS (See Timing Diagram) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tee	E Pulse Width, High	Vi	200	Economic (se	entylem kyronez	ns
T <sub>dw</sub>	Data to E Setup Time	Panisappasa a albanias non upatara satura	100			ns
T <sub>wd</sub>	Data to E Hold Time		30			ns
T <sub>rd</sub>	E to Valid Data	T <sub>ee</sub> = 400ns			550	ns
T <sub>rx</sub>	E to Data Hold Time	property and the second of the second	something and	agranding right	150	ns
Tasd	E to AS Setup Time	ADDRESS VALID	60	1991	1111	ns A-o







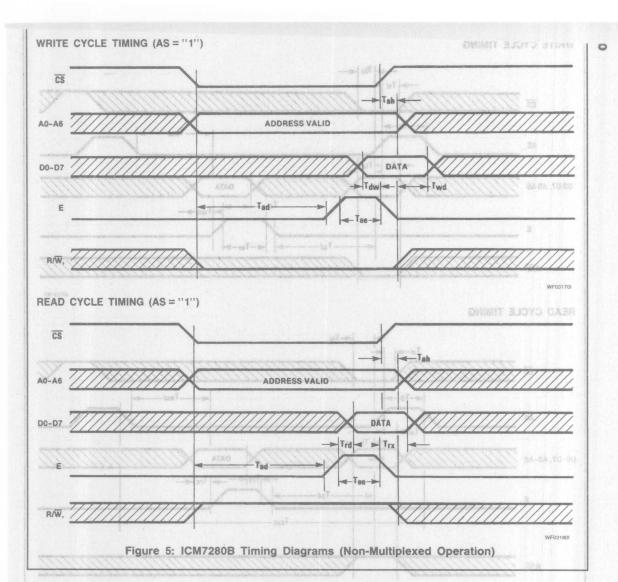
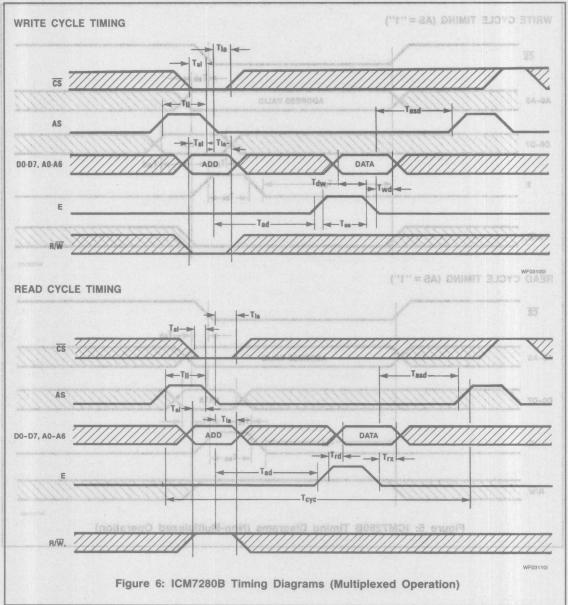


Figure 6: ICMY280B Timing Disgrams (Multiplexed Operation)

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ICM7280



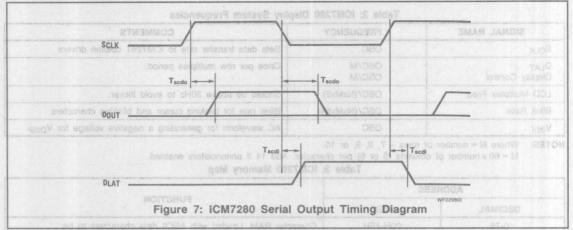


Table 1: Pin Descriptions

	Table 1:	Pin Descriptions
SIGNAL	PIN	DESCRIPTION
ROW10-1	1-10	LCD row drivers
Dout	11	Serial data (OPI) 0 telaiget
VDISP	12	Negative LCD supply voltage
V2, V3	13, 14	LCD column voltage
DCONT	15	Column driver control output
SCLK	16	Serial data clock output
DLAT	17	Row data latch output
V <sub>INV</sub>	18	Negative voltage generator clock
OSC	19	Oscillator input and vitral baseling
Vss	20	Digital ground
D0-D7	28-21	Data I/O
RD(7280A) E(7280B)	29 29	Read input
WR(7280A) R/WR(7280B)	30	Write input Read/write input
ALE(7280A) AS(7280B)	31 31	Address latch enable Address strobe
CSot retoansi	32	Chip select input
A0-A6	39-33	Address inputs to all solice mobiles
V <sub>DD</sub>	40	Positive digital and LCD supply voltage

## DETAILED DESCRIPTION on a spation blodecut Hardware Interface and 01 and oats 065 MAOI and

Figure 1 is a simplified block diagram of the ICM7280. It is a dedicated hardware IC and the speed of data entry and command processing is limited only by gate delays. Unlike other display controllers, the ICM7280 will not "go busy" for milliseconds at a time while processing data or commands.

#### Microprocessor Bus Interface

There are two versions of the ICM7280. The ICM7280A has  $\overline{\text{WR}}$  and  $\overline{\text{RD}}$  pins, as well as ALE and  $\overline{\text{CS}}$ . This version can be interfaced to standard multiplexed or non-multiplexed data buses of parts such as the 8085, Z80, 8088 and other microprocessors. The ICM7280B has R/ $\overline{\text{W}}$ , E and AS pins instead of  $\overline{\text{WR}}$  and  $\overline{\text{RD}}$  and ALE. The ICM7280B is intended for use on 6800 and 6500 family buses.

To use the ICM7280 on a multiplexed bus, tie the A0-A6 lines to the D0-D6 lines and ALE/AS driven with the system address latch enable or strobe signal. For a non-multiplexed bus, A0-A6 should be connected to the least significant address lines, D0-D7 connected to the data bus and ALE/AS tied high. The only external circuitry needed is a chip select or address decoder. The ICM7280 uses an address space of 128 bytes.

#### ICM7281 Data Interface

The ICM7280 Row Drivers require ICM7281 Column Drivers to operate an LCD display. Three lines are used to load data serially into the ICM7281 column drivers,  $D_{OUT}, S_{CLK},$  and  $D_{LAT}.$  The data is latched and shifted with each negative going edge of  $S_{CLK},$  and the data is transferred from the ICM7281 shift register to its latches with the negative going edge of  $D_{LAT}.$  The frequency of the  $S_{CLK}$  is set by the oscillator frequency of the ICM7280 and is normally about 600kHz.

#### Oscillator

The ICM7280 oscillator will free run at 600kHz in die form, when not loaded with any capacitance. With 15pF of external capacitance at pin 19, the frequency will be about 250kHz. Figure 8 shows the relationship between oscillator period and the value of Cexternal. Table 1 shows the relationship between the oscillator frequency and various display system signals and features. Standard CMOS logic gates can be used to overdrive the oscillator to control frequency. A suitable frequency can also be derived by dividing down the host processor's clock.

SIGNAL NAME	FREQUENCY	COMMENTS
S <sub>CLK</sub>	OSC	Sets data transfer rate to ICM7281 column drivers
D <sub>LAT</sub> Display Control	OSC/M OSC/M	Once per row multiples period.
LCD Multiplex Freq.	OSC/(NxMx2)	Should be above 30Hz to avoid flicker.
Blink Rate	OSC/(NxMx64)	Blink rate for blinking cursor and blinking characters
VINV	OSC	AC waveform for generating a negative voltage for VDISP

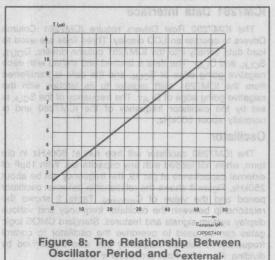
NOTES: Where N = number of rows - 7, 8, 9, or 10.

M = 80 x number of columns (5 or 6) per character. Add 14 if annunciators enabled.

Table 3: ICM7280 Memory Map

ADDRESS		1 November 19410		
DECIMAL	menge HEX nimiT hu	FIGURE A: ICM7280 Serial Outs		
0-79 908119	ni sud rosesporgo	Character RAM. Loaded with ASCII data characters to be displayed. Address 0 is the leftmost character (assuming the Preset Display Position Register is 0.)		
80-119 Soles and a soles and a		Font RAM. Holds bit pattern for four user-definable characters. See Table 4.		
ne 8808 08 120a08 aru as	78H	Instruction register 0 (IR0)	De	
72808 ha 121 W. E and Al	Olent 79H orgonom	Instruction register 1 (IR1)	gV	
122	7AH	Instruction register 2 (IR2)	SV	
123		Cursor Register (IR3)	QQ.	
natava adt di 124 e orb 8A13	JA bas ser7CH -00 ant of	Preset Display Position Register (IR4)	05	
125	7DH	Annunciator Register 1 (AR1)	ule.	
But bas aud 26% art of b		Annunciator Register 2 (AR2)	MY	
127	7FH	Cursor-Addressed Entry Register	20	

NOTE: See Table 6 for more detail about addresses 120-127 (78H-7FH).

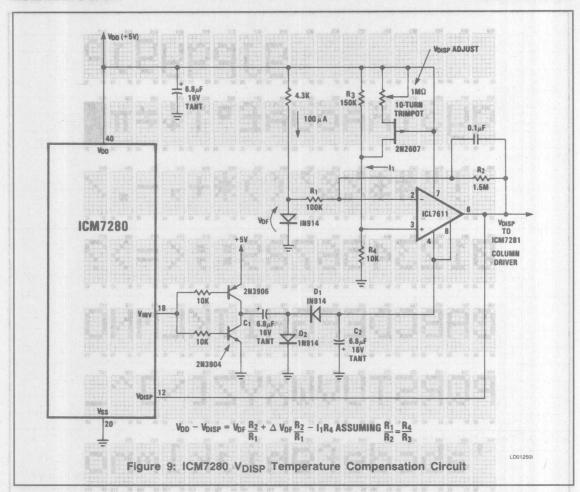


#### Display Interface

The ICM7280 will support a dot matrix LCD display which has 7, 8, 9, or 10 rows, and either evenly-spaced columns or a space after every fifth column. If the display has evenly-spaced columns, then 6 columns per character should be selected and the sixth column is always blank. If the display provides a blank after every fifth column, then 5 columns per character should be selected. The character font is automatically changed to take advantage of all rows. The ICM7280 will automatically use one of the 6 evenly-spaced columns for a space.

The ICM7280 can drive LCD displays with threshold voltages up to 2.5 volts. There is no minimum display threshold voltage since V<sub>DISP</sub> can be above V<sub>SS</sub>.

The ICM7280 also has 10 onboard row drivers designed to handle large dot matrix displays. These drivers provide fast slew rates, and have a minimum offset voltage.



#### Display Voltage Generator

The ICM7280 not only has an onboard resistor string to generate the required V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>, and V<sub>4</sub>, but also has an output that assists in generating a negative voltage for V<sub>DISP</sub>. The V<sub>INV</sub> pin is a low-impedance output that swings from V<sub>DD</sub> to V<sub>SS</sub> at the oscillator frequency. The circuit of Figure 9 connected to the V<sub>INV</sub> pin generates a temperature-compensated V<sub>DISP</sub>. Diodes D<sub>1</sub> and D<sub>2</sub>, with capacitors C<sub>1</sub> and C<sub>2</sub> form a charge-pump negative voltage generator. The ICL7611 CMOS op-amp and its associated circuitry form an adjustable temperature compensated voltage source that provides V<sub>DISP</sub> to the ICM7280, as well as the ICM7281 column drivers. Temperature compensation for V<sub>DISP</sub> is necessary because the threshold voltage of LCD fluids have a pronounced negative tempco.

#### SOFTWARE INTERFACE

Table 3 provides a memory map of the ICM7280. The ICM7280 uses 128 bytes of memory space: 80 bytes for character data storage, 2 bytes for 14 independent annunci-

ators or flags, 40 bytes for storing 4 user-programmable characters, 5 bytes for control registers, and one dummy address to identify cursor-addressed character entry.

#### Character RAM

Data may be entered in a random-access mode by simply writing to the desired character address. Address 0 corresponds to the leftmost character of the display, and address 79 corresponds to the rightmost character (assuming the Preset Display Position register has been loaded with a 0). Block moves or other high-speed data transfers can be used to move data from the host system's RAM or ROM to the ICM7280's character RAM. Character data format is standard ASCII for the 96 upper and lower case characters, with the eighth data bit ignored. As shown in Figure 10, the ICM7280 Character Font Table, the display controller additional European and graphics characters. The characters 08 through 17 are alternate lower case characters that are used with 8, 9, and 10 row displays.



ure-compensuited Vpispe. Diodes Dy and Dg, with capaci.

78 corresponds to the leftmost character of the display, and address one of the display and address of the Compensuity register with a Compensuity of the Compensuity of the compensuity

Figure 10: ICM7280 Character Font

oursor location will wrep around

Table 4: Font RAM for User-Definable Characters

JAROW HO CHUC	ASCII CHARACTER 0 FONT ADDRESS		ASCII CHARACTER 1		ASCII CHARACTER 2 FONT ADDRESS		ASCII CHARACTER 3 FONT ADDRESS	
	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex
Row 1 (top row)	80	50H	90	5AH	100	64H	19110810	of 6EH
character data from the hos				BOM WIT .	ersigen tas	eilder tid s	ai r <del>o</del> laiger	ORI TONT
to a senal data stream for the					A .notterequ			
and provides the row drive	nn drivers,	1281 colui	T ICM		as ed at			Control of the contro
system firming and control. The	eral) display	ages End ov	Hov T		stid fee fliw			
display system is typically (	into the moite	er consum	wog =		olear bit 4			
eration and 5 microwa7swoRer	86	56H	96	60H	106	6AH	b416 Hs	for 74H and
ta and control setup).	retainting da	jud) Triwob	urla -	agristers that	set/reset r	sters are bil	peR Totalor	unnA enT
Row 10 (bottom row)	89	59H	99	63H	109	6DH	119	77H

display module and a module with fewer of In addition to the 120 characters available in the built-in character ROM, 4 characters may be user-defined. Table 4 shows the mapping between the Font RAM and the userdefined character font. An example of an additional character is provided in Figure 11. Note that addresses 80-119 (50H-77H) hold 5 bit words that correspond to the bit pattern of the four user-definable characters, such that each 5 bit word defines the pattern for one row of the character. The LSB corresponds to the right-hand dot. Each character uses 10 words, with the lowest address representing the top row. Once defined, these characters are treated the same as the predefined characters from the Font ROM. Enter ASCII data 0, 1, 2, or 3 into Character RAM to call up one of those characters.

display may be left out. This means that an

CAUTION: The ICM7280 should not be left in the reset

made for extended penods, because in this condition there

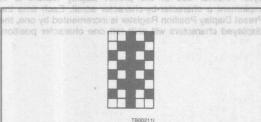


Figure 11: An Example of a User-Defined Character

#### Instruction and Annunciator Registers

Table 5 details the bit assignments of the control registers. All registers are write-only registers.

Attributes are enabled by bit 5 of Instruction Register IR2, at address 122 (7AH). Blinking, underlined, and reverse video characters are controlled by attribute characters in the character RAM. These attribute characters are displayed as blanks, but signal the ICM7280 that the characters to the right of the attribute character are to be displayed with one of the three attributes (5 = underline, 6 = reverse video, and 7 = blinking). Each attribute is cancelled by a second occurence of the attribute character. The entire display can be blinked or blanked by setting the appropriate bits in IRO.

Table 5: ASCII Character 0 Example

may also be incremented or decremented by writing the appropriate instructions to IR2 at address 122 (ZAH). The

	Font Ac	ddress	HT THEY Dat	a edi lo A
Row	Decimal	Hex	Decimal	- Hex
1	80	50H	5	05H
2	81	51H	not 14 leni	0EH
081V3 00	82	52H	21 115 0	15H
48	83	53H	14	0EH
9 5 9	84	54H	2181037	15H
6	85	55H	ugo 14uld br	0EH
iewo7, no	gu 1861 eus	39 56H	or bits 12 copt	dei 15H A
1 8	Harris Committee of the		1 8 OF 4 10 8 1	04H
98 890 1	d ell 88 of ne	58H	egiste <b>4</b> s can	04H
10	1 89 asolo	59H	enild41 noil	OEH od

The starting point of the display can be offset by changing the value stored in IR4, the Preset Display Position Register, at address 124 (7CH). The number in this register (usually 0) specifies the address of the character in character RAM that will appear at the leftmost position on the display. For example, a 5 in this register causes the sixth character in the RAM to be displayed at the left end of the display. The Preset Display Position Register can be loaded with a value, or it can be incremented and decremented by writing to bits 2 and 3 of IR2, address 122 (7AH). The Preset Display Position Register will automatically wrap around from 79 to 0 when incremented, and wrap around from 0 to 79 when decremented past 0.

CAUTION: If a number greater than 79 is loaded into the Preset Display Position Register, display multiplexing stops. The LCD can be damaged if left in this condition for an extended period of time.

The Cursor Register determines the location of the cursor on the display, depending upon value in the Preset Display Position Register. If for example, the Cursor Register is set to 5 and the Preset Display Register is set to 0, the cursor will then be displayed in the 6th character of the display. If, however, the Cursor Register is set to 14 and the Preset Display Position Register is also set to 14, then the cursor will be displayed in the leftmost character position. If data is written to address 127 (7FH), the data is entered at the current location of the cursor and the cursor position is incremented. The cursor position may be directly set by writing to Cursor Register address 123 (7BH). The cursor may also be incremented or decremented by writing the appropriate instructions to IR2 at address 122 (7AH). The cursor location will wrap around from 79 to 0 or vice versa when incremented or decremented. A number greater than 79 written to the Cursor Register causes no cursor to be displayed, but the ICM7280 will otherwise function normally. If bit 4 of IR1 at address 121 (79H) is at "1", then all characters to the right of the cursor are blanked but the data in the character RAM is retained.

The IRO register is a bit set/reset register. The MSB selects either set-(1) or reset (0) operation. A "1" in any other bit position selects that bit to be set/reset. For example, a bit pattern of 10011001 will set bits 0, 3 and 4, while a bit pattern of 00010000 will clear bit 4. Unselected bits are not affected.

The Annunciator Registers are bit set/reset registers that operate similarly to IRO. When used with the ICM7281 column drivers, bit 0 of Annunciator Register 1 will be the last bit shifted out, and will appear at the column 1 output of the ICM7281. Bit 6 of Annunciator Register 2 is the first annunciator bit to be shifted out, and will appear on column 14 of the ICM7281. The annunciator outputs, if enabled, appear on all rows in columns 1-14. Annunciators are enabled by bit 7 at IR1.

Bit 6 of instruction register 2 resets all instruction registers and annunciator registers, as well as the Cursor Register and Preset Display Position Register. Bit 6 of Instruction Register 2 also resets and stops the display multiplex and blink counters.

All register bits except bit 6 of IR2 are reset upon powerup. Since bit 6 of IR2 is indeterminate at power-up, and the instruction registers cannot be written to while bit 6 is set, the initialization routine should first clear bit 6 before the other registers of the ICM7280 display controller, are accessed. When normal operation resumes after bit 6 of IR2 is cleared, the attributes will be off, the cursor will be present at 0, and the 5 x 7 character format will be engaged.

character RAM that will appear at the tettmost position on the display. For example, a.5 in this register causes the sixth character in the RAM to be displayed at the left end of the display. The Preset Display Position Register can be loaded with a value, or if can be incremented and decremented by militing a value, or if can be incremented and decremented by Display Position Register will automatically wrap around from 19 to 0 when incremented, and wrap around from 0 to 79 when decremented past 0.

CAUTION: If a number greater than 79 is loaded into the Proset Display Position Register, display multiplaying stops The LCD can be damaged if left in this condition for an extended period of time.

The Cursor Register determines the location of the cursor on the display, depending upon value in the Preset Display. Position Register, it is earlied to 5 and the Preset Display Register is set to 0, the cursor to 5 and the Preset Display Register is set to 0, the cursor lowever, the Cursor Register is set to 14, and the Preset Display Position Register is also set to 14, then the cursor will be displayed in the refinost character position. If data is written to address 127 (7FH), the data is entered at the cursor to called the cursor position may be directly set by writing to Cursor Register address 123 (7FH). The cursor incremented. The cursor position may be directly set by writing to Cursor Register address 123 (7FH). The cursor position is writing to Cursor Register address 123 (7FH). The cursor

**CAUTION:** The ICM7280 should not be left in the reset mode for extended periods, because in this condition there is a DC bias on the liquid crystal display which can permanently damage it.

## 80 CHARACTER LIQUID CRYSTAL DISPLAY SYSTEM

Figure 10 shows a complete 80 character Intel/Zilog compatible display system without annunciators. The ICM7280A receives ASCII character data from the host microprocessor, converts it to a serial data stream for the ICM7281 column drivers, and provides the row drive voltages and overall display system timing and control. The power consumption of this display system is typically 6 milliwatts during normal operation and 5 microwatts when shutdown (but retaining data and control setup).

If less than 80 characters are desired, the ICM7281's that would normally drive the right-hand characters of the display may be left out. This means that an 80 character display module and a module with fewer characters can have exactly the same hardware and software interface, except that extra ICM7281's are missing from the module with fewer characters.

The Preset Display Position Register is most useful when the LCD system has fewer than 80 characters. For example, if the display has only 16 characters, all 80 characters stored in RAM can be displayed by first setting the Preset Display Position Register to 0, waiting 2 seconds, setting it to 16, waiting 2 seconds, and so forth, on up through a character preset of 64. The host processor would need to do just one write of the data and then use one command to write to the Preset Display Position Register. This requires much less time than shifting all of the data around byte by byte. Another use of the preset display feature is to implement a character-by-character scroll. Each time the Preset Display Position Register is incremented by one, the displayed characters will shift left one character position.

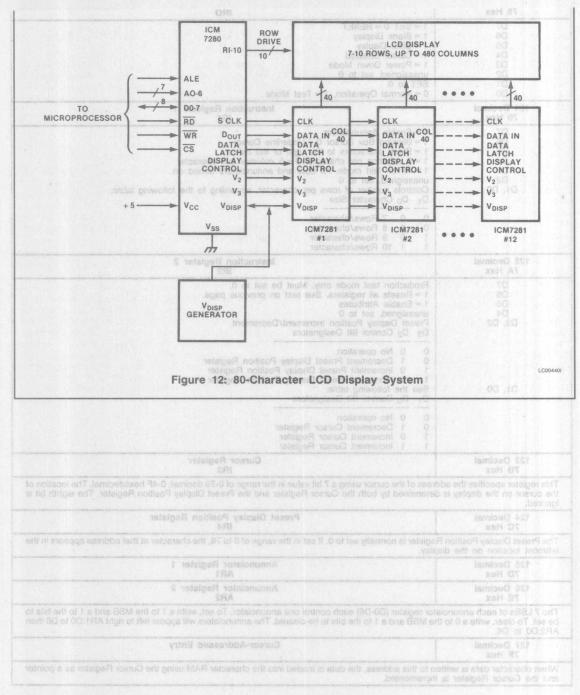


Figure 11: An Example of a User-Defined Character

Instruction and Annunciator Registers

Attributes are enabled by bit 5 of Instruction Register IR2, at address 122 (7AH). Blinking, underlined, and reverse video characters are controlled by attribute characters in the obaracter RAM. These attribute characters are displayed as blanks, but signal the ICM7280 that the character to the right of the attribute character are to be displayed with one of the trase attributes (5 = underline, 6 = reverse video, and 7 = birthog). Each attribute is cancelled by a second occurrence of the attribute character. The entire





ICM7280



Table 6: Instru	ction and	Annunciator	Registers
-----------------	-----------	-------------	-----------

120 Decimal 78 Hex	Instruction Register 0 IRO
D7 D6 D5 D4 D3 D2 D1	1 = SET 0 = RESET 1 = Blank Display 1 = Blink Display 4 = Cursor Enabled 1 = Power Down Mode unassigned, set to 0 SET to 0 0 = Normal Operation, 1 = Test Mode
121 Decimal 79 Hex	Instruction Register 1
D7 D6 D5 V D4 D3 D2 V D1, D0	1 = Enable Annunciators 1 = Blinking Box Cursor 0 = Underline Cursor 1 = Blank characters to the right of the cursor 1 = 6 columns per character 0 = 5 columns per character 1 = All on test mode. All dots and annunciators turned on. unassigned, set to 0 Controls number of rows per character, according to the following table:  D1 D0 Character Size  0 0 7 Rows/character 0 1 8 Rows/character 1 0 9 Rows/character 1 1 10 Rows/character
122 Decimal 7A Hex	Instruction Register 2
D7 D6 D5 D4 D3, D2	Production test mode only. Must be set to 0.  1 = Resets all registers. See test on previous page.  1 = Enable Attributes unassigned, set to 0 Preset Display Position Increment/Decrement  D <sub>3</sub> D <sub>2</sub> Control Bit Designators
D1, D0	0
	0 0 No operation 0 1 Decrement Cursor Register 1 0 Increment Cursor Register 1 1 Increment Cursor Register
123 Decimal 7B Hex	Cursor Register IR3

This register specifies the address of the cursor using a 7 bit value in the range of 0-79 decimal, 0-4F hexadecimal. The location of the cursor on the display is determined by both the Cursor Register and the Preset Display Position Register. The eighth bit is ignored.

404 Bardard	Barrell Birder Barrier Barriet
124 Decimal	Preset Display Position Register
7C Hex	IB4

The Preset Display Position Register is normally set to 0. If set in the range of 0 to 79, the character at that address appears in the leftmost location on the display.

125 Decimal	Annunciator Register 1
7D Hex	AR1
126 Decimal	Annunciator Register 2
7E Hex	AR2

The 7 LSBs of each annunciator register (D0-D6) each control one annunciator. To set, write a 1 to the MSB and a 1 to the bits to be set. To clear, write a 0 to the MSB and a 1 to the bits to be cleared. The annunciators will appear left to right AR1:D0 to D6 then AR2:D0 to D6.

127 Decimal	Cursor-Addressed Er	ntry
7F Hex		

When character data is written to this address, the data is loaded into the character RAM using the Cursor Register as a pointer and the Cursor Register is incremented.

## ICM7281 40-Column LCD Dot Matrix Display Driver

#### GENERAL DESCRIPTION

The ICM7281 LCD Dot Matrix Column Driver is designed to convert a serial data stream into drive signals for a multiplexed dot matrix LCD. Easily cascadable, up to 16 ICM7281's can be driven by one ICM7280 Intelligent Row Driver to make an 80 character dot matrix display. The ICM7281 also serves as both a Row Driver and Column Driver in LCD dot matrix graphics displays. The low output resistance and the 15V drive capability make it well suited for graphics displays with up to 256 x 256 dots (with 10pF/ dot capacitance).

The ICM7281 consists of a 40 bit shift register, a 40 bit latch and 40 level-shifters/drivers. The 4 display drive voltages are generated externally, usually by a Row Driver. A serial data interface is used to minimize the number of 15V VDISP pins needed for digital interfacing. A data Carry Output is included for cascading several ICM7281's to drive large LCD displays.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7281IPL	-40°C to +85°C	40-Pin PLASTIC DIP
ICM7281IJL	-40°C to +85°C	40-Pin CERDIP
ICM7281/D	00+ - 100	DICE

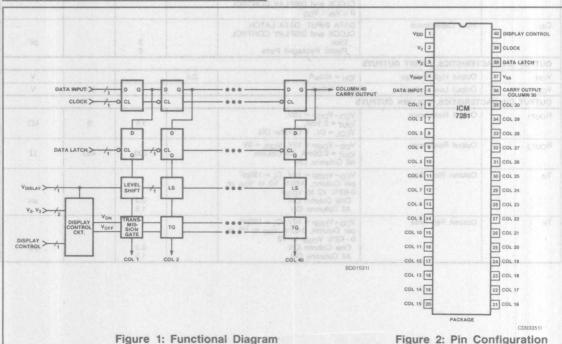


#### **FEATURES**

- 40 High Voltage LCD Column Drive Outputs
- Easy Interface - Serial Input Shift Register with Parallel Latch and Carry Outputs
- Directly Compatible with ICM7280 Row Driver - Up to 16 ICM7281's can be Driven by an ICM7280 with No External Components
- Low Resistance Outputs - Can Drive Both Columns and Rows of LCD Graphics Displays
- Will Drive 1.5V Threshold LCDs with Only Single 5V Supply - Can Drive Up to 4.5V Threshold LCDs with

#### **APPLICATIONS**

- Column Drivers For Dot Matrix Alphanumeric Displays Using ICM7280 Row Driver
- Row and Column Drivers For LCD Dot Matrix **Graphics Displays**
- Segment Driver For LCD Bargraphs and Annunciators
- Serial Input I/O Expander



-002

(Outline dwg. PL)

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Display Voltage (V <sub>DD</sub> – V <sub>DISP</sub> )	Operating Temperature Range40°C to +85°C
V2, V3VDISP to VDD	Storage Temperature Range65°C to +150°C
Input Voltage (Note 1)(VSS -0.3V) to (VDD +0.3V)	Lead Temperature (Soldering, 10sec)300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Due to the SCR structure inherent in any junction isolated CMOS device, connecting an input to any voltage greater than V<sub>DD</sub> or less than V<sub>SS</sub> may cause destructive device latch-up. If the input voltage can exceed the recommended range, the input should be limited to less than 1mA to avoid latch-up.

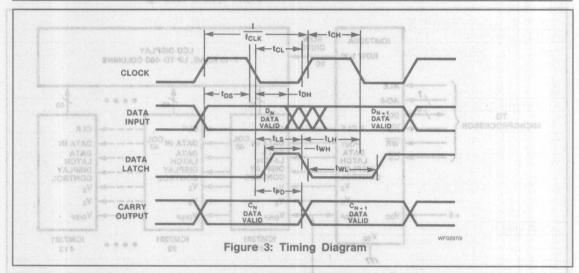
NOTE 2: This limit refers to that of the package and will not occur during normal operation.

**ELECTRICAL CHARACTERISTICS**  $(V_{DD} = 5V, V_{DISP} = -10V, V_2 = 1/3 (V_{DD} - V_{DISP}). V_3 = 2/3 (V_{DD} - V_{DISP}), V_{SS} = 0V, T_A = -40^{\circ}C$  to +85°C. Unless otherwise specified.)

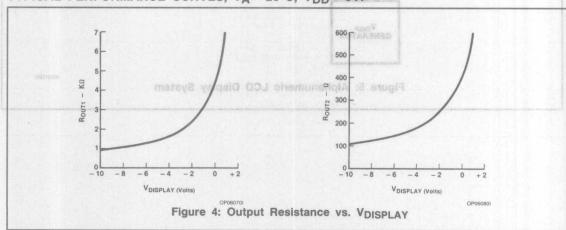
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARAC	TERISTICS AMOI	LADI IGGA REPLICAT	med elab	terfacing. A	or digital in	s neeced !
VSUPP	Operating Supply Range	Lateralia D	4.5	5.0	5.5	V
V <sub>DISP</sub>	Display Voltage	Displays	-10		V <sub>DD</sub>	V
Supply Current Quiescent Dynamic Oynamic		F <sub>CLK</sub> = 0 F <sub>CLK</sub> = 500kHz		.1 500	10 1000	μΑ
INPUT CHARACTI	ERISTICS	Principle 2007	PAUK	301	BAL	BESILLIM
V <sub>IH</sub>	Logic 1 Input Range	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	0.7V <sub>DD</sub>	0°89+	- 40°C 1	FOLK 28 LIPE
VIL	Logic 0 Input Voltage	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL	40-Pin C	D*88+ 3	0.3V <sub>DD</sub>	CMV2911H
IIN	Input Current	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL 0 < V <sub>IN</sub> < V <sub>DD</sub>	-10	0.01	+10	μА
CIN 10 1400 YALKON [8]	Input Capacitance	DATA INPUT, DATA LATCH, CLOCK and DISPLAY CONTROL Dice Plastic Packaged Parts		3 5		pF
OUTPUT CHARAC	TERISTICS, CARRY OUTPUTS		1517246			
Vон	Output High Voltage	I <sub>OH</sub> = 400μA	2.4	en grounding	02233	V
Volument	Output Low Voltage	I <sub>OL</sub> = 1.6mA		0 0-0-0	0.4	V
OUTPUT CHARAC	TERISTICS, COLUMN OUTPUT	S		0 CT - 10 C		
ROUT1	Output Resistance	V <sub>DD</sub> - V <sub>DISP</sub> = 10V, I <sub>OUT</sub> = 0.1mA, V <sub>COL</sub> = 0V, 1 Column ON		1.5	3	kΩ
ROUT2 Output Resistance		V <sub>DD</sub> -V <sub>DISP</sub> = 10V, V <sub>COL</sub> = 0V I <sub>OUT</sub> = 0.05mA per Column All Columns ON		200	400	Ω
T <sub>R</sub> ec. 60 00 00 00 00 00 00 00 00 00 00 00 00	Column Rise Time	V <sub>DD</sub> -V <sub>DISP</sub> = 10V, C <sub>L</sub> = 150pF per Column, 0-63% V3 to V <sub>DD</sub> or 0-63% V2 to V <sub>DISP</sub> One Column ON		0.3	T, I	μs
T <sub>F</sub> (\$1,00) (	Column Fall Time	All Columns ON  VDD-VDISP = 10V, CL = 150pF per Column, 0-63% VDD to V3 or 0-63% VDISP to V2 One Column ON All Columns ON	01	0.3 1.5	AV 10810	μs

**ELECTRICAL CHARACTERISTICS (CONT.)**  $(V_{DD} = 5V, V_{DISP} = -10V, V_2 = 1/3 (V_{DD} - V_{DISP})$ .  $V_3 = 2/3$   $(V_{DD} - V_{DISP})$ ,  $V_{SS} = 0V$ ,  $V_{DS} = 0V$ ,  $V_{$ 

SYMBOL	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
AC CHARACTER	RISTICS (See Timing Diagram)	tel COJ	In celso po	Aller Vision P	SHOULDED TO	nativis as	de el reteiro
T <sub>DS</sub>	Data Setup	FOL OUT	oldstinus ei	150	90	edt of stab	an ns
T <sub>DH</sub>	Data Hold	onados nor	ne (CM7281	10 97	0-2000	JTPUT and	0.00 ns.0
Twh	Data Latch Width, High	/ SV conV	CUTPUL	AF 250 and	100	ckaged part	enns eo
Iwa word Input	Data Latch Width, Low	agretixe be	mally used	on ens stug	500	nmulgo diti	non si non
Tusixelaithum p	Data Latch Setup	Each colui		400	250	INPUT TO	ns
TLAde ons lexe	Data Latch Hold	fruth table	eril mon the	b ratonard	130	Igni HOTAL	ns
FCLK	Clock Frequency	La surgiri	Oh lo atala	D.C.	100 2 10	DE edi ci	MHz
T <sub>CH</sub>	Clock High Period	s ent onn	Anna ean an	500	100	ne refft en	ns
TCL	Clock Low Period	MATE ARGES	ONE TO THE	500	150	art Iliaz etel	ns
T <sub>PD</sub>	Carry Prop Delay C <sub>I</sub>	= 15pF	100		200	350	ns ns



TYPICAL PERFORMANCE CURVES, TA = 25°C, VDD = 5V.



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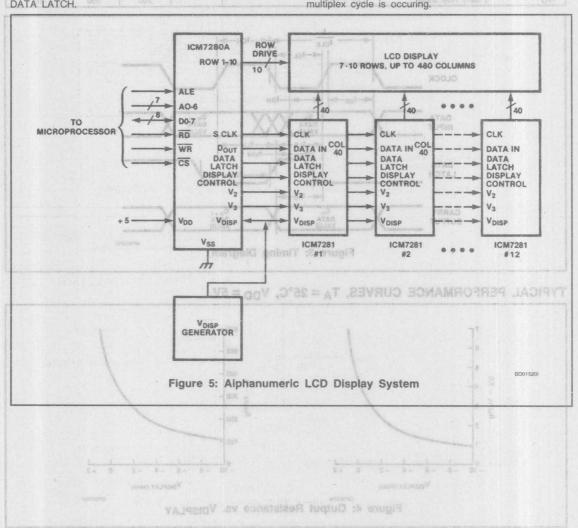
The data on DATA INPUT is shifted into the shift register with each falling edge of CLOCK. The data in the shift register is also shifted one bit with each falling edge of CLOCK. The data in the 20th and 40th registers is available as COL 20 OUTPUT and COL 40 OUTPUT on the ICM7281 dice. The packaged part has only one CARRY OUTPUT, which is the 30th column. These outputs are normally used as the DATA INPUT for an adjacent ICM7281.

The DATA LATCH input is used to transfer data from the shift register to the 40 bit latch, which consists of 40 negative edge-triggered D flip-flops. The data in the shift register is stored by the falling edge of DATA LATCH and this latched data will be held until the next falling edge of DATA LATCH.

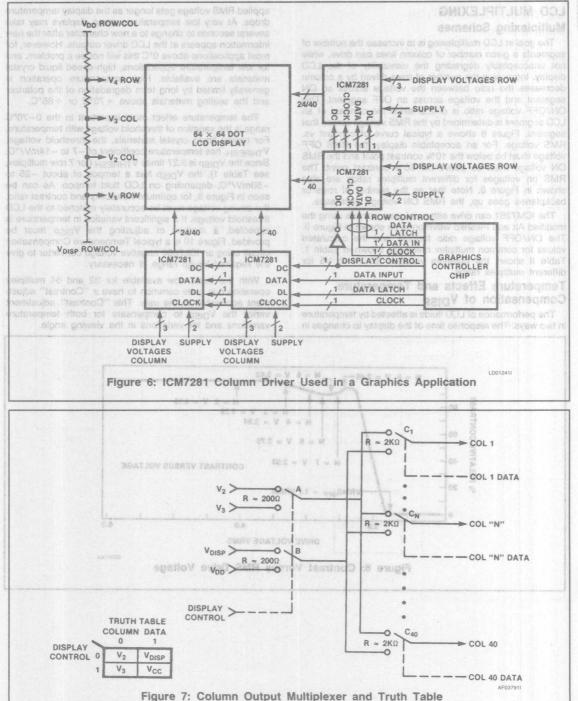
The DISPLAY CONTROL pin is used to convey multiplex timing information to the Column Drivers. This input is used as one of the two control inputs to the 1 of 4 analog multiplexer that drives each column output.

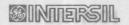
#### LCD Interface

The ICM7281 uses a modified Alt and Pleshko multiplexing scheme, in which the Column Driver uses 4 voltages:  $V_{\rm DD}$ , V2, V3, and  $V_{\rm DISP}$ . These drive voltages are generated externally, usually by the ICM7280 Intelligent Row Driver. Each column output is driven by an analog multiplexer. The truth table and a schematic of this multiplexer are shown in Figure 7. The column data is the data that is serially loaded into the shift register, then parallel loaded into the data latch. The DISPLAY CONTROL signal, generated by the ICM7280 Row Driver, tells the ICM7281 which half of the multiplex cycle is occurring.



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## LCD MULTIPLEXING Multiplexing Schemes

The goal in LCD multiplexing is to increase the number of segments a given number of column lines can drive, while not unacceptably degrading the viewability of the LCD display. Increasing the number of rows driven by a column decreases the ratio between the voltage across an ON segment and the voltage across an OFF segment. This ON/OFF voltage ratio is critical since the contrast of an LCD segment is determined by the RMS voltage across that segment. Figure 8 shows a typical curve of contrast vs. RMS voltage. For an acceptable display, the RMS OFF voltage must be below the 10% contrast point and the RMS ON voltage must be above the 50% contrast point. The RMS on voltages for different multiplex ratios are also shown in Figure 8. Note that as the number of rows or backplanes goes up, the RMS ON voltage decreases.

The ICM7281 can drive either columns or rows using the modified Alt and Pleshko waveforms as shown in Figure 9. The ON/OFF voltage ratio formula and the calculated values for common multiplex ratios are shown in Table 1. Table II shows the optimum voltages for V1 to V5 for different multiplex ratios.

## Temperature Effects and Temperature Compensation of VDISP

The performance of LCD fluids is affected by temperature in two ways. The response time of the display to changes in

applied RMS voltage gets longer as the display temperature drops. At very low temperatures some displays may take several seconds to change to a new character after the new information appears at the LCD driver outputs. However, for most applications above 0°C this will not be a problem, and for low temperature applications, high-speed liquid crystal materials are available. High temperature operation is generally limited by long term degradation of the polarizer and the sealing materials above +70°C or +85°C.

The temperature effect most important in the 0-70°C range is the variation of threshold voltage with temperature. For typical liquid crystal materials, the threshold voltage, V<sub>THRESH</sub>, has temperature coefficient of -7 to -14mV/°C. Since the V<sub>DISP</sub> is 3.27 times V<sub>THRESH</sub> (for 7 row multiplex, see Table 1), the V<sub>DISP</sub> has a tempco of about -25 to -50mV/°C, depending on LCD fluid tempco. As can be seen in Figure 8, for optimum viewability and contrast ratio, the driving voltage must be accurately matched to the LCD threshold voltage. If a significant variation in temperature is expected, a method of adjusting the V<sub>DISP</sub> must be provided. Figure 10 is a typical Temperature Compensation circuit using an ICL7660 negative voltage converter to give the required V<sub>DISP</sub> range, if necessary.

With the fluids now available for 32 and 64 multiplex operation it is quite common to have a "Contrast" adjustment accessible to the user. This "Contrast" adjustment varies the V<sub>DISP</sub> to compensate for both temperature variations and for variations in the viewing angle.

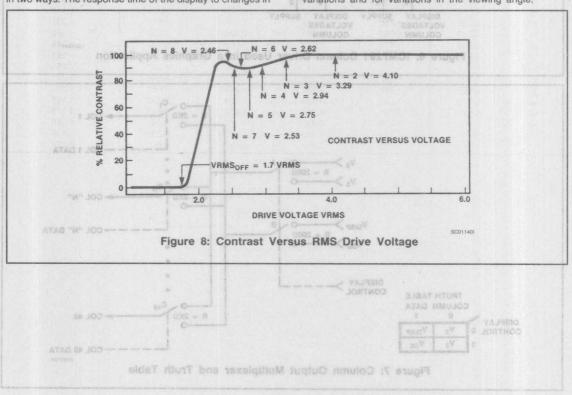


Table 1: Optimum Multiplex Drive 148339 & 7.14 Garagous

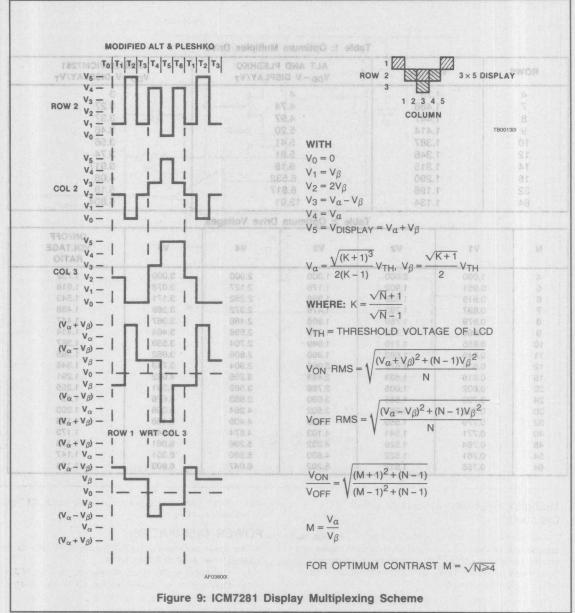
ROWS	Von/off	ALT AND PLESHKO VDD - V DISPLAY/VT	T2 T3	ICM7280/ICM7281 VDD - V DISPLAY/VT
4	1.73	4		3
7	1.488	4.74		3.27 s wos
8	1.447	4.97		3.37
9 (00.000)	1.414	5.20		3.46
10	1.387	MTIW 5.41		3.56
12	1.346	5.81		3.74
14	1.315	6.18		3.917
16	1.290	6.532		4.08
32	1.196	8.817		5.19 2 300
64	1.134	QV-sV = gV 12.01		6.804

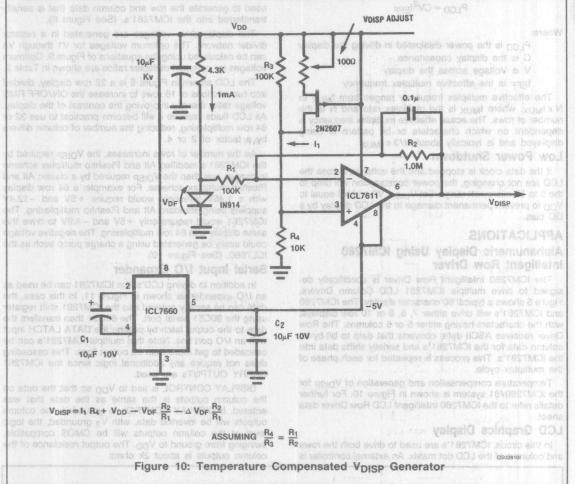
Table 2: Optimum Drive Voltages

N	V1 (+)	V2 Ε(1	+ ≥1) \/ V3	V4	V5	ON/OFF VOLTAGE RATIO
4	1.000	2.000	- X)S 1.000	2.000	3.000	v 1.732
5	0.951	1.902	1.176	2.127	3.078	1.618
6	0.919	1.838	1.332	2.252	3.171	1.543
7	0.897	1.793	1.476	2.372	3.269	1.488
8	0.879	1.759	1.608	2.488	3.367	1.447
9	0.866	1.732	1.732	2.598	3.464	1.414
0	0.855	1.710	1.849	2.704	3.559	1.387
1	0.846	1,692	1.960	2.806	3.652	1.365
2	0.838	1.677	2.066	2.904	3.743	1.346
6	0.816	1.633	2.449	3.266	4.082	1.291
0	0.802	1.605	2.786	3.589	4.391	1.255
4	0.793	1.585	3.090	3.883	4.676	1.23
0	0.782	(1.564)	3.502	4.284	5.066	1.203
2	0.779	1.559	3.629	4.409	5.188	1.196
0	0.771	1.541	4.103	4.874	5.645	1.173
8	0.764	1.529	4.332	5.296	6.061	- 1.156
4	0.761	1.522	4.830	5.590	6.351	- V 1.147
4	0.756	1.512	5.292	6.047	6.803	- 6 V 1.134

Figure 9: ICM7281 Display Multiplexing Scheme

FOR OPTIMUM CONTRAST M = VINSE





## Multiplex Rate and Maximum Drive Capability

The minimum multiplex rate is determined by the response time of the LCD. To avoid flicker, the multiplex rate should be above 30Hz. The maximum multiplex rate is determined by power dissipation limits and the drive capability of the ICM7281.

The drive capability of the ICM7281 indirectly sets the upper limit of the multiplex rate. The absolute maximum limit of DC voltage across an LCD is usually specified as 50mV. As the multiplex rate increases, any asymmetry in the rise and fall times will cause a DC offset, in addition to any offset caused by V2 and V3 not being exactly symmetrical with respect to V<sub>DISP</sub> and V<sub>DD</sub>. The ICM7281 was designed to have equal rise and fall times, as well as low resistance drivers which make the rise and fall times short. This allows the ICM7281 to drive over 2000pF at multiplex rate of 100Hz. Normally an LCD dot matrix display will have less

than 1000pF capacitance per 40 columns (each ICM7281 drives 40 columns).

#### POWER DISSIPATION

The power dissipation of a display system driven by the ICM7281 has several components:

- 1) Quiescent or DC power dissipation of the ICM7281
- 2) Dynamic or AC power dissipation of the ICM7281
- 3) Power consumed in driving the LCD display.

#### ICM7281 Power Dissipation

The quiescent current of the ICM7281 is very low, typically less than 1µA, and can generally be ignored. The dynamic current is proportional to the clock frequency, with a typical value of 1.0mA per MHz. This means that at a 500kHz clock the dynamic current will be 0.5mA.

#### LCD Display Drive Dissipation

Since the LCD has very low leakage currents, most of the power used to drive the LCD is used to charge and discharge the LCD capacitance. The power is

Where:

P<sub>LCD</sub> is the power dissipated in driving the display C is the display capacitance

V is Voltage across the display

fFFF is the effective multiplex frequency

The effective multiplex frequency ranges from  $f_{MUX}$  to N x  $f_{MUX}$ , where  $f_{MUX}$  is the multiplex rate and N is the number of rows. The actual effective multiplex frequency is dependent on which characters or bit pattern is being displayed and is typically about N/3 x  $f_{MUX}$ 

#### Low Power Shutdown

If the data clock is stopped and the voltages across the LCD are not changing, the power consumption will drop to the 5 to 50 microwatt range. Set  $V_{DISP}$ ,  $V_{2}$  and  $V_{3}$  equal to  $V_{DD}$  to prevent permanent damage to the LCD display by a DC bias.

#### **APPLICATIONS**

## Alphanumeric Display Using ICM7280 Intelligent Row Driver

The ICM7280 Intelligent Row Driver is specifically designed to drive multiple ICM7281 LCD Column Drivers. Figure 5 shows a typical 80 character display. The ICM7280 and ICM7281's will drive either 7, 8, 9 or 10 row displays, with the characters having either 5 or 6 columns. The Row Driver receives ASCII data, converts that data to bit-by-bit column data for the ICM7281's and serially shifts data into the ICM7281's. This process is repeated for each phase of the multiplex cycle.

Temperature compensation and generation of  $V_{DISP}$  for the ICM7280/81 system is shown in Figure 10. For further details refer to the ICM7280 Intelligent LCD Row Driver data sheet.

#### LCD Graphics Display

In this circuit, ICM7281's are used to drive both the rows and columns of the LCD dot matrix. An external controller is

used to generate the row and column data that is serially transferred into the ICM7281's. (See Figure 6).

The display drive voltages are generated in a resistor divider network. The optimum voltages for V1 through V5 can be calculated using the equations of Figure 9. Optimum voltages for common multiplex ratios are shown in Table 2.

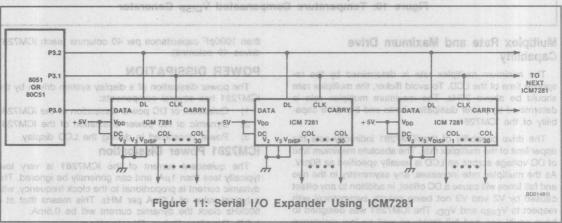
The LCD shown in Figure 6 is a 32 row display, divided into two sections of 16 rows to increase the ON/OFF RMS voltage ratio, thereby improving the contrast of the display. As LCD fluids improve it will become practical to use 32 or 64 row multiplexing, reducing the number of column drivers by a factor of 2 or 4.

As the number of rows increases, the V<sub>DISP</sub> required by the ICM7281's modified Alt and Pleshko multiplex scheme increases less than the V<sub>DISP</sub> required by a classic Alt and Pleshko multiplex scheme. For example: a 64 row display with a 1.45V threshold would require  $+5\mathrm{V}$  and  $-12.4\mathrm{V}$  supplies using standard Alt and Pleshko multiplexing. The ICM7281 would require only  $+5\mathrm{V}$  and  $-4.9\mathrm{V}$  to drive this same display with 64 row multiplexing. The negative voltage could easily be generated using a charge pump such as the ICL7660. (See Figure 10).

#### Serial Input I/O Expander

In addition to driving LCD's, the ICM7281 can be used as an I/O expander as shown in Figure 11. In this case, the data can be serially entered into the ICM7281 shift register using the 80C51 serial port. The 80C51 then transfers the data to the output latch by pulsing the DATA LATCH input with an I/O port line. Note that multiple ICM7281's can be cascaded to get more than 30 output lines. This cascading does not require any additional logic since the ICM7281 CARRY OUTPUTs are used.

DISPLAY CONTROL is tied to  $V_{DD}$  so that the data on the column outputs is the same as the data that was entered. If DISPLAY CONTROL is grounded, the column outputs will be inverted data. with  $V_3$  grounded, the logic level at the column outputs will be CMOS compatible, swinging from ground to  $V_{DD}$ . The output resistance of the column outputs is about 2k ohms.



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# LIMINARY

#### GENERAL DESCRIPTION

The ICM7283 is designed to provide a complete microprocessor interface for an 2 line by 40-character alphanumeric LCD display system. It includes a character generator, display voltage generator and resistor string, row drivers, and control circuitry. Interface to a host microprocessor is achieved through either a multiplexed or nonmultiplexed parallel bus.

Storage Temperature

The ICM7283 is designed to offload all display-related tasks from the host microprocessor and to provide an easyto-program software interface. Since the internal circuitry operates at full microprocessor speeds, there is no waiting for completion of internal operations. Testing of a "Busy" flag, when characters or commands are written, is not

Character data can be loaded with an auto-incremented cursor or in a random-access mode. Versatile control functions allow all or selected portions of the display to be underlined, blinked, blanked, or displayed in reverse video. Power-down features are provided, and both an underline and a blinking-box cursor are available.

The ICM7283 can display four user-defined characters in addition to the standard 96 ASCII upper and lower-case characters and 14 European and graphics characters.

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7283AIDM	-40°C to +85°C	48-Pin Side Braze Ceramic
ICM7283A/D	man year	DIE
ICM7283BIDM	-40°C to +85°C	48-Pin Side Braze Ceramic
ICM7283B/D		DIE

- Two Lines by 40 Characters Wide Display Memory
  - Directly Drives up to 6 ICM7281 Column Drivers
- High Speed µP Interface
  - ICM7283A: Intel, Zilog Compatible
  - ICM7283B: Motorola, Rockwell Compatible
- 120 Character Font With Multiple Attributes - Underline, Cursor, Blinking, Reverse
- 4 User Definable Characters
- Versatile Character Font Matrix
- -5 or 6 Columns By 8 Rows
- High Speed Internal Architecture
  - No Busy Flag Needed

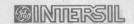
#### **APPLICATIONS**

- **Battery Hand-Held Terminals**
- **Portable Computers**
- Instrument Control Panels
- LCD Display Modules

CHITTHIODA .				
CONTROL LOCK			PH -	
			1 31	
	1 ROW 14	ROW 15	48	
	2 ROW 13	ROW 16	47	
	3 ROW 12	VDD	45	
	4 ROW 11	A <sub>6</sub>	45	
	5 ROW 10	As	44	
	6 ROW 9	NO CA4	43	
	7 ROWS	CM7283 A <sub>3</sub>	42	
	8 ROW 7	A <sub>2</sub>	41	
	9 ROW 6	Α,	40	
	10 ROW 5	Ao	39	
	11 ROW 4	CS	38	
	12 ROW 3		37	
Figure 2:	13 ROW 2		36	
	14 ROW 1		35	
	15 DOUT	Do	34	
	16 VOISP	D <sub>t</sub>	33	DIFFCTRIC
	17 V3	D2	32	AC CHARL
	18 V2	n.c.	-	
ADIRL = ADD	19 DCONT	N.C.	-	
	20 SCLK	03	29	
aT .	21 DLAT	THAR D4	28	TOBRIAGO
Address/Dat	22 VINV	Ds	27	Pre-cate
	23 OSC	D6	26 JUGA	
	24 VSS	07	25	
Osc open of		Inoxio	Buppiy	
VII = 0V, VII		The same of the sa	34911	Toward .
11. 11. 11. 11.	PART	PIN PIN	PIN	YSTAL

			CD034	Will the Sales		
The second second	PART #	PIN 33	PIN 34	PIN 35		
1	7283A	RD	WR	ALE		
1	7283B	F	R/W	AS		

Figure 1: Pin Configuration

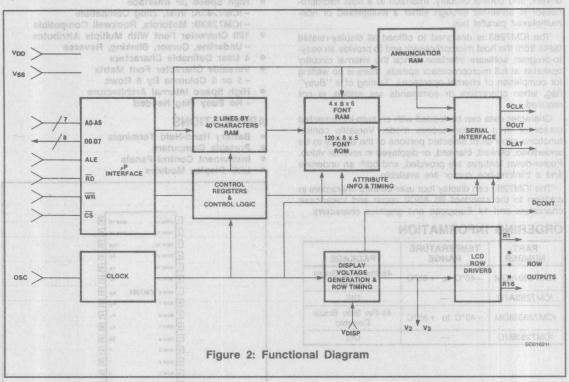


#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (VDD - VSS)	+6.5V
Display Voltage (VDD - VDISP)	
Input VoltageVSS-0.5V to VDD	
Power Dissipation500mW @	70°C

Operating Temperature Range	40°C to +85°C
Storage Temperature Range.	
Lead Temperature (Soldering,	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



#### ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS

 $(V_{DD} = 5.0V \pm 10\%, T_A = -40 \text{ to } +85^{\circ}\text{C}, V_{DISP} = V_{DD} -8V, V_{SS} = 0V, \text{ unless otherwise specified.})$ 

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
l <sub>IL</sub>	Input Leakage	Address/Data pins high impedance 0 < V <sub>IN</sub> < V <sub>DD</sub>	-10		+10	μΑ
IDD	Supply Current	Osc open ckt, V <sub>IL</sub> = 0V, V <sub>IH</sub> = V <sub>DD</sub>			2.5	mA
ISTBY	Shutdown Current	V <sub>IL</sub> = 0V, V <sub>IH</sub> = V <sub>DD</sub>			100	μΑ
VSUPP	Operating Voltage Range	V <sub>IL</sub> = 0.4V, V <sub>IH</sub> = 2.4V	4.5		5.5	٧
fosc	Osc. Frequency	Pin 23 open ckt.	0.2		1.0	MHz
Serial Outp	outs					
VoL	Output Voltage, Low	I <sub>OL</sub> = 1mA		130112	1.0	V

# ELECTRICAL CHARACTERISTICS (CONT.) (margaid primit see) 2017219310494000A

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voн	Output Voltage, High	I <sub>OH</sub> = 1mA	V <sub>DD</sub> - 1.0	BC 13 G	2012/11	V
Data I/O,	μP Interface Inputs	20004 =T	p1	eči bileV	AS 3	ON I
VOL	Output Voltage, Low	I <sub>OL</sub> = 1.6mA	smit bi	orl atsC	0.4	V
Vон	Output Voltage, High	Ι <sub>ΟΗ</sub> = 400μΑ	2.4	use SA	E to	V
VIL	Input Voltage, Low				0.8	V
VIH	Input Voltage, High		3.0	OH MA	20.0	V
Row Drive	r Outputs	The Land				
Ron	Output Resistance, ON	D <sub>CONT</sub> high, $V_0 = V_{DISP} + 0.5V$ D <sub>CONT</sub> low, $V_0 = -0.5V$	COCCECCO	6666	1	kΩ
ROFF	Output Resistance, OFF	DCONT high, $V_0 = V_4 \pm .5V$ DCONT low, $V_0 = V_1 \pm 0.5V$			2.5	kΩ
V <sub>1</sub>	parameter - 144 15	DCONT high	-	-1.0		V
V <sub>2</sub> , V <sub>3</sub>	Newstand transcent	Tay offi	- Neuron	1.0	manus.	V
V <sub>4</sub>		DCONT low		3.0		V

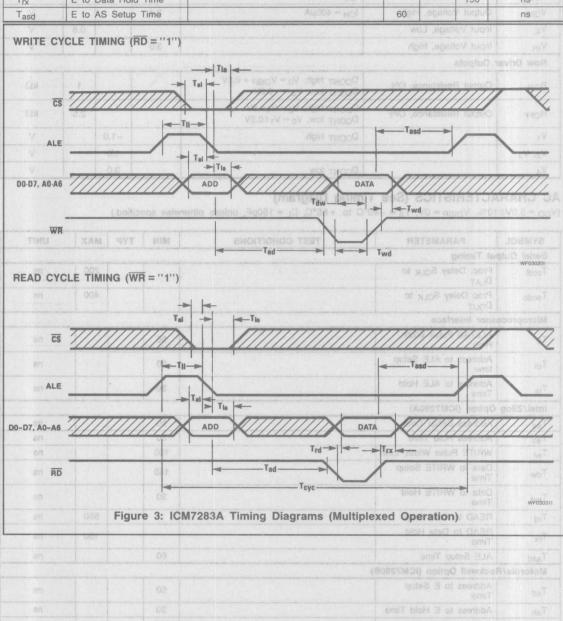
#### AC CHARACTERISTICS (See Timing Diagram)

 $(V_{DD} = 5.0V \pm 10\%, V_{DISP} = 0V, T_A = -40$ °C to +85°C,  $C_L = 150$ pF, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Serial Out	put Timing	12-21 12-31-31-31-31-31-31-31-31-31-31-31-31-31-	1				
T <sub>scdl</sub>	Prop. Delay S <sub>CLK</sub> to D <sub>LAT</sub>			("1" =	W) as	200	LIOYO NS
T <sub>scdo</sub>	Prop Delay S <sub>CLK</sub> to D <sub>OUT</sub>		-m   let-			400	ns
Microproc	essor Interface	gH ->	db-	1			
TII	ALE/AS Pulse Width, High		LK	55	27		25 ns
Tol	Address to ALE Setup time		19-1	30			ns
T <sub>la</sub>	Address to ALE Hold Time	tion to the monthly the control probation through the	Z.	30	gara programa		3.14 ns
Intel/Zilog	Option (ICM7280A)	——— a)	1 (45)				
Tad	Address Setup Time	TAG TO THE TOTAL OF THE TAGE	aan Di	50	1000	1777	ns
Tah	Address Hold Time	consumat "Bellevilein in the technique of the		30		decimalisation	ns
T <sub>wl</sub>	WRITE Pulse Width, Low	- THE TONE OF STREET		100			ns
T <sub>dw</sub>	Data to WRITE Setup Time	Van 191	4	150			TA ns
T <sub>wd</sub>	Data to WRITE Hold Time			30			ns
T <sub>rd</sub>	READ to Valid Data	Timing Disgrams (Multiple	MY283A	31 10	Figure	550	ns
T <sub>rx</sub>	READ to Data Hold Time					150	ns
Tasd	ALE Setup Time			60			ns
Motorola/I	Rockwell Option (ICM7280B)						
Tad	Address to E Setup Time			50			ns
Tah	Address to E Hold Time		357	30			ns
Tee	E Pulse Width, High			200			ns

### AC CHARACTERISTICS (See Timing Diagram) (CONT.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>dw</sub>	Data to E Setup Time	A section of the second section of the second section of the secti	150	Anothe	/ horizon	ns
Twd	Data to E Hold Time		30	VOID APPRO	10000	ns
T <sub>rd</sub>	E to Valid Data	T <sub>ee</sub> = 400ns	63	adur ao	550	ns
T <sub>rx</sub>	E to Data Hold Time	Am6.1 = 301	WO.	ollsge,	150	ns
Tasd	E to AS Setup Time	With = HOI	60	oftage,	/ hughuQ	ns



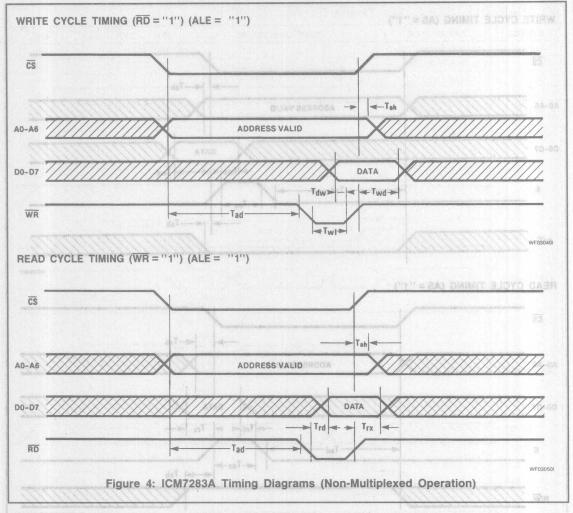
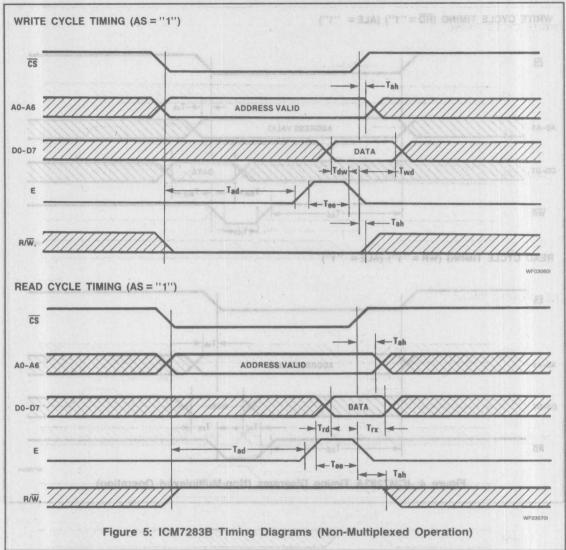
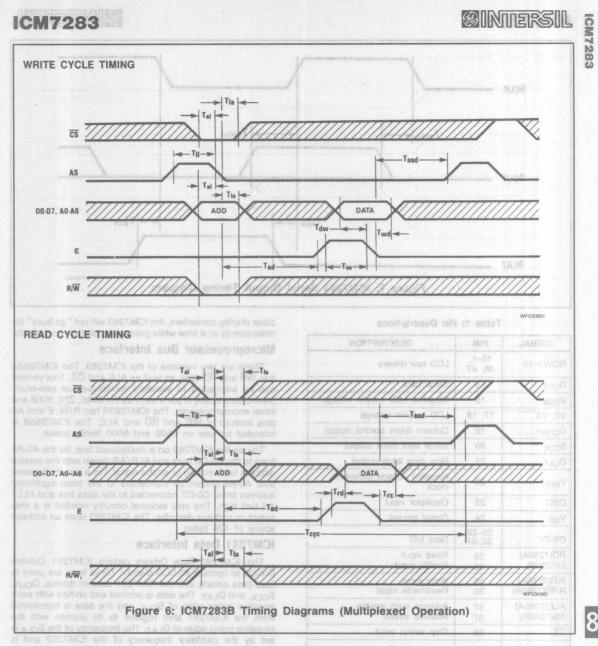


Figure 5: ICM7283B Timing Diagrams (Mon-Multiplexed Operation)





The ICM7283 oscillator will tree run at 600kHz in dia and the value of Cexternal Table 1 shows the relationship

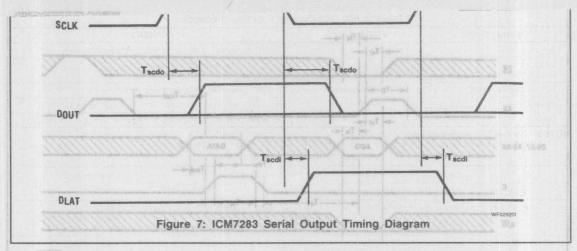


Table 1: Pin Descriptions

SIGNAL	PIN	DESCRIPTION
ROW1-16	10–1, 48, 47	LCD row drivers
Dout	15	Serial data
V <sub>DISP</sub>	16	Negative LCD supply voltage
V2, V3	17, 18	LCD column voltage
DCONT	19	Column driver control output
SCLK	20	Serial data clock output
DLAT	21	Row data latch output
VINV	22	Negative voltage generator clock
osc	23	Oscillator input
Vss	24	Digital ground
D0-D7	25-29 32-34	Data I/O
RD(7280A) E(7280B)	35 35	Read input Enable input
WR(7280A) R/W(7280B)	36 36	Write input Read/write input
ALE(7280A) AS(7280B)	37 37	Address latch enable Address strobe
CS	38	Chip select input
A0-A6	39-45	Address inputs
V <sub>DD</sub>	46	Positive digital and LCD supply voltage

# DETAILED DESCRIPTION Hardware Interface

Figure 1 is a simplified block diagram of the ICM7283. It is a dedicated hardware IC and the speed of data entry and command processing is limited only by gate delays. Unlike

other display controllers, the ICM7283 will not "go busy" for milliseconds at a time while processing data or commands.

#### Microprocessor Bus Interface

There are two versions of the ICM7283. The ICM7283A has  $\overline{WR}$  and  $\overline{RD}$  pins, as well as ALE and  $\overline{CS}$ . This version can be interfaced to standard multiplexed or non-multiplexed data buses of parts such as the 8085, Z80, 8088 and other microprocessors. The ICM7283B has R/ $\overline{W}$ , E and AS pins instead of  $\overline{WR}$  and  $\overline{RD}$  and ALE. The ICM7283B is intended for use on 6800 and 6500 family buses.

To use the ICM7283 on a multiplexed bus, tie the A0-A6 lines to the D0-D6 lines and ALE/AS driven with the system address latch enable or strobe signal. For a non-multiplexed bus, A0-A6 should be connected to the least significant address lines, D0-D7 connected to the data bus and ALE/AS tied high. The only external circuitry needed is a chip select or address decoder. The ICM7283 uses an address space of 128 bytes.

#### ICM7281 Data Interface

The ICM7283 Row Drivers require ICM7281 Column Drivers to operate an LCD display. Three lines are used to load data serially into the ICM7281 column drivers,  $D_{OUT}$ ,  $S_{CLK}$ , and  $D_{LAT}$ . The data is latched and shifted with each negative going edge of  $S_{CLK}$ , and the data is transferred from the ICM7281 shift register to its latches with the negative going edge of  $D_{LAT}$ . The frequency of the  $S_{CLK}$  is set by the oscillator frequency of the ICM7283 and is normally about 600kHz.

#### Oscillator

The ICM7283 oscillator will free run at 600kHz in die form, when not loaded with any capacitance. With 15pF of external capacitance, the frequency will be about 250kHz. Figure 8 shows the relationship between oscillator period and the value of Cexternal. Table 1 shows the relationship between the oscillator frequency and various display system signals and features. Standard CMOS logic gates can be used to overdrive the oscillator to control frequency. A

suitable frequency can also be derived by dividing down the host processor's clock.

Table 2: ICM7283 Display System Frequencies

SIGNAL NAME		FREQUENCY	COMMENTS
S <sub>CLK</sub>	cust	OSC	Sets data transfer rate to ICM7281 column drivers
D <sub>LAT</sub> Display Control	TRIBUTET	OSC/M OSC/M	Once per row multiples period.
LCD Multiplex Freq.	January 1	OSC/(NxMx2)	Should be above 30Hz to avoid flicker.
Blink Rate	TRACES	OSC/(NxMx64)	Blink rate for blinking cursor and blinking characters
VINV		OSC	AC waveform for generating a negative voltage for VDISP

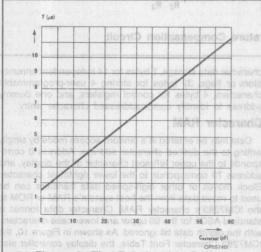
**NOTES:** Where N = number of rows - i.e. 16.

M = 40 x number of columns (5 or 6) per character. Add 14 if annunciators enabled.

Table 3: ICM7283 Memory Map

A	DDRESS	
DECIMAL	HEX	FUNCTION SERVICE SERVI
0-79	00H-4FH	Character RAM. Loaded with ASCII data characters to be displayed. Address 0 is the upper leftmost character and Address 40 (28H) is the lower leftmost character.
80-119	50H-77H	Font RAM. Holds bit pattern for four user-definable characters. Set Table 4.
120	78H	Instruction register 0 (IR0)
121	V2.5- = 79H	Instruction register 1 (IR1)
122	7AH Sa	Instruction register 2 (IR2)
123	7BH 78	Cursor Register (IR3)
124	7CH	Unassigned
125	7DH	Annunciator Register 1 (AR1)
126	7EH	Annunciator Register 2 (AR2)
127	7FH	Cursor-Addressed Entry Register

NOTE: See Table 6 for more detail about addresses 120-127 (78H-7FH).



# Figure 8: The Relationship Between Oscillator Period and Cexternal

#### Display Interface

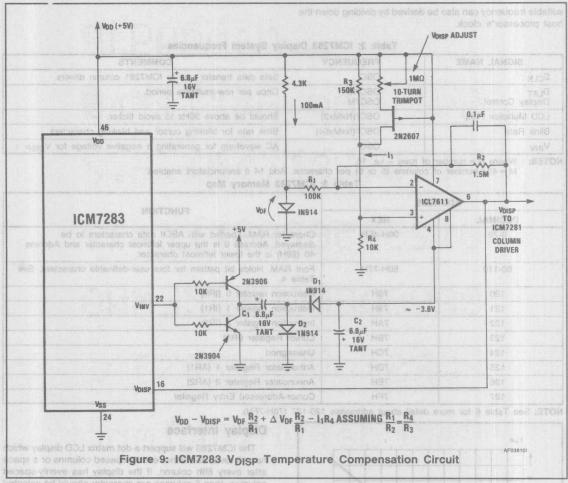
The ICM7283 will support a dot matrix LCD display which has 16 rows, and either evenly-spaced columns or a space after every fifth column. If the display has evenly-spaced columns, then 6 columns per character should be selected and the sixth column is always blank. If the display provides a blank after every fifth column, then 5 columns per character should be selected. The character font is automatically changed to take advantage of all rows. The ICM7283 will automatically use one of the 6 evenly-spaced columns for a space.

The ICM7283 can drive LCD displays with threshold voltages up to 2.5 volts. There is no minimum display threshold voltage since V<sub>DISP</sub> can be above V<sub>SS</sub>.

The ICM7283 also has 16 onboard row drivers designed to handle large dot matrix displays. These drivers provide fast slew rates, and have a minimum offset voltage.

LCO floids have a pronounced negative tempora-

8



#### Display Voltage Generator

The ICM7283 not only has an onboard resistor string to generate the required V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>, and V<sub>4</sub>, but also has an output that assists in generating a negative voltage for V<sub>DISP</sub>. The V<sub>INV</sub> pin is a low-impedance output that swings from V<sub>DD</sub> to V<sub>SS</sub> at the oscillator frequency. The circuit of Figure 9 connected to the V<sub>INV</sub> pin generates a temperature-compensated V<sub>DISP</sub>. Diodes D<sub>1</sub> and D<sub>2</sub>, with capacitors C<sub>1</sub> and C<sub>2</sub> form a charge-pump negative voltage generator. The ICL7611 CMOS op-amp and its associated circuitry form an adjustable temperature compensated voltage source that provides V<sub>DISP</sub> to the ICM7283, as well as the ICM7281 column drivers. Temperature compensation for V<sub>DISP</sub> is necessary because the threshold voltage of LCD fluids have a pronounced negative tempco.

#### SOFTWARE INTERFACE

Table 3 provides a memory map of the ICM7283. The ICM7283 uses 128 bytes of memory space: 80 bytes for

character data storage, 2 bytes for 14 independent annunciators or flags, 32 bytes for storing 4 user-programmable characters, 4 bytes for control registers, and one dummy address to identify cursor-addressed character entry.

#### Character RAM

Data may be entered in a random-access mode by simply writing to the desired character address. Address 0 corresponds to the upper leftmost character of the display, and address 79 corresponds to the lower rightmost character. Block moves or other high-speed data transfers can be used to move data from the host system's RAM or ROM to the ICM7283's character RAM. Character data format is standard ASCII for the 96 upper and lower case characters, with the eighth data bit ignored. As shown in Figure 10, the ICM7283 Character Font Table, the display controller also recognizes three special control characters and 14 additional European and graphics characters. The characters 08 through 17 are alternate lower case characters.



Attributes are enabled by bit 5 of that from the first state of the st

instruction bit to be shifted out, and will appear on column information cutputs; if enabled the of the ICMZ81. The annunciator outputs; if enabled appear on all rows in columns 1-14. Annunciators are unabled inv bit 7 at IR1.

the character RAM. These attribute characters are displayed as bianks, but signal the ICM7283 that the character to the right of the attribute character are to be displayed with one of the three attributes ( $5 = u_0 de_1 tine$ , 6 = reverse video, and 7 = b linking). Each attribute is cancelled by a



Table 4: Font RAM for User-Definable Characters

ROW	ASCII CHARACTER 0 FONT ADDRESS		ASCII CHARACTER 1 FONT ADDRESS		ASCII CHARACTER 2 FONT ADDRESS		ASCII CHARACTER 3 FONT ADDRESS	
	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex
Row 1 (top row)	80	50H	90	5AH	100	64H	110	6EH
- 664 66	10 SH-0 11	-		图 医土土 新工		FLLE Seen	Diet-	-
	THE REAL PROPERTY.	# 15 AT AT		tr dt dr ts	5 M 70 M	Se To be	- 6	-
	-	-	I	-	-	-	-	
	-	-		_	-	-	-	-
- FR 180 100 100 110 110 110 110 110 110 110	The coals as	CONTRACTOR	S ONCE ITEM	C CONFO DES		CHECK COST	000	-
- 5011111111					5.在10g-10g-10g-10g-10g-10g-10g-10g-10g-10g-		BE-	104
Row 8 (bottom row)	87	57H	97	61H	107	68H	117	75H

#### Font RAM

In addition to the 120 characters available in the built-in character ROM, 4 characters may be user-defined. Table 4 shows the mapping between the Font RAM and the user-defined character font. An example of an additional character is provided in Figure 11. Note that addresses 80-119 (50H-77H) hold 5 bit words that correspond to the bit pattern of the four user-definable characters, such that each 5 bit word defines the pattern for one row of the character. The LSB corresponds to the right-hand dot. Each character uses 8 words, with the lowest address representing the top row. Once defined, these characters are treated the same as the predefined characters from the Font ROM. Enter ASCII data 0, 1, 2, or 3 into Character RAM to call up one of those characters.

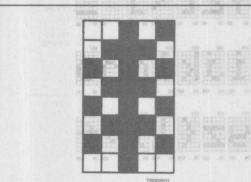


Figure 11: An Example of a User-Defined Character

#### Instruction and Annunciator Registers

Table 5 details the bit assignments of the control registers. All registers are write-only registers.

Attributes are enabled by bit 5 of Instruction Register IR2, at address 122 (7AH). Blinking, underlined, and reverse video characters are controlled by attribute characters in the character RAM. These attribute characters are displayed as blanks, but signal the ICM7283 that the characters to the right of the attribute character are to be displayed with one of the three attributes (5 = underline, 6 = reverse video, and 7 = blinking). Each attribute is cancelled by a

second occurence of the attribute character. The entire display can be blinked or blanked by setting the appropriate bits in IRO.

Table 5: ASCII Character 0 Example

M 10	Font Ac	Font Address		ta	
Row	Decimal	Hex	Decimal	Hex	
1	80	50H	5	05H	
2	81	51H	14	0EH	
3	82	52H	21	15H	
or 4 m	83	53H	14	0EH	
5	84	54H	21	15H	
6	85	55H	14	0EH	
7	86	56H	21	15H	
8	87	57H	4	04H	

The Cursor Register determines the location of the cursor on the display. If data is written to address 127 (7FH), the data is entered at the current location of the cursor and the cursor position is incremented. The cursor position may be directly set by writing to Cursor Register address 123 (7BH). The cursor may also be incremented or decremented by writing the appropriate instructions to IR2 at address 122 (7AH). The cursor location will wrap around from 79 to 0 or vice versa when incremented or decremented. A number greater than 79 written to the Cursor Register causes no cursor to be displayed, but the ICM7283 will otherwise function normally. If bit 4 of IR1 at address 121 (79H) is at "1", then all characters to the right of the cursor are blanked but the data in the character RAM is retained.

The IRO register is a bit set/reset register. The MSB selects either set (1) or reset (0) operation. A "1" in any other bit position selects that bit to be set/reset. For example, a bit pattern of 10011001 will set bits 0, 3 and 4, while a bit pattern of 00010000 will clear bit 4. Unselected bits are not affected.

The Annunciator Registers are bit set/reset registers that operate similarly to IR0. When used with the ICM7281 column drivers, bit 0 of Annunciator Register 1 will be the last bit shifted out, and will appear at the column 1 output of the ICM7281. Bit 6 of Annunciator Register 2 is the first annunciator bit to be shifted out, and will appear on column 14 of the ICM7281. The annunciator outputs, if enabled, appear on all rows in columns 1-14. Annunciators are enabled by bit 7 at IR1.

registers, annunciator registers, and the Cursor Hegister. Bit 6 of Instruction Register 2 also resets and stops the display multiplex and blink counters.

All register bits except bit 6 of IR2 are reset upon powerup. Since bit 6 of IR2 is indeterminate at power-up, and the instruction registers cannot be written to while bit 6 is set, the initialization routine should first clear bit 6 before the other registers of the ICM7283 display controller, are accessed. When normal operation resumes after bit 6 of IR2 is cleared, the attributes will be off and the cursor will be present at 0.

CAUTION: The ICM7283 should not be left in the reset mode for extended periods, because in this condition there is a DC bias on the liquid crystal display which can permanently damage it.

#### DISPLAY SYSTEM

Figure 10 shows a complete 2 line by 40 character Intel/ Zilog compatible display system without annunciators. The ICM7283A receives ASCII character data from the host microprocessor, converts it to a serial data stream for the ICM7281 column drivers, and provides the row drive voltages and overall display system timing and control. The power consumption of this display system is typically 6 milliwatts during normal operation and 5 microwatts when shutdown (but retaining data and control setup).

If less than 80 characters are desired, the ICM7281's that would normally drive the right-hand characters of the display may be left out. This means that an 80 character display module and a module with fewer characters can have exactly the same hardware and software interface, except that extra ICM7281's are missing from the module with fewer characters.

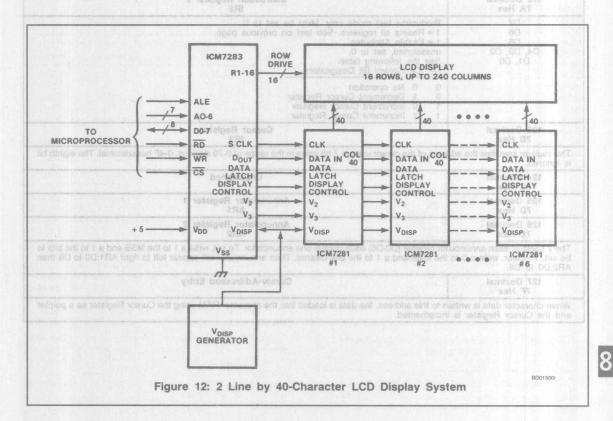




Table 6: Instruction and Annunciator Registers

120 Decimal 78 Hex		tion Register 0 IRO
D7 D6 1950 1950 1950 1950 1950 1950 1950 1950	1 = Blink Display 1 = Cursor Enabled 1 = Power Down Mode unassigned, set to 0. unassigned, set to 0. 0 = Normal Operation, 1 = Test Mode	All register bits except bit 6 of IR2 are reset upon a since bit 6 of IR2 are reset upon a since bit 6 of IR2 is indeterminate at power-up arruction registers cannot be written to written to written to written to written to written to be infectation rousine should triss clear bits bit her registers of the ICM7283 display control control conceptor resumes after
121 Decimal 79 Hex	and ormans of name see to	tion Register 1, and line setud atts and beneate at SI
D7 D6 D6 D6 D6 D6 D6 D6 D6 D6 D6 D6 D6 D6	1 = Blank characters to the right of the cu	sor les et on blands Cast Mot and HOTTLAS ursor sper character ciators turned on, 0 = Normal Operation
122 Decimal 7A Hex	Instruc	tion Register 2 IR2
D7 D6 D5 D4, D3, D2 D1, D0	0 0 No operation 0 1 Decrement Cursor Register 1 0 Increment Cursor Register	ous page.
123 Decimal 7B Hex	1 1 Increment Cursor Register	sor Register
	ress of the cursor using a 7 bit value in the ran	ge of 0-79 decimal, 0-4F hexadecimal. The eighth bit
124 Decimal 7C Hex	MOTAL DISPLAY	nassigned
125 Decimal 7D Hex	gV gV Annunc	iator Register 1 AR1
126 Decimal 7E Hex	aged Annunc	lator Register 2 AR2
		tor. To set, write a 1 to the MSB and a 1 to the bits to nunciator will appear left to right AR1:D0 to D6 then
127 Decimal	Cursor-/	Addressed Entry

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# Section 9 — Microcontrollers, Microperipherals, Memory

Section 9 — Microcontrollers,
Microperipherals, Memory

# Per Compatible Real-Time Clock RELIMINATION OF THE CHARGE



The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Intersil's silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from 1/100 seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (tacc) of 300ns eliminates the need for any microprocessor wait states or software overhead. Furthermore, the ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts. The first type is the periodic interrupt (i.e., 100Hz, 10Hz, etc.) which can be programmed by the internal interrupt control register to provide 7 different output signals. The second type is the alarm interrupt. The alarm time is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power-Down Detector eliminates the need for external components to support the battery back-up function. When a power-down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Input/output and read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

#### **FEATURES**

- 8-Bit µP Bus Compatible - Multiplexed or Direct Addressing
- Binary Time Data Format Lowers Software Overhead
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll-Over During
- Full Calendar With Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less Than 300ns
- 4 Programmable Crystal Oscillator Frequencies
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: 2µA Typ. at 3.0V and 32kHz Crystal

#### **APPLICATIONS**

- Portable and Personal Computers
- **Industrial Control Systems**
- Data Logging
- Point Of Sale

#### ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE					
ICM7170IPG	-40°C to +85°C	24-PIN PLASTIC DIP					
ICM7170IJG	-40°C to +85°C	24-PIN CERDIP					

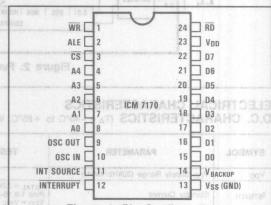


Figure 1: Pin Configuration



#### ABSOLUTE MAXIMUM RATINGS

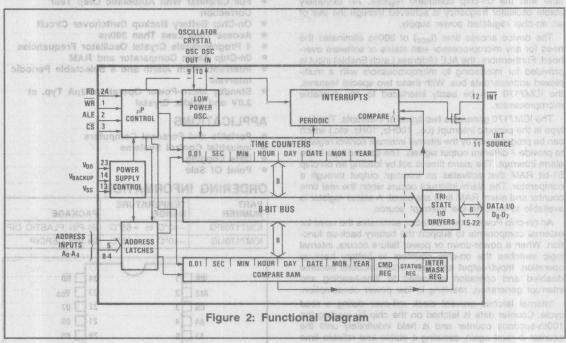
Supply Voltage	8V
Power Dissipation (Note 1)	500mW
Input Voltage (Any Terminal)	
(Note 2)VDD + 0.3V to	Vss -0.3V

Operating Temperature	40°C to +85°C
Storage Temperature	65°C to +150°C
Lead Temperature (Soldering,	10sec)300°C

NOTE 1: TA = 25°C.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V<sub>DD</sub> or less than V<sub>SS</sub> may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

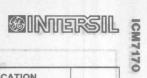


# **ELECTRICAL CHARACTERISTICS**

D.C. CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = +5V ±10%, V<sub>BACKUP</sub> = V<sub>DD</sub>,V<sub>SS</sub> = 0V unless otherwise specified)

OVINDOL	ro 🗆 al e 🗆 rue na		SP	LIMIT			
SYMBOL	PARAMETER OF DEC DES	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>DD</sub> quaga	V <sub>DD</sub> Supply Range (32kHz/4MHz)	(3)	2.6		5.5	V	
ISTBY(1)	Standby Current	F <sub>XTAL</sub> = 32kHz Pins 1-8,15-22 & 24 = V <sub>DD</sub> V <sub>DD</sub> = V <sub>SS</sub> ; V <sub>BACKUP</sub> = V <sub>DD</sub> - 3.0V		2.0	20	μΑ	
ISTBY(2)	Standby Current	FXTAL = 4MHz Pins 1-8,15-22 & 24 = VDD VDD = VSS; VBACKUP = VDD - 3.0V		20	150	μА	
I <sub>DD(1)</sub>	Operating Supply Current	F <sub>XTAL</sub> = 32kHz Read/Write Operation at 100Hz		0.3	1.2	mA	
I <sub>DD(2)</sub>	Operating Supply Current	F <sub>XTAL</sub> = 32kHz Read/Write Operation at 1MHz		1.0	2.0	mA	
VIL	Input low voltage	V <sub>DD</sub> = 4.5V			0.8	V	
VIH	Input high voltage	V <sub>DD</sub> = 4.5V	3.5			V	
VOL	Output low voltage except INTERRUPT	I <sub>OL</sub> = 1.6mA			0.4	V	

## ICM7170



## **ELECTRICAL CHARACTERISTICS (CONT.)**

evana.		T-07 001	DITIONS	SP			
SYMBOL	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
Vон	Output high voltage except INTERRUPT	I <sub>OH</sub> = 400μA	ili no escripcio de la caración de	2.4	market make		V
IIL	Input leakage current	VIN = VDD or VSS		-10	0.5	+10	μΑ
loL	Tristate leakage current (D <sub>0</sub> -D <sub>7</sub> )	V <sub>0</sub> = V <sub>DD</sub> or V <sub>SS</sub>		-10	0.5	+10	μΑ
VBATTERY	Backup Battery Voltage	F <sub>XTAL</sub> = 1, 2, 4MHz		2.6		3.2	V
VBATTERY	Backup Battery Voltage	F <sub>XTAL</sub> = 32kHz			2.0	3.2	V
VOL	Output low voltage INTERRUPT	I <sub>OL</sub> = 1.6mA	INT SOURCE	Des Fred	10000	0.4	V
loL	Leakage current INTERRUPT	V <sub>0</sub> = V <sub>DD</sub> or V <sub>SS</sub>	to Vss		10		μΑ

AC CHARACTERISTICS (TA = -40°C to +85°C, VDD = +5V ±10% D0-D7 VBACKUP = VDD Load Capacitance = 150pF, V<sub>IL</sub> = 0.4V, V<sub>IH</sub> = 3.5V unless otherwise specified)

SYMBOL	( P = 02 PARAMETER CENTRUM NO	M FICHINGE	TYP	MAX	UNIT
READ CYC	LE TIMING				
t <sub>rd</sub>	READ to DATA valid		170	250	ns
tacc	ADDRESS valid to DATA valid	E REMIDEA	200	300	ns
tcyc	READ cycle time	400			ns
t <sub>rx</sub>	RD high to bus tristate		85	100	ns
tas	ADDRESS to READ set up time*		100		ns
tar	ADDRESS HOLD time after READ*	0			ns
trl	READ pulse width, low*	0.25		9,000*	μs
	*Guaranteed Parameter by Design	(Not 100% Te	sted)		
WRITE CY	CLE TIMING	MIN	TYP	MAX	UNIT
tad	ADDRESS valid to WRITE strobe	100			ns
twa	ADDRESS hold time for WRITE	0	-to-		ns
twi	WRITE pulse width, low	100	7		ns
tdw	DATA IN to WRITE set up time	100	A		ns
t <sub>wd</sub>	DATA IN hold time after WRITE	30	10		ns
t <sub>cyc</sub>	WRITE cycle time	400	P. Leve strate P.		ns
MULTIPLE	KED MODE TIMING	MIN	TYP	MAX	UNIT
t <sub>  </sub>	ALE Pulse Width, High	50			ns
tal	ADDRESS to ALE set up time	30			ns
tla	ADDRESS hold time after ALE	30			ns

NULTIPLEXED MODE TIMING

Figure 3: Timing Diagrams — Nonmultiplexed Bus

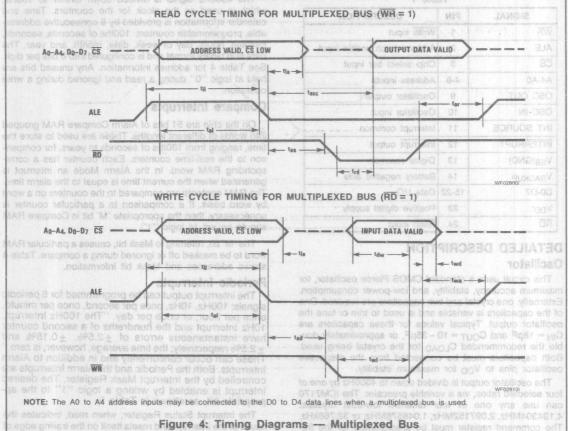


Table 2: Command Register Foresat

	Y.JMO-STI	HW (arr , are	00F) 883FG0	REGISTER AS	COMMAND		
00				P.G			10
Freq						8\n	

TEST BIT	90	INTERRUPT	MO			24/12 HOUR FORMAT	gg	CRYSTAL	00	10
Normal		Interrupt disabled		Step	0		0	32.768kHz	0	
		Interrupt enable				24 hour mode				
									0 -	
								ALT9439414Hz		

CM7170

Table 1

SIGNAL	PIN	DESCRIPTION
WR	1	Write input
ALE	2	Address latch enable input
CS	3	Chip select bar input
A4-A0	4-8	Address inputs
OSC OUT	9	Oscillator output
OSC IN	10	Oscillator input
INT SOURCE	11	Interrupt common
INTERRUPT	12	Interrupt output
V <sub>SS</sub> (GND)	13	Digital common
VBACKUP	14	Battery negative side
D0-D7	15-22	Data I/O
V <sub>DD</sub>	23	Positive digital supply
RD	24	Read input

#### DETAILED DESCRIPTION Oscillator

This circuit uses a standard CMOS Pierce oscillator, for maximum accuracy, stability, and low-power consumption. Externally, one crystal and two capacitors are required. One of the capacitors is variable and is used to trim or tune the oscillator output. Typical values for these capacitors are CIN = 18pF and COUT = 10 - 35pF, or approximately double the recommended CLOAD for the crystal being used. Both capacitors must be connected from the respective oscillator pins to VDD for maximum stability.

The oscillator output is divided down to 4000Hz by one of four selected ratios, via a variable prescaler. The ICM7170 can use any one of four different low-cost crystals: 4.194304MHz, 2.097152MHz, 1.048576MHz, or 32.768kHz. The command register must be programmed for the frequency of the crystal chosen, and this in turn will determine the prescaler's divide ratio.

Command Register frequency selection is written to the D0 and D1 bits at address 11H and the 12 or 24 hour format is determined by bit D2, as shown in Table 4.

The 4000Hz signal is divided down further to 100Hz, which is used as the clock for the counters. Time and calendar information is provided by 8 consecutive addressable, programmable counters: 100ths of seconds, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format and is configured into 8 bits per digit. See Table 4 for address information. Any unused bits are held at logic "0" during a read and ignored during a write operation.

#### Compare Interrupts

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 100ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate 'M' bit in Compare RAM should be set to logic "1".

The 'M' bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 4 shows addresses and Mask bit information.

#### Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100Hz, 10Hz, once per second, once per minute, once per hour, or once per day. "The 100Hz Interrupt, 10Hz Interrupt and the hundreths of a second counter have instantaneous errors of ±2.5%, ±0.15% and ±2.5% respectively; the time average, however, is zero." These can occur concurrently and in addition to Alarm Interrupts. Both the Periodic and the Alarm Interrupts are controlled by the Interrupt Mask Register. The desired interrupt is enabled by writing a logic "1" to the appropriate bit, as shown in Table 5.

The Interrupt Status Register, when read, indicates the cause of the interrupt and resets itself on the trailing edge of the read pulse. Once one or more bits have been set in the Mask Register, a roll-over in a corresponding counter will strobe the appropriate bit in the Interrupt Status Register. The interrupt pin (#12) is then pulled to the potential of the interrupt source pin (#11) through an internal open-drain Nchannel MOSFET. This facilitates wire-ORing the ICM7170 with other interrupt generators that must be connected to the system MPU.

Table 2: Command Register Format

		COMMAND	REGISTER A	DDRESS (100	01b, 11h) WR	ITE-ONLY	
07	D6	D5	D4	D3	D2	D1	D0
a	n/a	Test	Int.	Run	12/24	Freq	Freq

**Table 3: Command Register Bit Assignments** 

D1	D0	CRYSTAL FREQUENCY	D2	24/12 HOUR FORMAT	D3	RUN/STOP	D4	INTERRUPT ENABLE	D5	TEST BIT
0	0	32.768kHz	0	12 hour mode	0	Stop	0	Interrupt disabled	0	Normal Mode
0	1	1.048576MHz	1	24 hour mode	1	Run	1	Interrupt enable	1	Test Mode
1	0	2.097152MHz	594				Tara da			
1	1	4.194304MHz								

Table 4: Address Codes and Functions

		ADD	RESS			A FINATION				DA	TA				WALLE
A4	A3	A2	A1	AO	HEX	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0	VALUE
0	0	0	0	0	00	Counter-1/100 seconds	-		-						0-99
0	0	0	0	1	01	Counter-hours	1000	-	10 -00						0-23
1.600		100	1. 331	Market .	THE SAME	12 Hour Mode		-	-	-				.51	1-12
0	0	0	141	0	02	Counter-minutes	110	-					10		0-59
0	0	0	1	1	03	Counter-seconds	-	-						1.00	0-59
0	0	1	0	0	04	Counter-month	En -	-	-	-				ann 1 1 1	1-12
0	0	1	0	1	05	Counter-date	NA -	-	-						1-31
0	0	1	1	0	06	Counter-year	-	01.14							0-99
0	0	1	1	1	07	Counter-day of week	14	-		-				B	0-6
0	1	0	0	0	08	RAM-1/100 seconds	M								0-99
0	1	0	0	1	09	RAM-hours	M =	M		1	-	-			0-23
A.		1 B B	1.		Low I	12 hour Mode	. *	M		-					1-12
0	1	0	1	0	OA	RAM-minutes	M	-							0-59
0	1	0	1	1	OB	RAM-seconds	M							2.	0-59
0	1	1	0	0	OC.	RAM-month	M	-	-	1-11	199	100			1-12
0	1	1	0	1	OD	RAM-date	M		-						1-31
0	1	1	1	0	0E	RAM-year	M			AFSYRU	15.31				0-99
0	1	1	1	1	OF	RAM-day of week	M	-	-	-	11-1	. %			0-6
1	0	0	0	10	10	Interrupt Status and Mask Register	rantins	181-	9:3 TT	-		10001 06-01	R.		
1 9	0	0	0	1	11	Command register	146213	mi-				onta-	been wed		

NOTES:

Address 10010 to 11111 (12h to 1Fh) are unused.

+' Unused bit for Interrupt Mask Register, MSB bit for Interrupt Status Register.

'-' Indicates unused bits.

\*\* AM/PM indicator bit in 12 hour format. Logic "0" indicates AM, logic "1" indicates PM.
'M' Alarm compare for particular counter will be enabled if bit is set to logic "0".

Table 5: Interrupt and Status Registers Format

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							morel 1 level cod
D7	D6	D5	D4	D3	D2	D1	D0
n/a	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm

HORE OF INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY TO TOTAL OF							when WR is a logic "0
D7	D6 mon	o SKC 20sistor	00 D4 (A	D3	Dra D291U9	ni nypria sa	80 "0"   Dogor s yo
ear Int. Gig	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm Alarm

#### Interrupt Operation

The interrupt output N-channel MOSFET is active at all times when the Interrupt Enable bit is set (bit 4 of the Command Register), and operates in both the standby and battery backup modes.

Since system power is usually applied between VDD and Vss, the user can connect the Interrupt Source (pin #11) to Vss. This allows the Interrupt Output to turn on only while system power is applied and will not be pulled to VSS during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (VBACKUP). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

#### Power-Down Detector of constal and alexan

The ICM7170 contains an on-chip power-down detector that eliminates the need for external components for the battery back-up function. Whenever the voltage from the VBACKUP pin to the VSS pin is less than approximately 1.0Volt, the chip automatically switches to battery backup operation. Until power is restored, operation is limited to time counting and interrupt generation only. All other functions are disabled to achieve micropower standby power and to preserve time integrity.

If standby battery operation is not required the VBACKUP should be connected to VDD.

#### APPLICATION NOTES In nettud and dutie desirable Time Synchronization

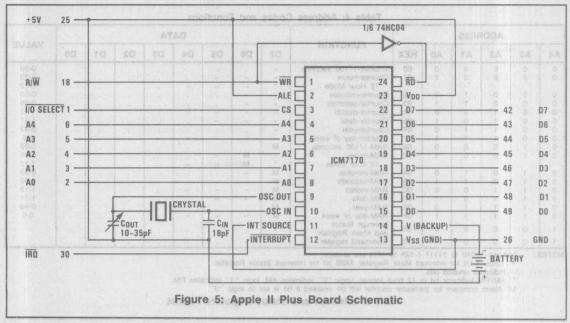
Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

#### Latched Data sets and retalloso of to gniedinon

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is stored into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle until the internal store operation is completed. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again.

(014 min) TUO OSO bris (014 min)



#### Control Lines

The RD, WR, and CS signals are active low inputs. Data is placed on the bus from counters or registers when RD is a logic "0". Data is transferred to counters or registers when WR is a logic "0". RD and WR must be accompanied by a logical "0" CS as shown in Figures 3 and 4.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0-A4 to the data lines D0-D4. To address the chip, the address is placed on the bus and ALE is strobed. On the falling edge, the address and CS information is read into the address latch and buffer. RD and WR are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to VDD.

#### Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz pulse train to the seconds counter, and speeds up the counting functions. a crit otni bereine semii beriseb erit nerit bris \$0

#### Oscillator Tuning behists hedt al dools and methods

Oscillator tuning should not be attempted by direct monitoring of the oscillator pins, unless very specialized equipment is used. External connections to the oscillator pins cause capacitive loading of the crystal, and shift the oscillator frequency. As a result, the precision setting being attempted is corrupted. One indirect method of determining the oscillator frequency is to measure the period between interrupts on the Interrupt Output pin (#12). This measurement must be relative to the falling edges of the INTER-RUPT pin. The oscillator set-up and tuning can be performed as follows:

1) Select one of 4, readily-available oscillator frequencies and place the crystal between OSC IN (pin #10) and OSC OUT (pin #9).

- 2) Connect a fixed capacitor from OSC IN to VDD.
- 3) Connect a variable capacitor from OSC OUT to VDD. In cases where the crystal selected is a 32kHz Statek type (CL = 9pF), the typical value of CIN = 18pF and COUT = 10-35pF.
- 4) Place a 5KΩ resistor from the INTERRUPT pin to VDD, and connect the INT SOURCE pin to Vss.
- 5) Apply 5V power and insure the clock is not in standby mode.
- 6) Write all 0's to the Interrupt Mask Register, disabling all interrupts.
- 7) Write to the Command Register with the desired oscillator frequency, Hours mode (12 hour or 24 hour), Run = "1", Interrupt Enable = "1", and Test = "0".
- 8) Write to the Interrupt Mask Register, enabling onesecond interrupts only.
- 9) Monitor the INTERRUPT output pin with a precision period counter and trim the OSC OUT capacitor for a reading of 1.000000 seconds. The period counter must be triggered on the falling edge of the interrupt output for this measurement to be accurate.
  - 10) Read the Interrupt Status Register. This action resets the interrupt output back to a logic "1" level.
- 11) Repeat steps 9 and 10 with a software loop. A suitable computer should be used.

# CIRCUIT APPLICATIONS

## Apple II Plus Real-Time Clock

Figure 5 shows the schematic of a board, using the ICM7170, that has been fabricated to plug into a slot in an Apple II Plus microcomputer. Very few external components are needed on the board to provide an interface to the Apple's 6502 MPU.

# IM4702/4712 Baud Rate Generator

#### GENERAL DESCRIPTION

The IM4702/12 Baud Rate Generators provide necessary clock signals for digital data transmission systems, such as UARTs, using a 2.4576MHz crystal oscillator as an input. They control up to 8 output channels and can be cascaded for output expansion.

Output rate is controlled by four digital input lines, and with the specified crystal, is selectable from "zero" through 9600 Baud. In addition, 19200 Baud is possible via hardwir-

Multi-channel operation is facilitated by making the clock frequency and the ÷8 prescaler outputs available externally. This allows up to eight simultaneous Baud rates to be

The IM4712 is identical to the IM4702 with the exception that the IM4712 integrates the oscillator feedback resistor and two load capacitors on-chip.

#### ORDERING INFORMATION

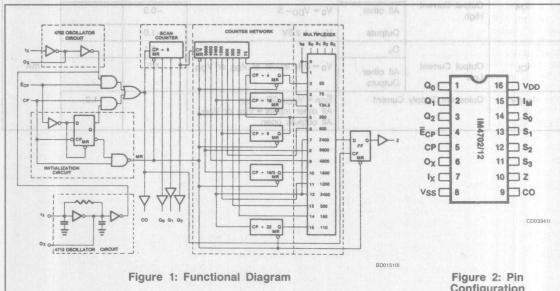
ORDER NUMBER	TEMPERATURE	PACKAGE
IM4702IJE	-40°C to +85°C	16-pin CERDIP
IM4702IPE	-40°C to +85°C	16-pin PLASTIC
IM4712IJE	-40°C to +85°C	16-pin CERDIP
IM4712IPE	-40°C to +85°C	16-pin PLASTIC

#### **FEATURES**

- **Provides 14 Most Commonly Used BAUD Rates**
- On-Chip Oscillator Requires Only One External Part (IM4712)
- Controls Up to Eight Transmission Channels
- TTL Compatible Outputs Will Sink 1.6mA
- Uses Standard 2.4576MHz Crystal
- Low Power Consumption: 5.5mW Guaranteed Maximum Standby
- Pin and Function Compatible With 4702B and HD-4702
- Inputs Feature Active Pull-Ups

#### PIN DESCRIPTION

SIGNAL	PIN	DESCRIPTION
Q <sub>0</sub> - Q <sub>2</sub>	1,2,3	Prescaler Outputs
ECP	\$1504	External Clock Enable Input
CP	enva5	External Clock Input
OX	6	Crystal Output
lx	7	Crystal Input
Vss alun	1018	Negative Supply
C <sub>0</sub> -	9 <sub>right</sub>	Clock Output
do Z	10	Baud Rate Output
S <sub>0</sub> - S <sub>3</sub>	14-11	Baud Rate Select Inputs
IM	15	Multiplexed Input
V <sub>DD</sub>	16	Positive Supply





## IM4702/4712



#### **ABSOLUTE MAXIMUM RATINGS**

 Storage Temperature Range ......-65°C to +150°C Operating Temperature Range .....-40°C to +85°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS V<sub>DD</sub> = +5V±10% V<sub>SS</sub> = 0V, T<sub>A</sub> = -40°C to +85°C

4702B and	competible With			og ar buall CIN	IITS	O Baud.
SYMBOL	PARAM aquiling syl	teature Act		MIN	MAX	UNIT
VIH	Input Voltage Hig	SCRIPTION	allable sylemally. PIN D	70% VCC	song 8 ant t	na yoneu
VIL	Input Voltage Lo	W MANAGE NAME OF THE PARTY OF T	Meso 90 OF Sets Fluer	ENDOS EDITORIOS	30% VCC	ewelV a
ėt.	Prescaler Outp	Other Inputs	VIN = VDD	S01#M1 ed to	recipitation s	Tabili ed
Enable Inpu	Input Current High	l <sub>x</sub> 4712	All other pins grounded	the oscillator		Mile (M4)
jugn!	External Glock	I <sub>x</sub> 4702	Pin under test at ground		-1	
li L	Input Current Low	I <sub>X</sub> 4712	All other Inputs at VDD	PROFITAL	+10	μА
	Negative Suppl	Other Inputs	SALANDO NO	-15	-100	SIGNO
VOH	Output Voltage F	ligh 0	$I_{OH} < -1\mu A$ ; Inputs at VSS or VDD	V <sub>DD</sub> 05		SOTAMI
VoL	Output Voltage L	w.w.	I <sub>OL</sub> < +1μA; Inputs at V <sub>SS</sub> or V <sub>DD</sub>	C to +86°C	0.05	1 <b>M</b> 47021
	Positive Supply	Ox	Inputs at V <sub>SS</sub> or V <sub>DD</sub>	-0.1	03-1-39	STYPIN
IOH	Output Current High	All other	$V_0 = V_{DD}5$	-0.3		
		Outputs	V <sub>0</sub> = +2.5V	-1.0	ROTALNOSO'S BODALO	
		O <sub>X</sub>	Juliania 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	-0.1	rocl	-d
IOL gov to at	Output Current Low	All other Outputs	$V_0 = 0.4$ ; Inputs at VSS or $V_{DD}$	1.6	de	mA
ISTBY	Quiescent Supply	Current	E <sub>CP</sub> = V <sub>DD</sub> ; CP = V <sub>SS</sub> All other Inputs = V <sub>SS</sub> or V <sub>DD</sub> , All outputs open		1.0	

Figure 2: Pin Configuration (Outline drawing

9-10

IM4702/4712

		en il e luta papavil		LIN	MITS	
SYMBOL	PARA	METER	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>plh</sub> (4702)	Salar and Mark		Part Commence of the	3890	350	
t <sub>phl</sub> (4702)		44			275	<b>第十十十</b>
t <sub>plh</sub> (4712)	Propagation de	Propagation delay <sup>(1)</sup> , CP to CO Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Z Propagation delay <sup>(1)</sup> , CO to Z Propagation delay <sup>(1)</sup> , CO to Z Propagation delay <sup>(1)</sup> , CO to Z Propagation delay <sup>(1)</sup> , CO to Z Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub> Propagation delay <sup>(1)</sup> , CO to Q <sub>n</sub>	Marie Contraction of the Contrac		350	
t <sub>pll</sub> (4712)			Tal-Market		275	
tplh	Propagation dalay(1) CP to CO		C <sub>L</sub> (except O <sub>x</sub> ) = 50pF	22 15 M	260	
tphl	Propagation de	lay(1), CP to CO	$C_{L(O_X)} = 7pF$		220	
t <sub>plh</sub>		(4)	No.	Z manifest	(2)	
tphl	Propagation de	lay <sup>(1)</sup> , CO to Q <sub>n</sub>	$R_L = 200k\Omega$		(2)	
tplh		41	Input May May		85	
tphl	Propagation de	lay(1), CO to Z	Transition times ≤ 20ns		75	ns
ttlh	Output Transition	on Time, (1)	Input low = 1.0V	100000000000000000000000000000000000000	160	
tthi	(except O <sub>x</sub> )		Input high = V <sub>CC</sub> -1.0V	МОІТЯІЯ	503.75 LAV	оптои
nortest	ades and Initia	Select to CO	ey a wide range of	350		sted letipiC
ts ARS	Set Up Time	I <sub>M</sub> to CO	gl emotipale roll) bu	350	bit rates, rangi	The second second
- "L mon l	L Glocke	Select to CO	speed modems) LUTII	0	emetric vivo	anical davi
9th mont t	Hold Time	I <sub>M</sub> to CO	of (aTRAU) after	no herionener	bris revieo	
twCP(L)	reseri J'i.	(0)	-fimensiii) maerte	120	elugni stab le	
twCP(H)	Clock pulse with	dth <sup>(3)</sup>	eam into parallel	120	ebio ni cavi	cul lane ( cours lane)
t <sub>w</sub> l <sub>x</sub> (L)(4702)	Inner I Activid		k rate which is a	polo 160 up	no recievar re	alsbite)
t <sub>w</sub> l <sub>x</sub> (H)(4702)	level WOJ =		ir MOSLSI UART ansmitted bit rate.	160	a incoming a	o abreicini s esu struc
t <sub>w</sub> l <sub>x</sub> (L)(4712)	I <sub>X</sub> Pulse Width		dock rates from	sbn 190 r at	12 can genera	
t <sub>w</sub> l <sub>x</sub> (H)(4712)	After Ero G			190	high frequen	10/11/100 0

NOTES: 1. Propagation delays and output transition times will vary with output load capacitance.

2. For multichannel operation, propagation delay (CO to Q<sub>n</sub>) plus set-up time (Select to CO) is guaranteed to be less than 367ns for the IM4702/12.

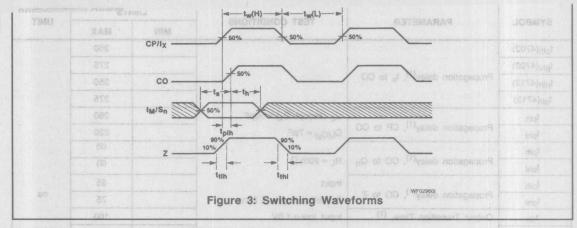
3. The first high level clock pulse after  $\overline{E}_{CD}$  goes low must be at least 200ns wide to ensure reseting of all counters.

as an internal + 16 prescaler). A lower input frequency will

4. For design reference only, not 100% tested.

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#### **FUNCTIONAL DESCRIPTION**

Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud (for electromechanical devices) to 9600 baud (for high speed modems). Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the reciever requires a clock rate which is a multiple of the incoming bit rate. Popular MOSLSI UART circuits use a clock that is 16 times the transmitted bit rate. The IM4702/12 can generate 14 standard clock rates from one common high frequency input.

The IM4702/12 contains the following five function subsystems.

**Oscillator** — For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The IM4702/12 can be driven from two alternate clock sources: (1) When the  $\overline{E}_{Cp}$  (External Clock Enable) input is LOW, the CP input is the clock source. (2) When the  $\overline{E}_{Cp}$  input is HIGH, a crystal connected between  $I_X$  and  $O_X$ , or a signal applied to the  $I_X$  input, is the clock source.

**Prescaler (Scan Counter)** — The clock frequency is made available on the CO (Clock Output) pin and is applied to the  $\div$  8 prescaler with buffered outputs  $Q_0$ ,  $Q_1$ , and  $Q_2$ .

Table 1: Clock Modes and Initialization

Ix	ECP	CP	OPERATION
X X X	O Hoole O'L of a H		Clocked from I <sub>X</sub> Clocked from CP Continuous Reset Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't Care

I = 1st HIGH Level Clock Pulse
After E<sub>CP</sub> Goes LOW

Clock Pulses

**Counter Network** — The prescaler output  $Q_2$  is a square wave of 1/8 the input frequency, and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is  $16 \times 9.6 \text{kHz} = 153.6 \text{kHz}$ . Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200.

bit rate 200 is divided by 4 to generate bit rate 50, bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of -0.87%, bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of -0.83%, and bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the  $\div$  16 feature of the UART, the resulting distortion is less than 0.78% regardless of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer — The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs  $(S_0-S_3).$  The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs  $(Q_0-Q_2).$  Table 2 lists the correspondance between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, nonstandardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S<sub>3</sub> input.

Initialization (Reset) — The initialization circuit generates a common master reset signal for all flip-flops in the IM4702/12. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the  $\overline{\mathbb{E}}_{CP}$  input goes LOW. Upon initialization, all counters are reset and all outputs will be in the LOW state. When  $\overline{\mathbb{E}}_{CP}$  is HIGH, selecting the Crystal input, CP must be LOW; a HIGH level on CP would apply a continuous reset.

All inputs to the 4702/12 except  $I_{\rm X}$  have on-chip pull-up circuits; the  $I_{\rm X}$  input of the 4712 has a high value resistor tied to  $O_{\rm X}$ .

Table 2: Truth Table for Rate Select Inputs

S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Output Rate (Z) Note 1
L L	L	t L	T	Multiplexed Input (I <sub>M</sub> ) Multiplexed Input (I <sub>M</sub> )
L	L	Н	L	50 Baud
L	L	H	Hear	75 Baud
L	Н	L	L	134.5 Baud
L	H	5 Las	o Ho	200 Baud
L	H	- H	L	600 Baud
L	Н	H	H	2400 Baud
Н	L	i vLana	o L	9600 Baud
Н	L	L	Н	4800 Baud
Н	L	Н	L	1800 Baud
Н	L	Н	Н	Horave 1200 Baud
Н	Н	LA	F	2400 Baud
Н	H-	- L	- H -	300 Baud
Н	Н	H	L	150 Baud
Н	Н	H	H	110 Baud

L = LOW Level has GOODS

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576MHz.

Table 3: Crystal Specifications

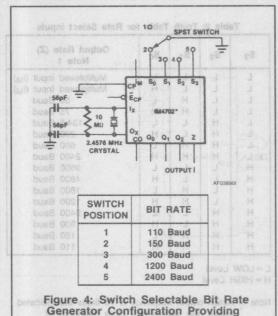
	TYPICAL CRYSTAL SPEC
Frequency Series Resistance	2.4576MHz ''AT'' Cut 250Ω
(Max) Unwanted Modes Type of Operation	-6dB (Min)
Load Capacitance	32pF±0.5pF

#### APPLICATIONS of elaponeral vite incupes of

#### Single Channel Bit Rate Generator

Figure 4 shows the simplest application of the IM4702/12. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (2) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 100, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

This mode of operation is commonly chosen for applications using industry standard 1402/6402 UARTs.



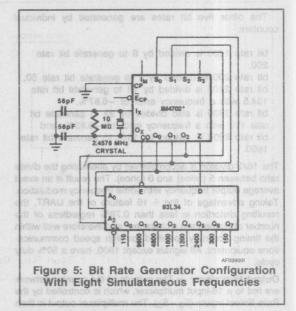
# Simultaneous Generation of Several Bit Rates

Five Bit Rates

Figure 5 shows a simple scheme that generates eight bit rates on eight output lines, using one IM4702/12 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q0 to Q2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select inputs of the multiplexer causes the IM4702/12 to sequentially interrogate the state of eight different frequency signals. The 93L34 Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) into eight parallel output frequency signals. In the simple scheme of Figure 5, input S<sub>3</sub> is left open (HIGH) and the following bit rates are generated:

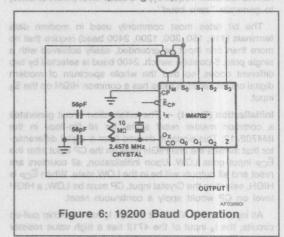
Q0:	110	Baud	11 18VOQ3	: 1800	Baud	Q6:	300	Baud
Q1: 9	600	Baud	Q <sub>4</sub>	: 1200	Baud	Q7:	150	Baud
Q2: 4	1800	Baud	Q5	: 2400	Baud			150,

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.



#### 19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the IM4702/12 can be used to generate this bit rate by connecting the Q<sub>2</sub> output to the I<sub>M</sub> input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the IM4702/12. (See Figure 6).



<sup>\*</sup> The 4712 may replace the 4702 in the above applications with the standard 2.4576MHz crystal. The two external capacitors and one resistor are not required when using the 4712.

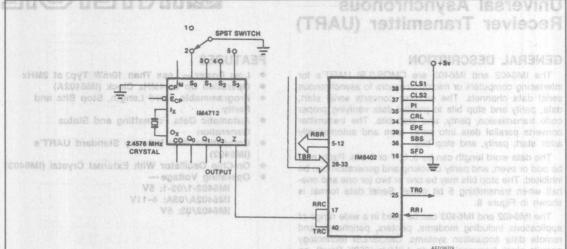


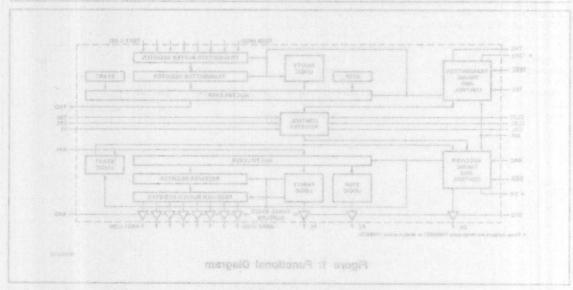
Figure 7: IM4712 Baud Rate Generator With IM6402 CMOS UART

simplifies the user interface

The IM6402 differs from the IM6403 in the use of five device give as indicated in Table 1 and Prouts 4.

#### DEDFEING INFORMATION

(M6402/03	ABOVAROSBIH	IBM6-10/2-1/03-1	зооо язоло
		IM6402-1703-IPL	PLASTIC PKG
			CERAMIC PKG
			MILITARY TEMP.
	IMEA02/03AMJL/HR		MILITARY TEMP WITH /Hi-Ret processing



9

#### **GENERAL DESCRIPTION**

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 8.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

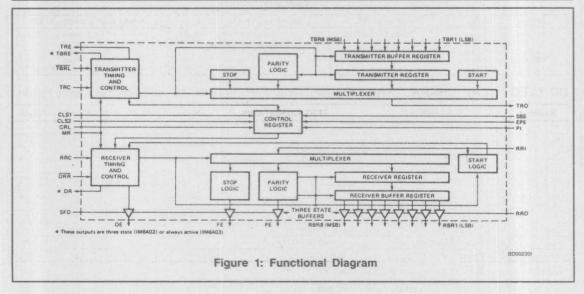
The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 4.

#### **FEATURES**

- Low Power Less Than 10mW Typ. at 2MHz
- Operation Up to 4MHz Clock (IM6402A)
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible With Industry Standard UART's (IM6402)
- On-Chip Oscillator With External Crystal (IM6403)
- Operating Voltage IM6402-1/03-1: 5V IM6402A/03A: 4-11V IM6402/03: 5V

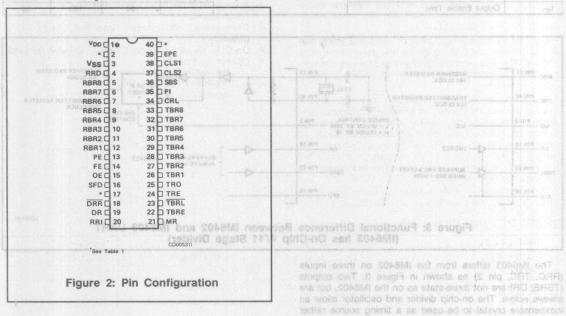
#### ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-IPL	IM6402/03AIPL	IM6402/03IPL
CERAMIC PKG	IM6402-1/03-1IJL	IM6402/03AIJL	IM6402/03IJL
MILITARY TEMP.	IM6042-1/03-1MJL	IM6402/03AMJL	
MILITARY TEMP. WITH /Hi-Rel processing	IM6402-1/03-1MJL/HR	IM6402/03AMJL/HR	



DITIONS TYP* TYP* UNIT T	Voltage On Any Input or Output Din (Voc. 0.2)
Operating Temperature	Voltage On Any Input or Output Pin (VSS -0.3V)
IM6402/03 (I)40°C to +85°C	to (V <sub>DD</sub> +0.3V)
Storage Temperature Range65°C to 150°C	Lead Temperature (Soldering, 10sec)300°C
Supply Voltage (VDD - VSS)+8.0V	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.



#### TABLE 1 additional directions as doubt and additional familiation and the transfer of the tran

PIN	IM6402	IM6403 w/XTAL	IM6403 W/EXT TTL CLOCK	IM6402 W/EXT CMOS CLOCK
2	N/C	Divide Control	Divide Control agreement and	Vent sos Divide Control (10) A (1)
17	RRC	XTAL	External Clock Input	No Connection
19	Tri-State	Always Active	Always Active	Always Active
22	Tri-State	Always Active	Always Active	Always Active
40	TRC	XTAL	Vss	External Clock Input

#### DC ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5.0V \pm 10\% V_{SS} = 0V$ , $T_A = Operating Temperature Range$ )

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>2</sup>	MAX	UNIT
ViH	Input Voltage High		V <sub>DD</sub> -2.0			V
VIL	Input Voltage Low				0.8	V
IIL	Input Leakage [1]	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-5.0		5.0	μΑ
VOH	Output Voltage High	I <sub>OH</sub> = -0.2mA	2.4	file of all the		V
VoL	Output Voltage Low	I <sub>OL</sub> = 1.6mA			0.45	V
lolk	Output Leakage	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>	-5.0		5.0	μΑ
ISTBY	Power Supply Current Standby	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub>		1.0	800	μΑ
IDD	Power Supply Current IM6402	f <sub>C</sub> = 500kHz			1.2	mA
IDD	Power Supply Current IM6403	f <sub>crystal</sub> = 2.46MHz			3.7	mA
CIN	Input Capacitance [1] [3]	T <sub>A</sub> = 25°C		7.0	8.0	pF
Co	Output Capacitance [1] [3]	T <sub>A</sub> = 25°C		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).

2. V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C.

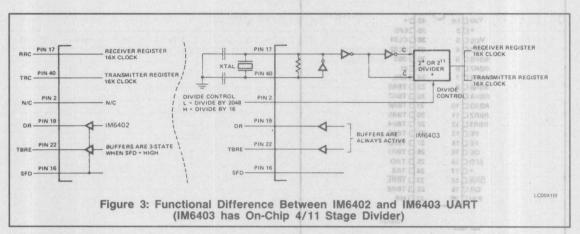
3. These parameters are guaranteed but not 100% tested.

# IM6402/IM6403



#### AC ELECTRICAL CHARACTERISTICS (VDD = 5.0V, ±10% VSS = 0V, CL = 50pF, TA = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>2</sup>	MAX	UNIT
fc	Clock Frequency IM6402	O*85 + of C	D.C.	7	1.0	MHz
fcrystal	Crystal Frequency IM6403	C to 150°C   esd Termos	20.	Pance	2.46	MHz
t <sub>pw</sub>	Pulse Widths CRL, DRR, TBRL	V0.8+	225	50	naVI sosii	ns
t <sub>mr</sub>	Pulse Width MR	See Timing Diagrams	600	200		ns
tds	Input Data Setup Time	(Figures 4,5,6)	75	20	an services arts	ns
t <sub>dh</sub>	Input Data Hold Time	ls may cause device failures.	oleag 90 bnetk	101 #40 flores	prites much	an ans
t <sub>en</sub>	Output Enable Time		company of the con-	80	190	ns



The IM6403 differs from the IM6402 on three Inputs (RRC, TRC, pin 2) as shown in Figure 3. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 12). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

Figure 2: Pin Configuration

IMTX\W 808408	ин
Always Active	
Always Active	

DC ELECTRICAL CHARACTERISTICS (VDD = 5.0V ±10% VSS = 0V, TA = Operating Temperature Range)

SAMBOT	PARAMETER	TEST CONDITIONS	\$4150	TYP2	XAM	
MV	ingut Vollaga High		V0D-2.0			
	Input Voltage Low				8.0	
HOV	Output Voltage High					V
	Output Voltage Low					
	Fewer Supply Current Standay					Aq
	Power Supply Ourrent M6402					Am
		foryetat = 2.46MHz				
CIN	Input Capacitance [1] [3]					

100 EDA T (coep) MABAGE XTAL input pins the pins TX and TX in to the total XX and XX in the total XX in the to

#### (IM6402AI/AM, IM6403AI/AM) ABSOLUTE MAXIMUM RATINGS

0°081+ of 0°88- epis H outs to (VDD +0.3V)

Operating Temperature Range
IM6402AI/03AI40°C to +85°C
IM6402AM/03AM55°C to +125°C
Storage Temperature Range65°C to 150°C
Lead Temperature (Soldering, 10sec)300°C

ABSOLUTE MAXIMUM RATINGS

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

#### DC ELECTRICAL CHARACTERISTICS (VDD = 4.0V to 11.0V VSS = 0V, TA = Operating Temperature Range)

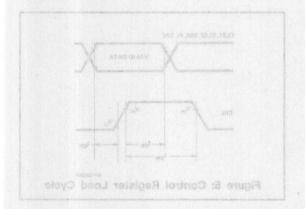
THE PARTY OF THE P	THE PARTY OF THE P		The second secon	ALL THE REAL PROPERTY.		Administration of the facility
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>2</sup>	MAX	UNIT
VIH	Input Voltage High		70% V <sub>DD</sub>	yes) pos/	aV Juoni	V
VIL	Input Voltage Low	Vals 5 Van 5 Vans		(6) (11 eps)s	10% V <sub>DD</sub>	V
TiLy	Input Leakage [1] [3]	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1.0	doiti enerio	1.0	μΑ
VOH	Output Voltage High	IOH = OmA		V <sub>DD</sub> -0.01	/ number	V
VOL	Output Voltage Low	IOL = OmA		V <sub>SS</sub> + 0.01	LiugiuO	V
lolk	Output Leakage	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>	-1.0	sensoO vigas	8 1.0 E	μΑ
loc	Power Supply Current Standby	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub>	neavo Sobaliti	5.0	500	μΑ
loc	Power Supply Current IM6402A	f <sub>crystal</sub> = 4MHz	more Cusemi	sersiO vleas	9.0	mA
lcc	Power Supply Current IM6403A	f <sub>crystal</sub> = 3.58MHz	181	H-eonatiose	13.0	mA
CIN	Input Capacitance [1] [3]	T <sub>A</sub> = 25°C	ISTI	7.0 500	8.0	pF
Co	Output Capacitance [1] [3]	T <sub>A</sub> = 25°C		8.0	10.0	pF

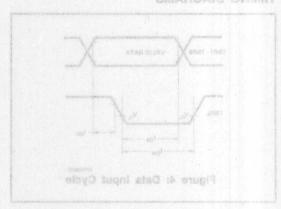
NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).

2. V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C.
3. These parameters are guaranteed but not 100% tested.

#### AC ELECTRICAL CHARACTERISTICS W AC ELECTRICAL CHARACTERISTICS (VDD = 10.0V ±5% VSS = 0V, CL = 50pF, TA = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN ON	TYP <sup>2</sup>	MAX	UNIT
forting	Clock Frequency IM6402A		D.C.ookai	i vanouaer	4.0	MHz
fcrystal	Crystal Frequency IM6403A	See Timing Diagrams (Figures 4,5,6)	JART AN	JRO amb	6.0	MHz
tpw	Pulse Widths CRL, DRR, TBRL		100	40	W setu9	ns
t <sub>mr</sub>	Pulse Width MR		400	200	aC Junet Da	ns
tds	Input Data Setup Time		40	0 20 61	act tuent	ns
tdh	Input Data Hold Time		30	30	a trotuci i	ns
ten	Output Enable Time	The second of the second secon		40	70	ns





# IM6402/IM6403



#### (IM6402-11/1M, IM6403-11/1M) **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (VDD - VSS)	+8.0V
/oltage On Any Input or Output Pin (Vss -	-0.3V)
to (V <sub>DD</sub> +	0.3V)

Operating Temperature Range	
IM6402-11/03-11	40°C to +85°C
IM6402-1M/03-1M	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

#### DC ELECTRICAL CHARACTERISTICS (V<sub>DD</sub> = 5.0 ±10% V<sub>SS</sub> = 0V, T<sub>A</sub> = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>2</sup>	MAX	UNIT
VIH	Input Voltage High	SURGEOUS TOST	V <sub>DD</sub> -2.0	A STATE OF THE STA		V
VIL	Input Voltage Low			Agar again	0.8	V
1p2 0	Input Leakage [1] [3]	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1.0	laga Low	1.0	μΑ
VOH	Output Voltage High	$I_{OH} = -0.2 \text{mA}$	2.4	ETTI SERVE	art India	V
Vol	Output Voltage Low	I <sub>OL</sub> = 2.0mA		rigiFl agello	0.45	V
lolk	Output Leakage	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>	-1.0	Mo'l adalo	1.0	μΑ
Icc	Power Supply Current Standby	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub>		1.0	100	μΑ
Icc	Power Supply Current IM6402 Dynamic	f <sub>C</sub> = 2MHz	ydnrast .	upply Current	1.9	mA
lcc	Power Supply Current IM6403 Dynamic	f <sub>crystal</sub> = 3.58MHz	ASCNAME	retruct yingst	5.5	mA
CIN	Input Capacitance [1] [3]	T <sub>A</sub> = 25°C	Accepm	7.0	8.0	pF
Co	Output Capacitance [1] [3]	T <sub>A</sub> = 25°C	(8)	8.0	10.0	pF

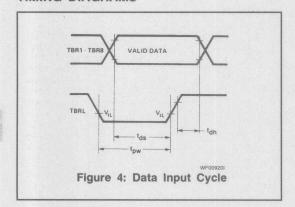
NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).

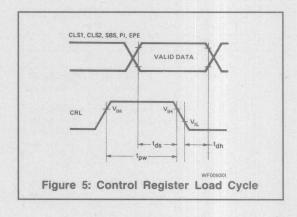
V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C.
 These parameters are guaranteed but not 100% tested.

#### AC ELECTRICAL CHARACTERISTICS (VDD = 5.0V ±10% VSS = 0V, CL = 50pF, TA = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>2</sup>	MAX	UNIT
fc	Clock Frequency IM6402-1	DITION TON!	D.C.	AND AND AND AND AND AND AND AND AND AND	2.0	MHz
fcrystal	Crystal Frequency IM6403-1	See Timing Diagrams (Figures 4,5,6)	ASOM	adnewsk tive	3.58	MHz
tpw	Pulse Widths CRL, DRR, TBRL		150	50	Crystel	ins
t <sub>mr</sub>	Pulse Width MR		400	200	W self	ns
t <sub>ds</sub>	Input Data Setup Time		50	20	W BENG	ns
tdh	Input Data Hold Time		60	40	DCI TUÇNI	ns
ten	Output Enable Time			80	160	ns

#### TIMING DIAGRAMS





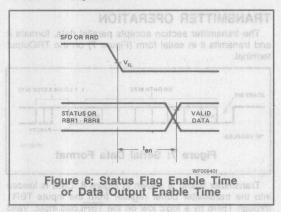


Table 1: IM6402/3 Pin Description

PIN	SYMBOL	DESCRIPTION	
	lock coovs later	Positive Power Supply	
	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2 <sup>4</sup> (16) Divider Low: 2 <sup>11</sup> (2048) Divider	
310	menuVssil to no	Negative Supply Wall and All a	
4	RRD acie	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.	
5	RBR8	The contents of the RECEIVE BUFFER REGISTER appear of these three-state outputs. Wor formats less than 8 character are right justified to RBR1.	
6	RBR7	See Pin 5 — RBR8	
7.00	RBR6	See Pin 5 — RBR8	
8	RBR5	See Pin 5 — RBR8	
9	RBR4	See Pin 5 — RBR8	
10	RBR3	See Pin 5 — RBR8	
11	RBR2	See Pin 5 — RBR8	
12	RBR1	See Pin 5 — RBR8	
13	PE	A high level on PARITY ERRO indicates that the received pari does not match parity programmed by control bits. The output is active until parimatches on a succeeding character. When parity is inhibited, this output is low.	
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.	

PIN	SYMBOL	DESCRIPTION	
	OE MOTORIPTION data start data appear sensity a inter REGIS data is loaded in inter BUFFE	received flag was not cleared before the last character was	
	SFD SFD SFD SFD SFD SFD SFD SFD SFD SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE FE, OE, DR*, TBRE* to a high impedance state. See Block Diagram and Figure 6.	
17	IM6402-RRC IM6403-XTAL	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.	
18	DRR	A low level on DATA RECEIVE RESET clears the data receive output (DR), to a low level.	
	DRIT — 85 FMOO no leve closed GAOJ FI	A high level on DATA RECEIVE indicates a character has bee received and transferred to the receiver buffer register.	
	PRI YTIHA'I no les entry living generation, and forces PF	Serial data on RECEIVER REGISTER INPUT is clocked infithe receiver register.	
	RM avet on STOP selects 1.5 stop b cler format and 2 ther lengths. sputs program	TRE returns high MR does no	
	D. (Ct. SART) St. (ct. SART) St. (ct. SART) St. (ct. SART) St. (ct. SART) St. (ct. SART) St. (ct. SART) St. (ct. SART)	A high level on TRANSMITTEI BUFFER REGISTER EMPT' indicates the transmitter buffer register has transferred its data to the transmitter register and it ready for new data.	
even ode	is low JR8Tgn lev ARITY ENAPL s and checks low level selecti NSMITTER RECI (Alon)	BUFFER REGISTER LOAD transfers data from inputs TBR TBR8 into the transmitter buffer register. A low to high transfer	
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.	

# IM6402/IM6403

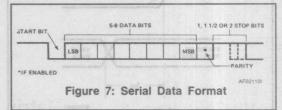
Table 1: IM6402/3 Pin Description

	CALL STATE OF THE	(CONT.)
PIN	SYMBOL	ROARS DESCRIPTION
25	TRO TRO TO THE TROP TROP TROP TROP TROP TROP TROP TROP	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	, e.i) TBR1cheq (v.e.,	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-
a PE, rigid	vel on STATUS FI forces the output DR*, TBRE* to a be state. See four and Figure 8.	TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	ovieoTBR4 X81	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	evel TBR7 of (R	See Pin 26 — TBR1
33	TBR8 no la	See Pin 26 — TBR1
34	CRL box box box detailed within	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 5.
	R MPUT is clocked register.  Telegister.  Telegister.	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
s (cnay,	SBS*  OOKS SITE IN SOS  THE TIEN MIT GOS	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
RBT YT9I	vel on TRANSMI NE OISTER EA the transmitter as transferred its of control register.	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits)(CLS1 high CLS2 low 6-bits)(CLS1 low CLS2 high 7-bits)(CLS1 high CLS2 high 8-bits)
38	CLS1* wen	See Pin 37 — CLS2
DAD BRT- buffer sition	REGISTER L REGISTER L data from Inputs 3 the transmitter low to high tran	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

\*See Table 2 (Control Word Function)

# TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal.



Transmitter timing is shown in Figure 8. Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the TBRLoad input. Valid data must be present at least tos prior to and toh following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock, which is 16 times the data rate. A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Data is automatically transferred to the transmitter register and transmission of that character begins.

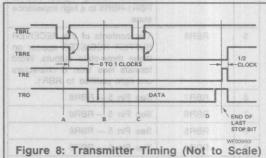


Table 2: Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT		
CLS2	CLS1	Bo Plander	EPE	SBS	d (CPIL) can be field	ontrol Register Los	ring operation, D	
receiged.	d chargoter i	ilsv iten ed	listra Edilisis   di	of L	pay to 5 y tank	ODD	e angel Jeeunu	
ent miles trains	ava al acutus	Notes Laura at	none Inmet	Н	5	ODD	1.5	
			ecery D. FE		ther and igceiver will	EVEN	is may bright and	
Land and the same of			Harach Haracon		aud Rate Generator.	EVEN	1.5	
L	Transfer St.	Н	X	L	A SQABMILEST VIOLENE			
retospacter	reserve to the	a a (Ha) 101	io maximo of the	Н	Master & cost (MFI)	DISABLED	teast 1.5 feuri	
MAN HETTERD	BUP HER RE	RECTIVER	edi of Loanster	BIT L	liably fro a Schmitter	a nevi ODD 180 br	is active trigin, a	
w nig EO en!	.bss Hreed	acter gas no	previous char	H The	ample, 191 MBUC46	ODD OF	bna religion reg	
PROLE TOUR	tid chis bet	eser (xen e	y high Hrai th	sla L	The Scients bigger	notion EVENTORS	eset through st	
L	Н	L	Hospings	teg H	behade 6 at How	on O-EVEN TORRE	good en2 neew	
L	H	H	X	L	6	DISABLED		
L	Н	Н	X	Н	6	DISABLED	2	
Н	L	L	L les	L	7	ODD	1	
Н	L	L	L	Н	7	ODD	2	
Н	L	L	H	L	7	EVEN	1	
Н	L	L	Н	Н	7	EVEN	2	
Н	L	Н	X	asps L	7	DISABLED	1	
Н	L	Н	X	Н	7	DISABLED	2	
Н	Н	L	63 L 205448	L	8	ODD	1	
Н	Н	L	pL p3 3	e H	8	ODD	2	
Н	Н	L	Н	L	8	EVEN	1	
Н	Н	L	TH 1	Н	8	EVEN	2	
Н	H	- Н	X	L	8	DISABLED	1	
Н	н	H	X	Н	8	DISABLED	2	

x = Don't Care

## RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 9.

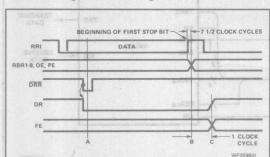


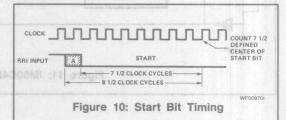
Figure 9: Receiver Timing (Not to Scale)

A low level on DRReset clears the DReady line. During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. 1/2 clock cycle later, DReady is set to a logic high and FError is evaluated. A

logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

# START BIT DETECTION

The receiver uses a 16X clock for timing. (See Figure 10.) The start bit (A) could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count  $7\frac{1}{2}$ . If the receiver clock is a symmetrical square wave, the center of the start bit will be located within  $\pm 1/2$  clock cycle,  $\pm 1/32$  bit or  $\pm 3.125\%$ . The receiver begins searching for the next start bit at the center of the first stop bit.



#### TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 11 shows how the IM6402 can be interfaced to an IM80C48 microcomputer system.

ted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs should be tied to either V<sub>DD</sub> or V<sub>SS</sub>.

The baud rate at which the transmitter and receiver will operate is determined by the IM4702 Baud Rate Generator.

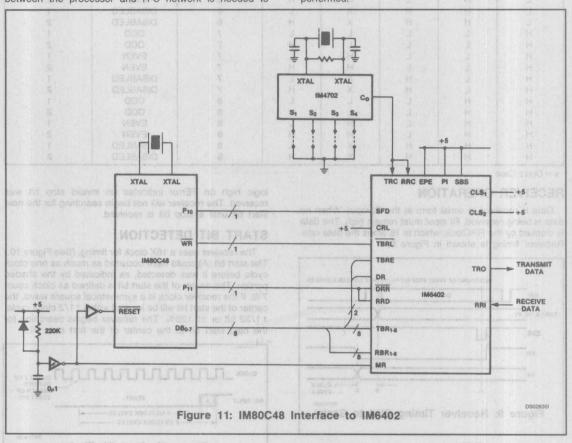
To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM80C48 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to

trigger RESET. A long reset pulse after power-up (~20ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a DRR is performed.



# IM6653/IM6654 4096-Bit CMOS UV EPROM



# GENERAL DESCRIPTION THE STATE OF THE STATE O

The Intersil IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

# **FEATURES**

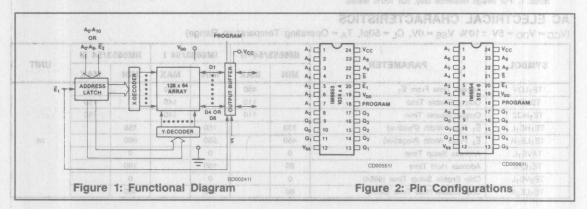
- Organization IM6653: 1024 x 4
- Low Power 770μW Maximum Standby
- High Speed
  - -300ns 10V Access Time For IM6653/54 AI -450ns 5V Access Time For IM6653/54-1I
- Single +5V Supply Operation
- OC ELECTRICAL CHARACTE SIdesers VV .
- Synchronous Operation For Low Power (V = 00V)
- Three-State Outputs and Chip Select for Easy System Expansion (MA)

Logical "0" Input Voltage

# ORDERING INFORMATION

Au PART NUMBER	1.0	TEMPERATURE RANGE	PACKAGE
IM6653/4IJG	0.45	-40°C to +85°C	24-Pin CERDIP
IM6653/4-1IJG	0.1	-40°C to +85°C	24-Pin CERDIP
IM6653/4AIJG	000	-40°C to +85°C	24-Pin CERDIP
IM6653/4MJG*	8	-55°C to +125°C	24-Pin CERDIP
IM6653/4AMJG*	7.0	-55°C to +125°C	24-Pin CERDIP

<sup>\*</sup> Add /HR for HiRel processing



# IM6653/IM6654



# ABSOLUTE MAXIMUM RATINGS (IM6653/54 I, -11, M)

Supply Voltages	Operating Range Range (TA)
VDD - VSS +8.0V	Industrial40°C to +85°C
Vcc - Vss +8.0V	Military55°C to +125°C
Input or Output Voltage (VSS -0.3V) to (VDD +0.3V)	Storage Temperature Range65°C to +150°C
values Standby Waximus Standby	Lead Temperature (Soldering, 10sec)300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = V_{DD} = 5V \pm 10\% V_{SS} = 0V, T_A = Operating Temperature Range)$ 

	hree-State Outputs and Chip Se-	TECT	IM6653	program devel		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	ms UNIT	
VIH	Logical "1" Input Voltage	Ē₁, Š	V <sub>DD</sub> - 2.0	.bemmstpp	ger nadt bris	
VIH		Address Pins	2.7	TOTA BACKEVORAL O	V	
VIL	Logical "0" Input Voltage		(F) (S) (A)	0.8	SALISTON IN	
l <sub>l</sub>	Input Leakage	$GND \le V_{IN} \le V_{DD}$	ESTO -1.0 CM3	1.0	μΑ	
Voн	Logical "1" Output Voltage	$I_{OH} = -0.2mA$	2.4	2000年	以以此	
VoL	Logical "0" Output Voltage	I <sub>OL</sub> = 2.0mA	10°0 to +85.10	0.45	DUBASSASIO	
lolk	Output Leakage	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	Pag 1.0 0 00	1.0	111-618374-11	
ISTBY	Standby Supply Current	V <sub>IN</sub> = V <sub>DD</sub>	loan - La rideo	100	μΑ	
Icc		V <sub>IN</sub> = V <sub>DD</sub>	100	40	DUTH HECOOM	
IDD	Operating Supply Current (1)	f = 1MHz	1.481 + 14 O.P	6	mA	
CI	Input Capacitance	Note 1	S'C to + 125°	7.0	MARKESS/ARM	
Co	Output Capacitance	Note 1		10.0	pF	

Note: 1. For design reference only, not 100% tested.

# AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = V<sub>DD</sub> = 5V ±10% V<sub>SS</sub> = 0V, C<sub>L</sub> = 50pf, T<sub>A</sub> = Operating Temperature Range)

SYMBOL		IM6653/54-11		IM6653/54 I		IIM6653/54 M		
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
TE <sub>1</sub> LQV	Access Time From E <sub>1</sub>	*	450		550	3/8K	600	1 1
TSLQV	Output Enable Time	A CONTRACTOR	110	1 2	140	12	150	
TE <sub>1</sub> HQZ	Output Disable Time		110	1 80 40 7	140		150	
TE1HE1L	Ē <sub>1</sub> Pulse Width (Positive)	130		150	0000380.8 T	150	B Hall B	
TE1LE1H	E <sub>1</sub> Pulse Width (Negative)	450		550	75	600	FIRE	ns
TAVE <sub>1</sub> L	Address Setup Time	. 0		0		0		
TE <sub>1</sub> LAX	Address Hold Time	80		100		100		
TE <sub>2</sub> VE <sub>1</sub> L	Chip Enable Setup Time (6654)	0	7105000	0		0		
TE <sub>1</sub> LE <sub>2</sub> X	Chip Enable Hold Time (6654)	80	7-1-8	100	IERODA	100	物の形形を	

# IM6653/IM6654

# ABSOLUTE MAXIMUM RATINGS (IM6653/54AI, AM)

Supply Voltages	Operating Temperature Range
V <sub>DD</sub> - V <sub>SS</sub> +11	1.0V Industrial40°C to +85°C
Vcc - Vss + 11	1.0V Military55°C to +125°C
Input or Output Voltage (VSS -0.3V) to (VDD +0	.3V) Storage Temperature Range65°C to +150°C
Size	Lead Temperature (Soldering, 10sec)300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS

(VCC = VDD = 4.5V to 10.5V VSS = 0V, TA = Operational Temperature Range)

The second	The state of the s	esq rettus turnus	IM665	1 48	
SYMBOL	PARAMETER	TEST CONDITIONS	MIN M	MAX	OM CHIT
VIH	Logical "1" Input Voltage	E <sub>1</sub> , S to bas	V <sub>DD</sub> - 2.0	READ operation	In a bypica
VIH	K** ,5	Address Pins Pins	V <sub>DD</sub> - 2.0	rationed by the fall	ns "savidan
VIL	Logical "0" Input Voltage	Grees pure	eno saugluo i	0.8 0.8	bilsV (0 = 1
har har	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1.0	1.0	μΑ'
VOH	Logical "1" Output Voltage	I <sub>OUT</sub> = 0 (Note 1)	V <sub>CC</sub> - 0.01	BU BINDY STREET BY	U 15 " 17 WI
VOL	Logical "0" Output Voltage	I <sub>OUT</sub> = 0 (Note 1)	DOUGH TIPLIT	V <sub>SS</sub> + 0.01	1 19 API AIBIU
lolk	Output Leakage	V <sub>SS</sub> ≤ V <sub>0</sub> ≤ V <sub>CC</sub>	-1.0	1.0	
ISTBY	Standby Supply Current	$V_{IN} = V_{DD}$	quies one bie	/ 90 181 100	μΑ
lcc	promountain management of	$V_{IN} = V_{DD}$	Self-1009-14-17	40	bns (UEVA)
IDD	Operating Supply Current	f = 1MHz	The self to	12	mA
CI	Input Capacitance	Note 1	and objects to	7.0	ori la lett a tutte
Co	Output Capacitance	Note 1		10.0	pF

Note: 1. For design reference only, not 100% tested.

# AC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = V_{DD} = 10V \pm 5\% V_{SS} = 0V, C_L = 50pf, T_A = Operating Temperature Range)$ 

SYMBOL	A CALADA LA PARTICIONA DE LA CAMATA	IM6653/	54 AI	IM6653		
	PARAMETER	MIN	MAX	MIN	MAX	UNIT
TE <sub>1</sub> LQV	Access Time From E <sub>1</sub>		-300		350	
TSLQV	Output Enable Time		60	PTURN	70	
TE <sub>1</sub> HQZ	Output Disable Time	1 0000000	60		70	3ME
TE <sub>1</sub> HE <sub>1</sub> L	E <sub>1</sub> Pulse Width (Positive)	125	A.	125	3 1.13	299
TE <sub>1</sub> LE <sub>1</sub> H	E <sub>1</sub> Pulse Width (Negative)	300	-1	350	C 1 H-1-	ns
TAVE <sub>1</sub> L	Address Setup Time	0		0		A CONTRACTOR
TE <sub>1</sub> LAX	Address Hold Time	60	17	60		
TE <sub>2</sub> VE <sub>1</sub> L	Chip Enable Setup Time (6654)	0		0		
TE <sub>1</sub> LE <sub>2</sub> X	Chip Enable Hold Time (6654)	60	1 X	60		

PIN	SYMBOL	LEVEL	DESCRIPTION REGISTORY VIQUE
1-8,23	A <sub>0</sub> -A <sub>7</sub> ,A <sub>8</sub>	Viscosition.	Address Lines
9-11, 13-17	Q <sub>0</sub> -Q <sub>7</sub> Q <sub>0</sub> -Q <sub>3</sub>	របស់នាច់ណ្ឌិច ខែ ១០ន	Data Out lines, 6654 Data Out lines, 6653
12	V <sub>SS</sub>	S. S. S. S. S. S. S. S. S. S. S. S. S. S	Negative Supply
18	Program	of sometimes and some	Programming pulse input
19	V <sub>DD</sub>	Cartie Total Cartie Control	Chip positive supply, normally tied to VCC
20	Ē <sub>1</sub>	L	Strobe line, latches both address lines and, for 6654, Chip enable E2
21	S	L	Chip select line, must be low for valid data out
22	Ag E <sub>2</sub>	(epress en	Additional address line for 6653 Chip enable line, latched by Chip enable E <sub>1</sub> on 6654
24	Vcc		Output buffer positive supply

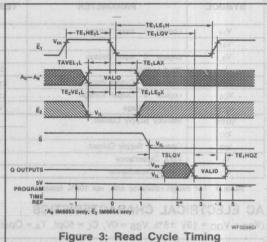
# READ MODE OPERATION

In a typical READ operation address lines and chip enable  $\overline{E}_2^*$  are latched by the falling edge of chip enable  $\overline{E}_1$  (T = 0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line  $\overline{S}$  is low (T = 3). Data remains valid until either  $\overline{E}_1$  or  $\overline{S}$  returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and  $\overline{E}_2$  must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of  $\overline{E}_1$  starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE<sub>1</sub>HQZ) after any rising edge on  $\overline{E}_1$  or  $\overline{S}$ .

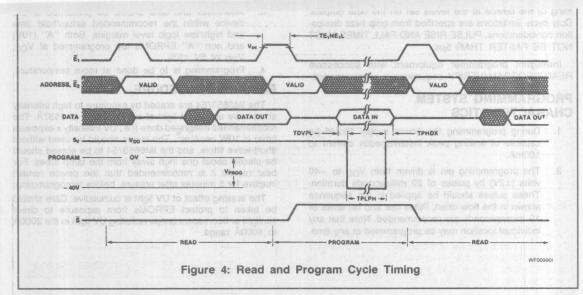
The program line remains high throughout the READ cycle.

Chip enable line  $\overline{\mathbb{E}}_1$  must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.



# **FUNCTION TABLE**

TIME	TIME INPUTS		OUTPUTS	-TSLOY   Gisput Enable Tans				
REF	Ē1	Ē2	S	A	Q	TENEDA CONDUCTION OF THE CONTROL OF		
-1	Н	X	X	X	Z	DEVICE INACTIVE		
0	_/_	Ļ	X	V	Z	CYCLE BEGINS; ADDRESSES, E2 LATCHED*		
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY		
2	L	X	L	X	A 00	OUTPUTS ACTIVE UNDER CONTROL OF E1, S		
3	L	X	L	X	٧	OUTPUTS VALID AFTER ACCESS TIME		
4	1	X	L	X	٧	READ COMPLETE		
5	Н	X	X	X	Z	CYCLE ENDS (SAME AS -1)		



# DC CHARACTERISTICS FOR PROGRAMMING OPERATION

 $(V_{CC} = V_{DD} = 5V \pm 5\% V_{SS} = 0V, T_A = 25^{\circ}C)$ 

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IPROG	Program Pin Load Current			80	100	mA
VPROG	Programming Pulse Amplitude		-38	-40	-42	. V
Icc	V <sub>CC</sub> Current			0.1	5	
IDD	V <sub>DD</sub> Current		BITALE SUI	40	100	mA -
VIHA	Address Input High Voltage	Thursday 9	V <sub>DD</sub> -2.0			
VILA	Address Input Low Voltage				0.8	100
V <sub>IH</sub>	Data Input High Voltage		V <sub>DD</sub> -2.0			V
VIL	Data Input Low Voltage		The state of the s		0.8	

# AC CHARACTERISTICS FOR PROGRAMMING OPERATION

 $(V_{CC} = V_{DD} = 5V \pm 5\% V_{SS} = 0V, T_A = 25^\circ)$ 

SYMBOL	PARAMETER	TEST	MIN	TYP	MAX	UNIT
TPLPH	Program Pulse Width	t <sub>rise</sub> = t <sub>fali</sub> = 5μs	18	20	22	ms
	Program Pulse Duty Cycle				75%	
TDVPL	Data Setup Time		9			THE REAL PROPERTY.
TPHDX	Data Hold Time		9			μs
TE <sub>1</sub> HE <sub>1</sub> L	Strobe Pulse Width		150			
TAVE <sub>1</sub> L	Address Setup Time		0	11.09.73		
TE <sub>1</sub> LE <sub>1</sub> X	Address Hold Time	A STATE OF THE STA	100		Tes Veries	ns
TE <sub>1</sub> LQV	Access Time				1000	

## PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V<sub>CC</sub> and V<sub>DD</sub> are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must

be set at V<sub>DD</sub> -2V minimum. Low logic levels must be set at V<sub>SS</sub> +0.8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ( $\overline{\mathbb{S}}$ ) pins are set high. The address is latched by the downward edge on the strobe line ( $\overline{\mathbb{E}}_1$ ). During valid DATA IN time, the PROGRAM pin is pulsed from V<sub>DD</sub> to -40V. This pulse initiates the program-

# IM6653/IM6654



ming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5µs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

# PROGRAMMING SYSTEM CHARACTERISTICS

- During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
- 2. The programming pin is driven from V<sub>DD</sub> to -40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.

 Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V<sub>CC</sub>, V<sub>DD</sub> of 5V ±5%.

4. Programming is to be done at room temperature.

# ERASING PROCEDURE

The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm². The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cumulative. Care should be taken to protect EPROMs from exposure to direct sunlight or fluorescent lamps radiating UV-light in the 2000Å to 4000Å range.

Figure 4: Read and Program Cycle Timing

# OC CHARACTERISTICS FOR PROGRAMMING OPERATION

TYP	19163	TEST CONDITIONS"	PARAMETER	
				PROG
			Programming Pulse Amplifludu	
			Address Inpid Low Vollage	
			Data Input High Verlage	

# AC CHARACTERISTICS FOR PROGRAMMING OPERATION

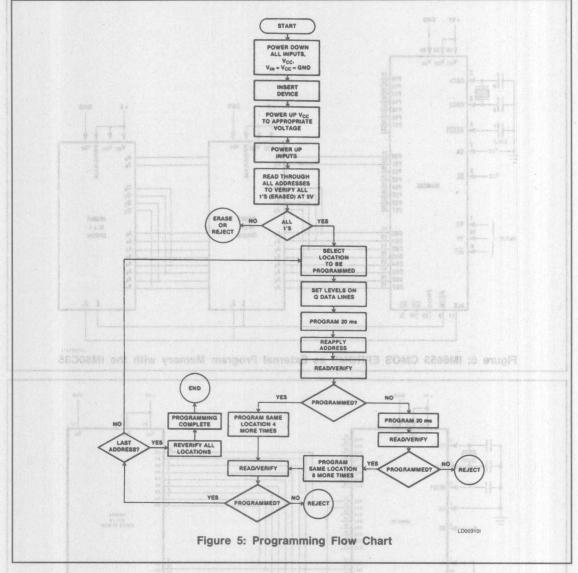
TIMO		CONDITIONS CONDITIONS	PARAMETER	SYMBOL
311			Program Putse Width	
			Program Palsa Duty Cycle	
			Data Setup Time	
				Jramat.
			Address Satur Time	TAVELL
			Address Hold Time	

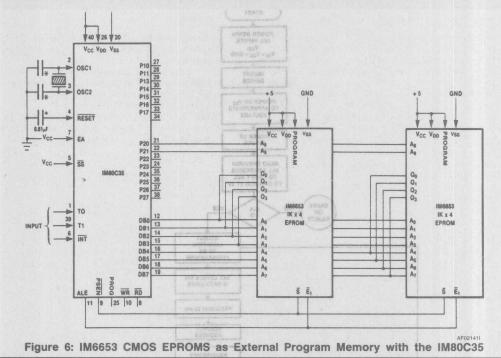
se set at V<sub>DD</sub> ~2V minimum. Low logic tovels must be set at V<sub>SD</sub> + 0.8V maximum. Addressing of the desired location of PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levers, and PROGRAM and only select (S) pins are set high. The address is istiched by the downward edge on the strobe line E<sub>1</sub>). During valid DATA IN time, the PROGRAM pin is subsetting when the ADD This guise initiates the programmations.

#### MOSTARRION MOONE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (autout high) state. Selective programming of proper bit locations in "0"s is performed electrically.

In the PROCRAM mode for all EPROMs, Voc and Vpp are tied together to a +5V operating supply. High logic levels at all of the appropriate cate inputs and outputs must levels at all of the appropriate cate inputs and outputs must





The Intersil IM80C48 family of CMOS microcontrollers combines the speed of the industry standard NMOS8048 with the low power consumption of CMOS. In addition to the low operating current, the IM80C48 family has three versatile power-down modes that reduce power dissipation even further. The HALT mode, entered by software command, shuts down selected portions of the CPU to reduce power consumption while retaining rapid response time to an interrupt or reset. The STandBY and STOP modes shut down all but the onboard RAM, reducing the supply current to typically 1 microamp.

The IM80C48 family microcontrollers include 27 I/O lines, RAM, and an 8-bit timer/counter on-chip, and are well suited for control applications. The low power consumption of the IM80C48 makes it particularly desirable in applications that require battery operation or long term battery backup of on-chip RAM during AC power interruptions.

# FEATURES WE De and I may you no eq

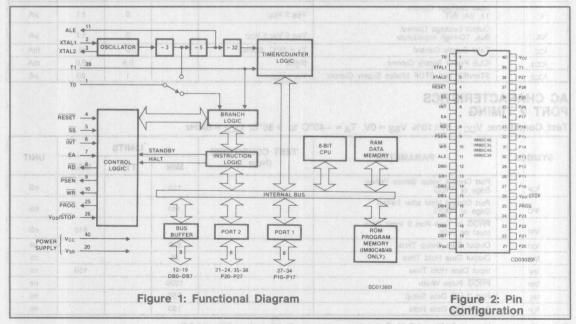
- Industry Standard NMOS 8048 Family Compatible
- Expanded Instruction Set Includes Software STandBY
- Ultra Low Power Consumption
  - Operating Supply Current: 3mA at 6MHz
  - IDLe Supply Current: 800μA at 6MHz - STandBY and STOP Modes: 1μA
- Wide Operating Voltage Range 3.5V to 6V
- Compatible with 8048/80/85 Peripherals
- 4 Standard ROM and ROM-Less Versions

# **APPLICATIONS**

- Portable Instrumentation
- Telecom
- Industrial Control
- Battery Operated Equipment

# ORDERING INFORMATION

V noV	Va A	SUFFIX					
BASIC PART NUMBER	TEMP. RANGE: 0°C to +70°C		TEMP. RANGE: -40°C to +85°C		media an	spalley wou	
Y	40-PIN PLASTIC	40-PIN CERDIP	40-PIN PLASTIC	40-PIN CERDIP	ROM	RAM	
IM80C48	CPL	CJL	IPL	IJL	1K x 8	64 x 8	
IM80C49	CPL	CJL	IPL	IJL	2K x 8	128 x 8	
IM80C35	CPL	CJL	IPL	IJL	NONE	64 x 8	
IM80C39	CPL	CJL	IPLVZ	IJL .	NONE	128 x 8	



# IM80C48/49/35/39



# **ABSOLUTE MAXIMUM RATINGS**

Voltage on Any Pin(VSS-0.3V) to (VCC+0.3V)
Supply Voltage(VCC - VSS) +8V
Storage Temperature (Plastic)65°C to +150°C

Operating Temperature Range:	
IM80CXXCXL 0°C to	+70°C
IM80CXXIXL40°C to	+85°C
Lead Temperature (Soldering, 10sec)	300°C

consumption while retaining rapid response time to an

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# DC CHARACTERISTICS

Test Conditions:  $V_{CC} = 5V \pm 10\%$   $V_{SS} = 0V$ ,  $T_A = -40$ °C to +85°C

	PLICATIONS		TEST CONDITIONS			MI orlT		
SYMBOL	PARAMETER	1			MIN	TYP	MAX	MUNITOR
VIL	Input Low Voltage (All Except XTAL1)			ni eiden tmet pro	-0.3	es it partic	0.8	BMI ont t
V <sub>IL1</sub>	Input Low Voltage XTAL1		.enotk	unelni n	Wod DA	prinub. NAA	V <sub>CC</sub> - 0.8	sokup of
VIH	Input High Voltage (All Except RESET, XTAL1, V <sub>DD</sub> /STOP)				V <sub>CC</sub> -2V	TAMHO	Vcc	V
V <sub>IH1</sub>	Input High Voltage RESET, XTAL1, XTAL2, VDD/STOP			10.0	V <sub>CC</sub> - 0.5V		Vcc	٧
VOL	Output Low Voltage	I <sub>OL</sub> = 2	mA		TA STORY		0.45	V
Voн	Output High Voltage BUS, RD, WR, PSEN, ALE	I <sub>OH</sub> = -	-100μΑ	1419-04	2.4	Ob		٧
V <sub>OH1</sub>	Output High Voltage All Other Outputs	t <sub>OH</sub> = -	-50μA	910/14	2.4	9.19		٧
l <sub>ILP</sub>	Input Pullup Current Port 1, Port 2	V <sub>IN</sub> ≤ V	IL <sup>(9)</sup>	CAL -		-150	-300	μΑ
I <sub>IL</sub>	Input Pullup Current SS, RESET	V <sub>IN</sub> ≤ V	IL <sup>S</sup>	313	jq	-20	-40	μА
I <sub>IL</sub>	Input Leakage Current T1, EA, INT	V <sub>SS</sub> ≤ \	/cc			0	±1	μΑ
loL	Output Leakage Current Bus, TO-High Impedance	V <sub>SS</sub> ≤ \	V <sub>IN</sub> ≤ V <sub>CC</sub>		reig promp	0	±1	μΑ
lcc	Total Supply Current	T <sub>A</sub> = 25	5°C, 6MHz	G-190-1	- 109-10- 10	3	8 TANK	mA
loc1	IDLE Power Supply Current	6MHz				0.8	2.0	mA
ICC2	STandBY and STOP Modes Supply Current	V <sub>IN</sub> = V	'cc		8	1	20	μΑ

# AC CHARACTERISTICS PORT 2 TIMING

Test Conditions: V<sub>CC</sub> = 5V±10% V<sub>SS</sub> = 0V, T<sub>A</sub> = -40°C to +85°C, f<sub>CLK</sub> = 6MHz

SYMBOL	ALCOHOL OF THE DAD AMETER OF THE	TEST CONDI					
	PARAMETER	(Note 1	)	MIN	TYP	MAX	UNIT
t <sub>CP</sub>	Port Control Setup Before Falling Edge of PROG	All SHARKS	2	110		0 W327	nS
tpc	Port Control Hold after Falling Edge of PROG			140		1 to 100mm	nS
tpR	PROG to Time Port 2 Input Data must be valid	[11004] [1	thon	208 937306	1	810	nS
tpp	Output Data Setup Time	40000		220		6	ns
tpD	Output Data Hold Time	44		65			ns
tpF	Input Data Hold Time	16-35 34-	VAR-IS	0		150	ns
tpp	PROG Pulse Width			1200			ns
tpL NIC	Port 2 I/O Data Setup	missoni@ to	nostanu	350	171		ns
t <sub>LP</sub> moits	Port 2 I/O Data Hold			150			ns

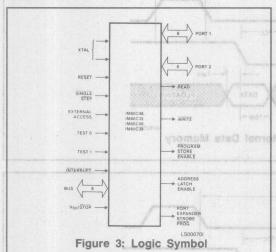
Note 1: Inputs are driven to 0.45V and 2.4V. Output timing measurements are made at 0.8V and 2.0V.

# READ, WRITE AND INSTRUCTION FETCH - EXTERNAL DATA AND PROGRAM MEMORY

Test Conditions: VCC = 5V±10% VSS = 0V, TA = -40°C to +85°C, fCLK = 6MHz

	_/_ \	TEST CONDITIONS					
SYMBOL	PARAMETER	(Note 1)	MIN	TYP	MAX	UNIT	
. t <sub>LL</sub>	ALE Pulse Width		400		BALLET !	ns	
t <sub>AL</sub>	Address Setup before ALE Falling	energy and	120			ns	
tLA	Address Hold from ALE Falling	PEDAGE-PE	80		ME IN EL	ns	
tcc	Control Pulse Width (PSEN, RD, WR)	ACCOUNTS OF THE PARTY OF	700			ns	
t <sub>DW</sub>	Data Setup before WR Rising	Attention of the	500			ns	
two	Data Hold after WR Rising	C <sub>L</sub> = 20pF	120			ns	
tcy	Cycle Time		2.5		150	μs	
tDR	Data Hold Wesspaw		0		200	ns	
t <sub>RD</sub>	PSEN, RD to Data in Valid	and mort been in	TUDIT		500	ns	
t <sub>AW</sub>	Address Setup before WR		230			ns	
t <sub>AD</sub>	Address Setup before Data in				950	ns	
tAFC	Address Float to RD, PSEN		0			ns	

Note 1: For Control Outputs  $C_L = 80pF$ , for Bus Outputs  $C_L = 150pF$ . Inputs are driven to 0.45V and 2.4V. Output timing measurements are made at 0.8V and 2.0V.



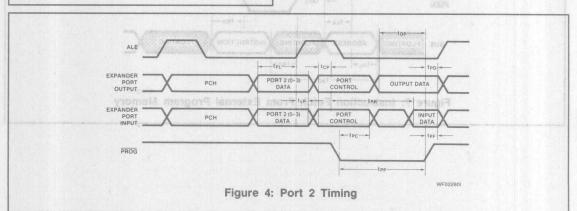
# ROM CODE DATA ENTRY

Intersil can accept customer ROM codes in a variety of media, including standard byte-wide EPROMs (2176, 2732, 2764, 27C16, 27C32, etc.) or (8048, 8748, 8049, 8749) microcomputers.

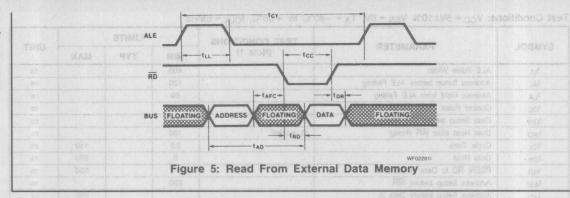
Contact GE-Intersil sales office for other formats.

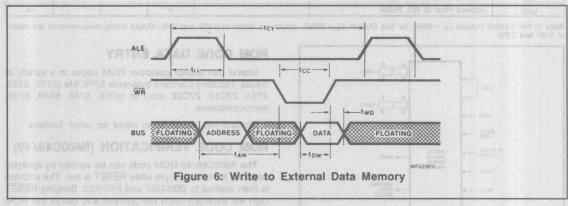
# **ROM CODE VERIFICATION (IM80C48/49)**

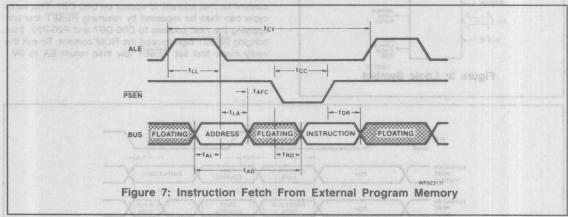
The IM80C48/49 ROM code can be verified by applying negative 5V to the EA pin while RESET is low. The address is then applied to DB0-DB7 and P20-P22. Bringing RESET high will internally latch the address and cause the ROM content for that address to appear on DB0-DB7. This verify cycle can then be repeated by returning RESET low and applying the next address to DB0-DB7 and P20-P22; then bringing RESET high to read the ROM content. To exit the verify mode first set RESET low then return EA to 0V.











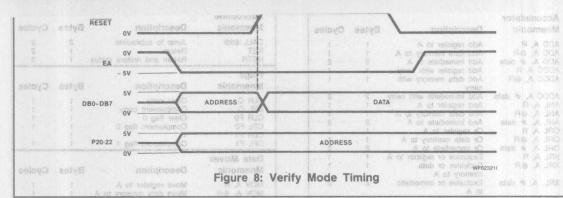


Table 1: Pin Description

PIN NAME	PIN	et etsiberuni evolv ateb 4 R VOM helFUNCTION ot stalbarreri evolvi ateb 4 R a VOM
ТО	1 1038	An input pin that is tested by the conditional jump instructions JT0 and JNT0. This pin can be designated as a clock output using the ENT0 CLK instruction.
XTAL1	e 2	used as the external clock input when
XTAL2	3 a a	Connected to one side of the crystal when using the internal oscillator. Leave open when using an external oscillator.
RESET	4	Active low input used to reset the microcomputer. A capacitor from this pin to ground will automatically reset the device on power-up.
SS Salaro	, 5	Single-Step input, active low, that can be used in conjunction with ALE to single-step the processor through each instruction.
INT	f 6 jaur	INTerrupt input, active low. Initiates an interrupt if external interrupt is enabled.
EA	7 0	External Access input, active high, is used to force all program memory accesses to reference external memory.
RD	8	This output, active low, is used by external devices to place data onto the bus during a bus read operation.
PSEN	9	Program Store ENable. This output, active low, occurs only during fetches to external program memory. The system uses this signal to strobe external program memory.

PIN	PIN	A taulou la FUNCTION A AG
WR	10	This output, active low, is used to strobe data into external devices during a bus write operation.
ALE seloyD e	11 11/3	Address Latch Enable. This output active high, occurs once during each cycle. The falling edge of this timing signal is used to strobe the address bits appearing on the data bus.
DB0 - DB7 (Bus)	12 – 19	Data Bus. These eight lines form a true bidirectional port which can store data as a latched output port or serve as a non-latching input/output port.
Vss	20	Circuit GND potential.
P20 – P27	21 - 24 35 - 38	Port 2. Identical to Port 1 except that P20 – P23 contain the four high-order program counter bits during external program memory fetches. If IM82C43 I/O Expanders are being used in the system, they communicate with the IM80C48 through these four lines.
PROG	25	Output strobe for IM82C43, I/O Expander.
V <sub>DD</sub> / STOP	26	Used to select low power hardware STOP mode.
P10 – P17	27 – 34	Port 1. An 8-bit quasi-bidirectional port. The I/O structure on these eight lines allows each to be used separately as an input or output.
T18	39	An input pin tested by the conditional jump instructions, JT1 and JNT1. The pin can also be programmed as the input to the counter.
V <sub>DD</sub>	40	Main power supply.

# IM80C48/49/35/39



Table 2. Instruction Set by Mnemonic

Accumulator	Description	Dest	0
Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add register to A Add data memory to A Add immediate to A Add register with carry Add data memory with	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry Add immediate with carry Add immediate with carry And register to A And data memory to A And immediate to A Or register to A Or immediate to A Or immediate to A Exclusive or register to A Exclusive or data memory to A	1	1
	carry		
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	-1	1
ORL A, @R	Or data memory to A	1	and a
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data	1	1
	Exclusive or data memory to A Exclusive or immediate to A		
XRL, A, # data	Exclusive or immediate	2	2
	to A		
INC A	Increment A	1	1
DEC A	Decrement A	1	nonqha
CLR A	Increment A Decrement A Clear A Complement A Decimal adjust A Swap nibbles of A Rotate A left through	1	1
CPL A	Complement A	1	MIS!
DA A	Decimal adjust A	9 1	Carlotte and Carlotte
SWAP A	Swap nibbles of A	1	3660年
RL A	Rotate A left Rotate A left through	1	1
		1	1
external device	Rotate A right through		
RR A moderage	Rotate A right	1	1
RRC A	Hotate A fight through	1	1
control Tels output	carry		9.14
Input/Output			
		Bytes	Cycles
	of Page of Intents		
IN A, P	input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	20
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	input expander port to A	1	2 2
MOVD P, A	Input port to A Output A to port And immediate to port Or immediate to port Input BUS to A Output A to BUS And immediate to BUS Or immediate to BUS Input expander port to A Output A to expander port		2
ANID D A 109	port	25	2
ODID P A	port And A to expander port Or A to expander port	HE.	2
		1491	2
Billianiania	Description	Bytes	Cycles
	rs angunsox divi		
INC R	increment register	1	1
DEC B	Increment data memory	1	
DEC N	Decrement register	1	-
Branch			
Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2 2
DJNZ R, addr	Jump indirect Decrement register and	2	2
not be an in the last to	skip	50	-019
JC addr	skip Jump on carry = 1 Jump on carry = 0 Jump on Z zero	2	
		2	2
JZ addr	Jump on Z zero	2	2
The state of the s	Jump on A not zero	2	2
JNZ addr	Jump on T0 = 1	2	2
JNZ addr JT0 addr		2	2
JNZ addr JT0 addr JNT0 addr	Jump on TO = 0		
JNZ addr JT0 addr JNT0 addr JT1 addr	Jump on T0 = 0  Jump on T1 = 1	2	2
JNZ addr JT0 addr JNT0 addr JT1 addr JNT1 addr	Jump on T0 = 0 Jump on T1 = 1 Jump on T1 = 0	2	2 2
JNZ addr JTO addr JNTO addr JT1 addr JNT1 addr JFO addr	Jump on T0 = 0 Jump on T1 = 1 Jump on T1 = 0 Jump on F0 = 1	2 2 2	2
JNZ addr JTO addr JNTO addr JT1 addr JNT1 addr JFO addr JFO addr	Jump on T0 = 0 Jump on T1 = 1 Jump on T1 = 0 Jump on F0 = 1 Jump on F1 = 1	2 2 2 2	2 2
JNZ addr JTO addr JNTO addr JT1 addr JNT1 addr JF0 addr JF1 addr JTF addr	Jump on T0 = 0 Jump on T1 = 1 Jump on T1 = 0 Jump on F0 = 1 Jump on F1 = 1 Jump on timer flag	2 2 2 2 2	2 2 2
JNC addr JZ addr JTO addr JNTO addr JT1 addr JNT1 addr JFO addr JF1 addr JF5 addr JF6 addr JF6 addr JF6 addr	Jump on F1 = 1 Jump on timer flag	2 2 2 2 2 2	2 2

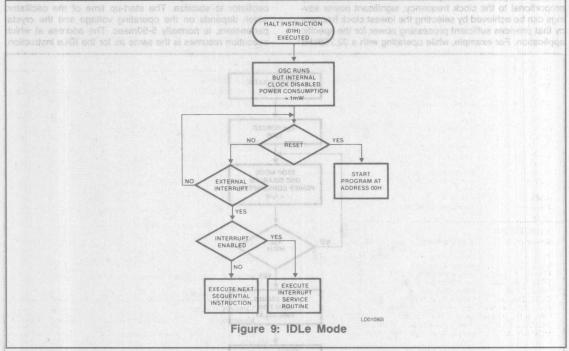
Table 2. Instruction Set by Mnemonic (Cont.)

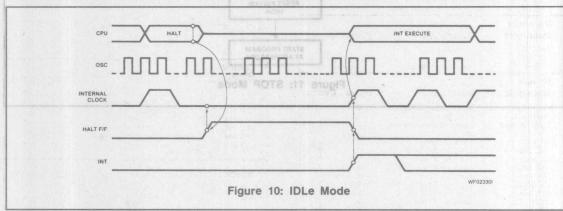
Subroutine Mnemonic	Description	Bytes	Cycles
This continue and the continue	metersuspersonnen AD		
CALL addr	Jump to subroutine	2	2
RET RETR	Return and restore status	1	2 2
	Hetuit and restore status		~
Flags			
Mnemonic	Description	Bytes	Cycles
CLR Canada	Clear carry	1	1
CPL C CLR F0	Complement carry	1	1
CLR F0 CPL F0	Clear flag 0	1	1
CLR F1	Complement flag 0	1	
CPL F1	Complement flag 1	1	1
Data Moves	All the same of th		
Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A. @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move register to A Move data memory to A Move immediate to A Move A to register	1	1
MOV @H, A	Move A to data memory	1	1
MOV R # data	Move immediate to	2	2
MOV @R. # data	register Move immediate to data		HAA2
	memory		P.CO.
MOV A, PSW	memory Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory		1
XCHD A, @R	Exchange nibble of A and register	1	1
	Move external data memory to A	1 .	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current	1	2
MOVP3 A, @A	page Move to A from page 3	1	5 1/2 X
Timer/Counter	thin Binth Halle.		
Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOVETA	Load timer/counter	1	TOPIN
STRT T	Start timer	1	1
STRT CNT STOP TCNT	Start counter Stop timer/counter	1	1
EN TONTI	Enable timer/counter	1	1
	interrupt		-754
DIS TCNTI	Disable timer/counter interrupt	1	1
THE RESERVE OF THE PARTY OF THE	arti deta-espoia	100	
Mnemonic	Description		Cycles
EN I	Enable external interrupt	1	1/4
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL MBO	Select memory bank 1	1	1
SEL MB1	Select register bank 0 Select register bank 1 Select memory bank 0 Select memory bank 1	1	143
ENTO CLK	Enable clock output on	1	i
Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	UR
IDL SO SOSIO	Low power Mode, OSC.	1	1
- HUNGERING OFFICE	on Low power Mode, OSC.	1	-1.
STBY			F 274 134

# LOW POWER MODES

The Intersil IM80C48 family incorporates IDLE and STandBY instructions as well as the hardware STOP mode. The IDLE instruction, opcode 01H, operates as shown in Figure 1. Execution of opcode 01H disables the internal clock and timing circuits while leaving the oscillator running.

Power consumption drops to less than 1mW. Either a RESET or external INTerrupt will terminate the IDLE mode. A RESET will start execution from address 00H. An external INTerrupt will start execution from 03H if INTerrupt is enabled, or start execution from the next sequential instruction following the IDLE instruction if the INTerrupt is disabled.



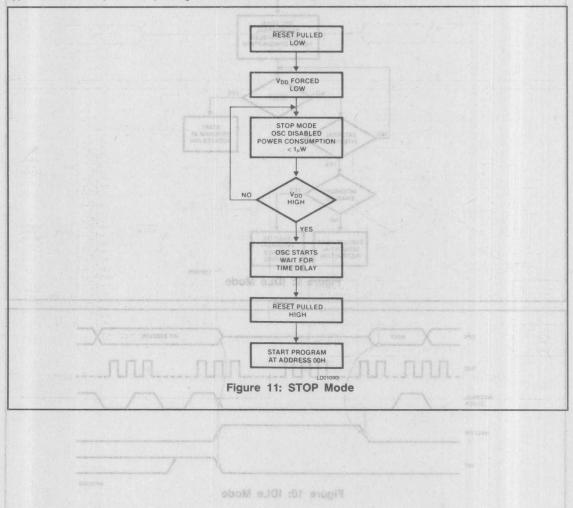


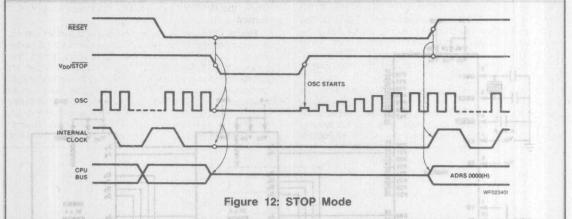
mode, first take RESET low, then pull V<sub>DD</sub>/ STOP low. The STOP mode, like the STandBY mode, shuts down the oscillator and causes the device to draws less than  $1\mu A$  of current. To exit the STOP mode, take V<sub>DD</sub>/ STOP high, wait for the oscillator to stabilize, then pull RESET high. Execution starts at address 0000H.

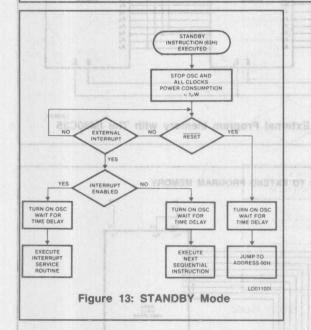
Since the power consumption of the IM80C48 is directly proportional to the clock frequency, significant power savings can be achieved by selecting the lowest clock frequency that provides sufficient processing power for the specific application. For example, while operating with a 32.768kHz

current.

Figure 13 shows the operation of the STandBY instruction, opcode 63H. This instruction is similar to IDLE except that the oscillator is also turned off, reducing current drain to less than  $1\mu A$ . A RESET or INTerrupt will restart the oscillator and execution will resume after the oscillator startup time, plus a delay of 2-3 instruction cycles that allows the oscillator to stabilize. The start-up time of the oscillator, which depends on the operating voltage and the crystal parameters, is normally 5-50msec. The address at which execution resumes is the same as for the IDLe instruction.







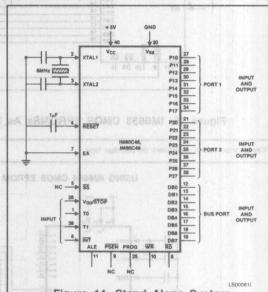
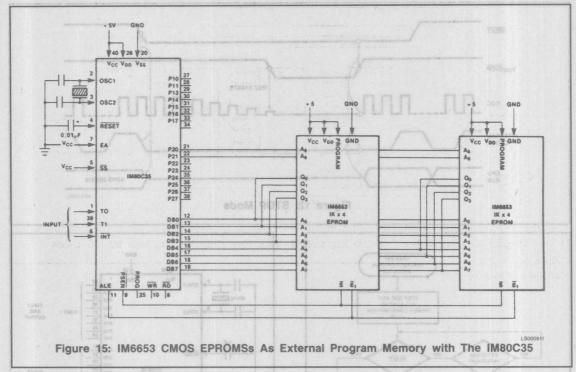
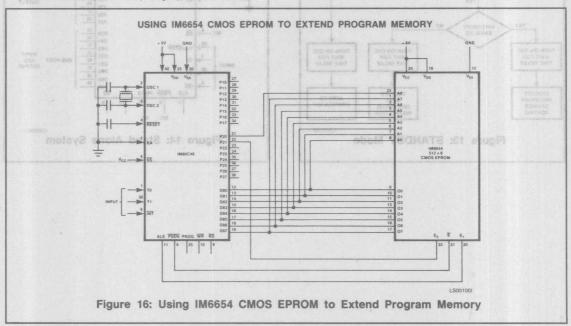


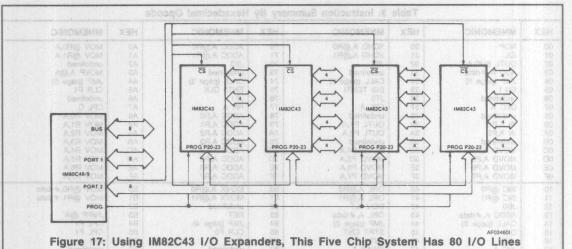
Figure 14: Stand Alone System

Figure 18: Using IM6654 CMOS EPROM to Extend Program Memory



\*Capacitance values dependent on package type





\*Capacitance values dependent on package type Biblius St. EIO All St. A. IRD BIBLIUM BIBLION BIBLIUM BIBLION BIBLIUM BIBLION BIBLION BIBLIUM BIBLION BIBLION BIBLIUM BIBLION BIBLIUM BIBLION BIBLIUM B

00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E	NOP IDL OUTL BUS,A ADD A,# data JMP (page 0) EN I undefined DEC A undefined IN. A,P1 IN A,P2 undefined MOVD A,P4 MOVD A,P5 MOVD A,P6 MOVD A,P7	30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F	XCHD A,@R0 XCHD A,@R1 JB1 undefined CALL (page 1) DIS TCNTI JT0 CPL A undefined OUTL P1,A OUTL P2,A undefined MOVD P4,A MOVD P4,A MOVD P6,A MOVD P7,A	70 71 72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F	ADDC A,@R0 ADDC A,@R1 JB3 undefined CALL (page 3) ENTO CLK JF1 RR A ADDC A,R0 ADDC A,R1 ADDC A,R2 ADDC A,R3 ADDC A,R3 ADDC A,R4 ADDC A,R4 ADDC A,R5 ADDC A,R6 ADDC A,R6 ADDC A,R6 ADDC A,R6 ADDC A,R7	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE	MOV @RO.A MOV @RO.A Undefined MOVP A.@A JMP (page 5) CLR F1 Undefined CPL C MOV RO.A MOV R1.A MOV R2.A MOV R3.A MOV R4.A MOV R5.A MOV R5.A MOV R7.A
10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	INC @R0 INC @R1 JB0 ADDC A, # data CALL (page 0) DIS I JFT INC A INC R0 INC R1 INC R2 INC R3 INC R4 INC R5 INC R6 INC R6 INC R7	40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F	ORL A,@R0 ORL A,@R1 MOV A,T ORL A, # data JMP (page 2) STRT CNT JNT1 SWAP A ORL A,R0 ORL A,R1 ORL A,R3 ORL A,R4 ORL A,R4 ORL A,R4 ORL A,R6 ORL A,R6 ORL A,R7	80 81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F	MOVX A,@R0 MOVX A,@R1 undefined RET JMP (page 4) CLR F0 JNI undefined ORL BUS,#data ORL P1,#data ORL P2,#data undefined ORLD P4,A ORLD P5,A ORLD P6,A ORLD P7,A	B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF	MOV @R0,#data MOV @R1,#data JB5 JB6 JMPP @A CPL F1 CPL F1 JF0 undefined MOV R0,#data MOV R1,#data MOV R2,#data MOV R3,#data MOV R3,#data MOV R4,#data MOV R5,#data MOV R6,#data MOV R7,#data
20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F	XCH A,@R0 XCH A,@R1 undefined MOV A,#data JMP (page 1) EN TCNTI JNT0 CLR A XCH A,R0 XCH A,R1 XCH A,R2 XCH A,R3 XCH A,R4 XCH A,R5 XCH A,R5 XCH A,R6 XCH A,R6 XCH A,R6 XCH A,R7	50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F	ANL A,@R0 ANL A,@R1 JB2 ANL A,# data CALL (page 2) STRT T JT 1 DA A ANL A,R0 ANL A,R1 ANL A,R2 ANL A,R3 ANL A,R4 ANL A,R5 ANL A,R6 ANL A,R6 ANL A,R7	C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CC	undefined undefined undefined undefined JMP (page 6) SEL RB0 JZ MOV A,PSW DEC R0 DEC R1 DEC R2 DEC R3 DEC R3 DEC R4 DEC R5 DEC R6 DEC R6 DEC R6	E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 EA EB EC ED EE EE	undefined undefined MOVP3 A,@A JMP (page 7) SEL MB0 JNC RL A DJNZ R0,addr DJNZ R1,addr DJNZ R3,addr DJNZ R3,addr DJNZ R4,addr DJNZ R5,addr DJNZ R6,addr DJNZ R6,addr DJNZ R7,addr
60 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D 6E 6F	ADD A,@R0 ADD A,@R1 MOV T,A STBY JMP (page 3) STOP TCNT undefined RRC A ADD A,R0 ADD A,R1 ADD A,R2 ADD A,R3 ADD A,R4 ADD A,R5 ADD A,R6 ADD A,R6 ADD A,R6 ADD A,R7	90 91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F	MOVX @R0,A MOVX @R1,A JB4 RETR CALL (page 4) CPL F0 JNZ CLR C ANL BUS,#data ANL P1,#data ANL P2,#data undefined ANLD P4,A ANLD P5,A ANLD P5,A ANLD P7,A	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC DD DD DE	XRL A,@R0 XRL A,@R1 JB6 XRL A, # data CALL (page 6) SEL RB1 undefined MOV PSW,A XRL A,R0 XRL A,R1 XRL A,R3 XRL A,R3 XRL A,R3 XRL A,R4 XRL A,R6 XRL A,R6 XRL A,R6 XRL A,R6 XRL A,R6 XRL A,R6 XRL A,R6	F0 F1 F2 F3 F4 F5 F6 F7 F8 FP FA FB FC FD FE FF	MOV A,@R0 MOV A,@R1 JB7 undefined CALL (page 7) SEL MB1 JC RLC A MOV A,R0 MOV A,R1 MOV A,R1 MOV A,R2 MOV A,R3 MOV A,R4 MOV A,R4 MOV A,R5 MOV A,R6 MOV A,R7

# DESCRIPTION

The Intersil IM82C43 is a CMOS input/output expander equivalent to the NMOS 8243. It is designed to provide I/O expansion for the CMOS IM80C48 and NMOS 8048 families of single-chip microcomputers.

The 24-pin IM82C43 provides four 4-bit bidirectional I/O ports: 8048/41 instructions control bidirectional transfers between theIM82C43 and the 8048 family microcomputers, and can execute logical AND/OR operations directly on the data contained in the IM82C43 ports. Paddisconor pade 600 = 4T) ROLLERS TO ARAMO JACKS TO SELECTION OF THE PROPERTY OF THE PRO

#### **FEATURES**

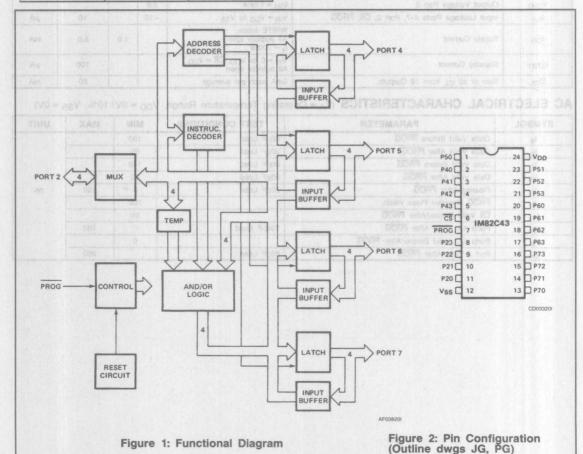
- 8048/41 Compatible I/O Expander
- CMOS Pin-For-Pin Replacement for Standard **NMOS 8243**
- Low Power Dissipation Maximum 25mW Active

COMITAN MUMAAM STURIOR

- Four 4-Bit I/O Ports in 24-Pin DIP
- Logical AND/OR Directly to Ports
- **High Output Drive**
- Single +5V Supply OAAAAO AAOLATO

# ORDERING INFORMATION

	PART NO.	TEMP. RANGE	PACKAGE
T	IM82C43CJG	0°C to +70°C	24 PIN CERDIP
T	IM82C43CPG	0°C to +70°C	24 PIN PLASTIC
-	IM82C43IJG	-40°C to +85°C	24 PIN CERDIP
-	IM82C43IPG	-40°C to +85°C	24 PIN PLASTIC



9-45

# IM82C43



# **ABSOLUTE MAXIMUM RATINGS**

upply Voltage (VDD - VSS)+8	3V
oltage on Any Pin(VSS-0.5V) to (VDD+0.5	V)
ower Dissipation	W
perating Temperature (C) 0°C to +70°	C
(I)40°C to +85°	°C

Storage Temperature		65°C	to +150°C
Lead Temperature (Soldering,	10sec)	PROPERTY.	300°C
CMCS Input/output expender			

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

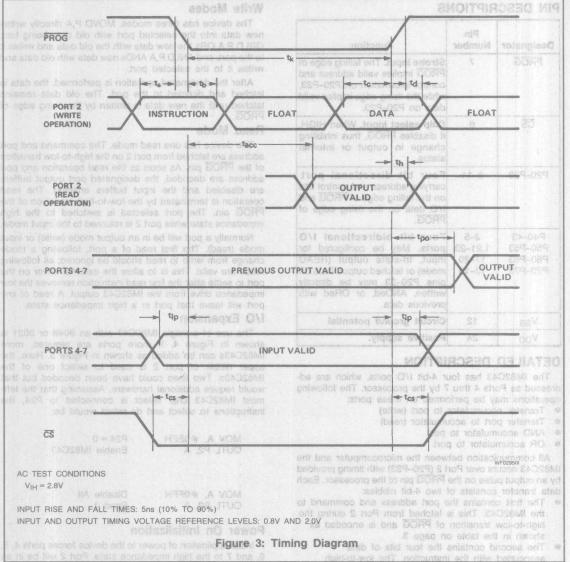
# ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (TA = Operating Temperature Range, VDD=5V±10%, VSS = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIL	Input Low Voltage	professional and a second seco	-0.5	and the second	0.8	
		V <sub>DD</sub> = 4.5	2.0	CHAIT	1.094	BAS
VIH	Input High Voltage	V <sub>DD</sub> = 5.5 0 30 MIG AS 1 00	2.4	10°0	DUDGE	IMBR
	Output Low Voltage Ports 4-7	I <sub>OL</sub> = 10mA	235	Con	0.4	V
VOL Output Low Vol		I <sub>OL</sub> = 20mA			0.8	
	Output Low Voltage Port 2	I <sub>OL</sub> = 1.6mA	1 0	D*0h-	0.4	SBM
V <sub>OH1</sub>	Output High Voltage Ports 4-7	I <sub>OH</sub> = 3.2mA	2.8	0°04-	D438PG	SEMI
V <sub>OH2</sub>	Output Voltage Port 2	I <sub>OH</sub> = 1.6mA	2.8			-14-0000-0-0-0
IILK	Input Leakage Ports 4-7, Port 2, CS, PROG	V <sub>IN</sub> = V <sub>DD</sub> to V <sub>SS</sub>	-10		10	μΑ
I <sub>DD</sub>	Supply Current	WRITE mode, All outputs open, t <sub>k</sub> = 700ns		1.6	5.0	mA
ISTBY	Standby Current	V <sub>IN</sub> = 0 or V <sub>DD</sub> , $\overline{CS}$ = V <sub>DD</sub> , All outputs open			100	μΑ
ΣloL	Sum of all ICI from 16 Outputs	5mA each pin average	51.55		80	mA

# AC ELECTRICAL CHARACTERISTICS (TA = Operating Temperature Range, VDD = 5V±10%, VSS = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ta	Code Valid Before PROG	80pF Load	100		
tb	Code Valid After PROG	20pF Load	60	em to	
tc	Data Valid Before PROG	80pF Load	140		
td	Data Valid After PROG	20pF Load	20	11 1/ 3	PERTE
th	Floating After PROG	20pF Load	0	150	ns
tk	PROG Negative Pulse Width		700		
tcs	CS Valid Before/After PROG		50	THE L	
tpo	Ports 4-7 Valid After PROG	100pF Load		700	HAI
t <sub>lp</sub>	Ports 4-7 Valid Before/After PROG		0		
tacc	Port 2 Valid After PROG	80pF Load		650	



transition of PROG indicates the presence of Port Address And Command Portman

			WSTRUCTION!		
C008	920	129	3000	P22:	88.9
Post 4			Flead	0	0
		0	. ethW-	1	0
	. 0				1
	1				

Designator	Pin Number	Function
PROG	7	Strobe input. The falling edge of PROG implies valid address and control information on P20–P23, while the rising edge implies valid data on P20–P23.
CS	6	Chip select input. When HIGH, it disables PROG, thus inhibiting change in output or internal status.
P20-P23	8–11	Four bit directional port carrying address and control bits on the falling edge of PROG and I/O data on the rising edge of PROG.
P40–43 P50–P53 P60–P63 P70–P73	2–5 1,21–23 17–20 13–16	Four bit bidirectional I/O ports. May be configured for input, tri-state output (READ mode) or latched output. Data on pins P20–23 may be directly written. ANDed, or ORed with previous data.
Vss	12	Circuit ground potential
V <sub>DD</sub>	24	Positive supply.

# **DETAILED DESCRIPTION**

The IM82C43 has four 4-bit I/O ports, which are addressed as Ports 4 thru 7 by the processor. The following operations may be performed on these ports:

- Transfer accumulator to port (write)
- Transfer port to accumulator (read)
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer and the IM82C43 occurs over Port 2 (P20–P23) with timing provided by an output pulse on the PROG pin of the processor. Each data transfer consists of two 4-bit nibbles:

- The first contains the port address and command to the IM82C43. This is latched from Port 2 during the high-to-low transition of PROG and is encoded as shown in the table on page 3.
- The second contains the four bits of data associated with the instruction. The low-to-high transition of PROG indicates the presence of data.

### Port Address And Command Format

P23	P22	INSTRUCTION CODE	P21	P20	ADDRESS CODE
0	0	Read	0	0	Port 4
0	1	Write	0	1	Port 5
1	0	ORLD	1	0	Port 6
1	1	ANLD	1	1	Port 7

new data into the selected port with old data being lost; ORLD P,A ORs the new data with the old data and writes it to the port; and ANLD P,A ANDs new data with old data and writes it to the selected port.

After the designated operation is performed, the data is latched and directed to the port. The old data remains latched until the new data is written by the rising edge of PROG.

# Read Mode

The device has one read mode. The command and port address are latched from port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the designated port output buffers are disabled and the input buffers enabled. The read operation is terminated by the low-to-high transition of the PROG pin. The port selected is switched to the high impedance state while port 2 is returned to the input mode.

Normally a port will be in an output mode (write) or input mode (read). The first read of a port, following a mode change from write to read should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the IM82C43 output. A read of any port will leave that port in a high impedance state.

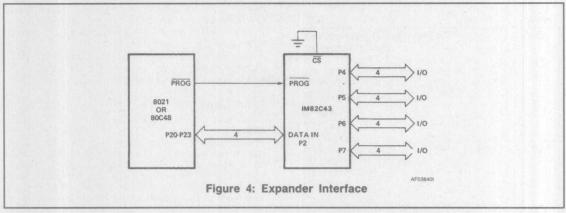
# I/O Expansion

The use of a single IM82C43 with an 8048 or 8021 is shown in Figure 4. If more ports are required, more IM82C43s can be added as shown in Figure 5. Here, the upper nibble of port 2 is used to select one of the IM82C43s. Two lines could have been decoded but that would require additional hardware. Assuming that the leftmost IM82C43 chip select is connected to P24, the instructions to select and de-select would be:

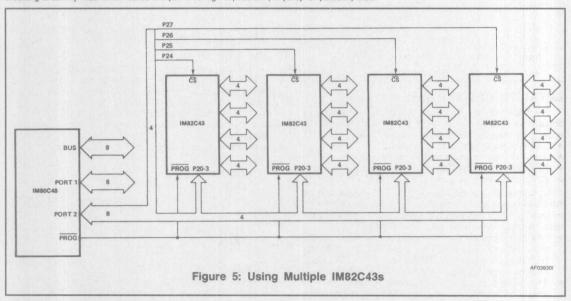
MOV A, #0EFH	P24 = 0
OUTL P2, A	Enable IM82C43
MOV A, #0FFH	Disable All
OUTL P2. A	Send it

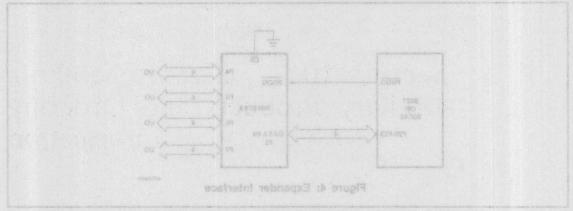
#### Power On Initialization

Initial application of power to the device forces ports 4, 5, 6, and 7 to the high impedance state. Port 2 will be in an input state if PROG or CS are high when power is applied. The first high-to-low transition of PROG causes the device to exit the power-on mode. The power-on sequence is initiated if VDD drops below one volt.

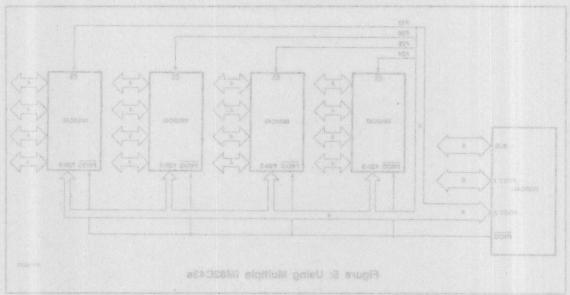


Note: The IM82C43 does not have the same quasi-bidirectional port structure as P1/P2 of the 8048. When a "1" is written to P4-7 of the IM82C43 it is a "hard 1" (low impedance to +5V) which cannot be pulled low by an external device. All 4 bits of any port can be switched from output mode to input mode by executing a dummy read which leaves the port in a high impedance (no pullup or pulldown) state.





Note: The IMSC43 does not have the same quasi-advectored pair structure as PT/P2 of the 9048. When a "1" is written to 457 which cannot be paired to by an extend device. All 4 bits of any portican be awarened to 457 which teached be paired to by an extend device. All 4 bits of any portican be switched from output mode to input mode by accounting a studiery read which teaches the port in a high impedance the pullup or publishers state.



Section 10 — High Reliability/ Military Products and Ordering Information Section 10 - High Reliability/ Military Products and Ordering Information

# DIE & WAFER ORDERING INFORMATION



# FET, MOSFET, AND DUAL TRANSISTOR CHIPS

### INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need, Intersil offers a full line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is due to the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy for dice as it can for packaged devices. This is due to equipment limitations and handling problems.

# PURCHASE OPTIONS

Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, scribed, and mounted on rings with adhesive tape.
- Wafers which have been electrically probed, inked, and visually inspected only.

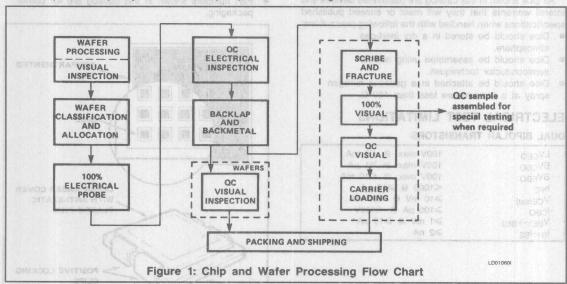
# **GENERAL PHYSICAL INFORMATION**

 Consult individual product information sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.

- Dice are 100% tested to D.C, +25°C electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

# Small Signal Devices Company of the Day of t

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003" to .006".
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general, dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.



# DIE & WAFER ORDERING INFORMATION



# RECOMMENDED DICE ASSEMBLY **PROCEDURE**

#### CLEANING

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is to boil the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

#### DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385°C and 400°C with eutectic visible on three sides of the die after attachment. · Chips are available

# BONDING: laubivibril sea) constatol auto ancianomib

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

#### HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430°C.

# **ELECTRICAL TEST LIMITATIONS**

# **DUAL BIPOLAR TRANSISTORS**

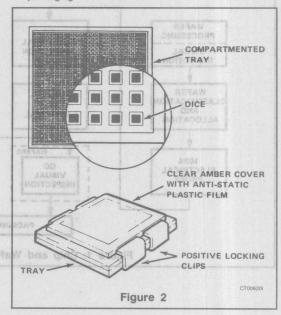
LVCEO	100V max. @ ≤1 mA
BVCBO	100V max. @ ≥1 μA
BVEBO	100V max. @ ≤10 mA
hFE	≤1000 @ ≥10 µA
V <sub>CE(sat)</sub>	≥10 mV @ ≤10 mA
ICBO	≥100 pA @ ≤100V
V <sub>BE1</sub> -V <sub>BE2</sub>	≥1 mV @ ≥10 µA
IB1-IB2	≥2 nA

# MOSFET, AND DUALSTEE

Breakdown voltage	100V max. @ 1 μA
Pinch-off voltage	0–20V @ ≥ 1nA
V <sub>GS(th)</sub>	0-5 @ ≥ 10 µA
orfDS(on) learning hee	
IDSS oils of atotals	100mA max.
	20,000 μMHOS max.
ID(off), Is(off), IGSS	100pA min.
VGS1-VGS2	5mV min.
Electrical testing is parameters such a	guaranteed to a 10% LTPD. AC s capitance and switching time

# STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.

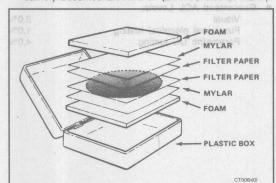


# DIE & WAFER ORDERING INFORMATION



## OPTIONAL WAFER PACKAGE

- 100% electrically probed rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package replace "D" in catalog number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).



NOTE: Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

Figure 3

# **ELECTRICAL TEST CAPABILITY**

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

ELECTRICAL TEST SPEC.	2N4391 IN A TO-18	2N4391 CHIP
IGSS @ 25C	100pA max.	100pA max.
BVGSS	40V min.	40V min.
I <sub>D</sub> (off) @ 25C	100pA max.	100pA max.
V <sub>GS</sub> (forward)	See note 1	1V max.
VGS(off) or VP	4V to 10V	4V to 10V
IDSS	50 to 150mA	50 to 150mA
V <sub>DS</sub> (on)	0.4V max.	0.4 max.
r <sub>DS</sub> (on)	30Ω max.	30Ω max.
Ciss	14pF max.	Guaranteed by Design
C <sub>rss</sub>	3.5pF max.	Guaranteed by Design
t <sub>d</sub>	15ns max.	Guaranteed by Design
t <sub>r</sub>	5ns max.	Guaranteed by Design
toff	20ns max.	Guaranteed by Design
tf	15ns max.	Guaranteed by Design

NOTE 1. This parameter is very dependent upon quality of metalization to which chip is attached.

## SUMMARY

Of the 14 items specified for the package part, only 8 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is twofold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe testing can be performed on the packaged devices per individual customer needs. When testing is required other than that called out in the data sheet, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown as follows:

# FET & DUAL FET PAIRS

- 1. Leakages to 1 pA (IGSS)
- 2. Rps(on) to as low as 3 ohms
- 3. ID(off) to 10 pA
- 4. IDSS to 1 amp (pulsed)
- gfs to 20,000 µmho
- 6. gos to 1 µmho
  - en noise to 5 nV/VHz at frequencies of 10Hz to 100Hz
- 8. CMRR to 100dB
- $\Delta (V_{GS1}-V_{GS2})/\Delta T$  down to  $10\mu V/^{\circ}C$  to an LTPD of 20%
- 10. gm match to 3%
- 11. IDSS match to 3%

#### TRANSISTOR PAIRS

- 1. Leakages to as low as 1pA
- Beta with collector current up to 50mA and as low as 100nA
- 3. f<sub>T</sub> up to 500MHz with collector currents in the range of 10µA to 10mA
- Noise measurements as low as 5nV/\/\Hz from 4. 10Hz to 100kHz
- 5.  $\Delta (V_{BE1} V_{BE2})/\Delta T$  to  $10\mu V/^{\circ}C$  to an LTPD of 20%

#### VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

# CMOS INTEGRATED CIRCUIT CHIPS | Design at the state of th

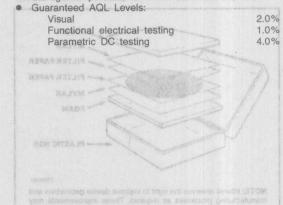
#### INTRODUCTION mot speakag in betast signes ad

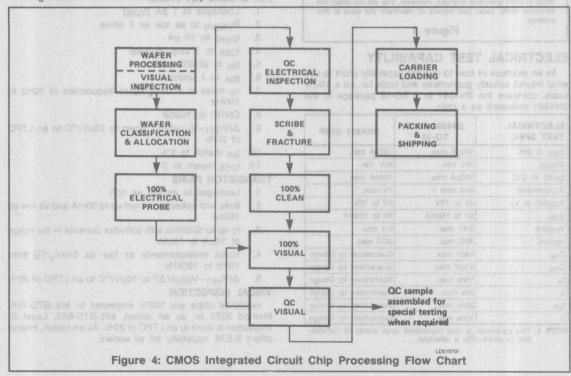
In addition to discrete device chips, Intersil also offers a full line of metal gate CMOS integrated circuits in die form. Die sales, however, present some unique problems. In many cases, chips cannot be guaranteed to the same electrical specifications as can the packaged parts. This is because leakage, noise, AC parameters and temperature testing cannot be guaranteed to the same degree of accuracy for dice as for packaged devices.

# GENERAL PHYSICAL INFORMATION

- Chips are available with precise length and width dimensions, ±2 mils in either dimension.
- Chip thickness is 9 to 20 mils, depending on device type.
- Bonding pad and interconnected material is aluminum, 10K to 15K A thick.
- Each die surface is protected by planar passivation and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by an HF etchant; bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.

- Dice are 100% tested to DC electrical specifications, at 25°C then visually inspected according to MIL-STD-883, Method 2010.2, condition B, with modifications reflecting CMOS requirements.
- Bonding pad dimensions are 4.0 x 4.0 mils minimum.
- Storage temperature is -40°C to +150°C.





#### PHUCEDURES

#### CLEANING

Dice supplied in die form do not require cleaning prior to assembly. However, if cleaning is desired, dice should be subjected to freon TF in a vapor degreaser and then vapordried.

#### RECOMMENDED HANDLING

Intersil recommends that dice be stored in the vacuumsealed plastic bags which hold the dice carriers. Once removed from the sealed bags, the dice should be stored in a dry, inert-gas atmosphere.

Extreme care should be used when handling dice. Both electrical and visual damage can occur as the result of an unclean environment or harsh handling techniques.

#### DIE ATTACH

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidization. If a eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C. If hermetic packages are used, epoxy die attach should be carried out with caution so that there will be no "outgassing" of the epoxy.

#### BONDING

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The wire should be 99.99% pure gold and the aluminum wire should be 99% aluminum/1% silicon. In either case, it is recommended that 1.0 mil wire be used for normal power circuits.

- casy to nativie, store and inventory.
- 100% electrically probed with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection dice are in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be used as storage contained for unused dice.
- Carriers hold 25, 100 or 400 dice, depending on die size and quantity ordered.
- Packing of integrated circuit dice in carriers is identical to illustration shown earlier for discrete device, except that IC chips are not available in vial packs or in wafer form.

#### CHANGES

Intersil reserves the right in improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect dice electrical limits, pad layouts, or maximum die sizes.

# USER RESPONSIBILITY

Written notification of any non-conformance by Intersil of Intersil's dice specifications must be made within 75 days of the shipment date of the die to the user. Intersil assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

### HIGH-RELIABILITY/MILITARY PRODUCTS



#### 100% INTEGRATED CIRCUIT PROCESSING

Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

#### HI-REL PROCESS OFFERINGS 38510 PRODUCTS ubong termotago ni aldang areimaO ...

Intersil holds QPL1 status on a number of JAN MIL-M-38510 products as listed herein. As required by JAN specifications, these products are fabricated, assembled, and 100% processed within the United States and are fully compliant with all the requirements, procedures, and methods as given in MIL-M-38510 Revision F and MIL-STD-883 Revision C.

#### 883B PRODUCTS

The 883B flow diagram represents product processed in accordance with Method 5004 and Method 5005 of MIL-STD-883 Rev. C, Class B. Most products listed as /883B herein are available as compliant to paragraph 1.2 of MIL-STD-883B Rev. C while others are available only as noncompliant at this time (Allowances for sale of non-compliant /883B products are covered in notice 3 of MIL-STD-883 Rev. C). Check with Intersil Customer Service as to the compliant status of individual product offerings at any point in time.

#### HR PRODUCTS

The HR flow diagram, newly offered by Intersil, represents high reliability hermetic product utilizing many, but not necessarily all, of the test methods and requirements of MIL-STD-883 Rev. C, to be used in high reliability applications where some deviations from Rev. C may be justified and economic advantages realized. Such product may not be branded /883B but may be branded /HR or a special brand as required as purchase order.

#### **BR PRODUCTS**

The BR flow diagram, newly offered by Intersil, represents hermetic or plastic encapsulated product intended for application in the computer, industrial, or hi-rel commercial marketplace. In addition to 100% burn-in, many other reliability processing steps are included to enhance quality levels on shipped parts and to improve long term reliability characteristics. Such product may be branded /BR or as required by purchase order.

Contact Product Marketing for availability and pricing on 883B, HR and BR products not listed here.

#### 100% DISCRETE DEVICE PROCESSING

Intersil also offers several QPL-approved discrete products carrying the JANTX designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

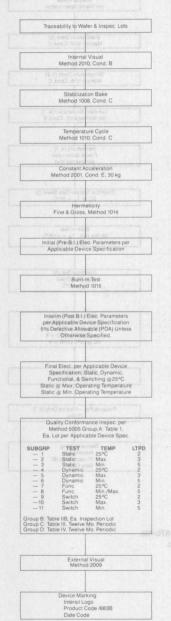
### 38510 Per MIL-M-38510 Slash Sheet Traceability to Water & Inspection Lots RECOMMENDED HANDLING Method 2010, Cond B Stabilization Bake Method 1008, Cond 24 hrs @ + 150°C Temperature Cycle Method 1010, Cond, C 10 Cycles, -65°C to + 150°C Constant Acceleration Method 2001, Cond E, 30 kg Fine & Gross, Method 1014 nitial (Pre-Burn-In) Electrical Parameters per silloon, in either case, it is rect Interium (Post Burn-In) Electrical Parameters per Applicable Device Specification 5% Defective Allowable (PDA) Unless Otherwise Specified Final Electrical per Applicable Device Static, Dynamic, Functional, & Switching Static @ Max. Operating Temperature Static @ Min. Operating Temperature Quality Conformance Inspection per Method 5005 Group A: Table I, Each Lot per Applicable Device Specification SUBGRP TEST TEMP LTPD 25°C Max Min up B: Table IIB, Eac External Visual Method 2009

Device Marking Intersil Logo JM 38510/XXX XX XXX Date Code

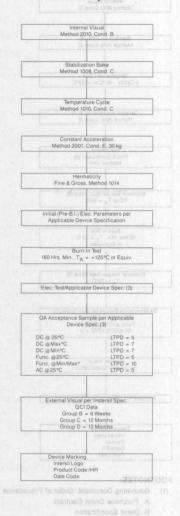




# /883B (1, 2, 4) Per MIL-STD-883 OF SELECTION Rev. C, Class B Screening per Method 5004

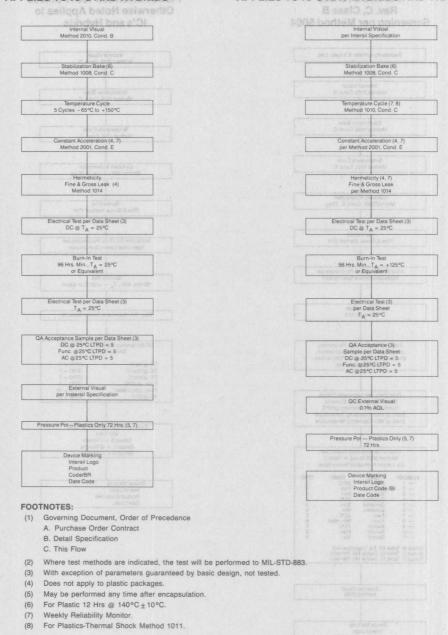


# HR (1, 2, 4) In-House Hi Rel Processing Flows Performed 100% Unless Otherwise Noted Applies to IC's and Hybrids



#### Performed 100% Unless Utnerwise Noted APPLIES TO IC'S AND HYBRIDS

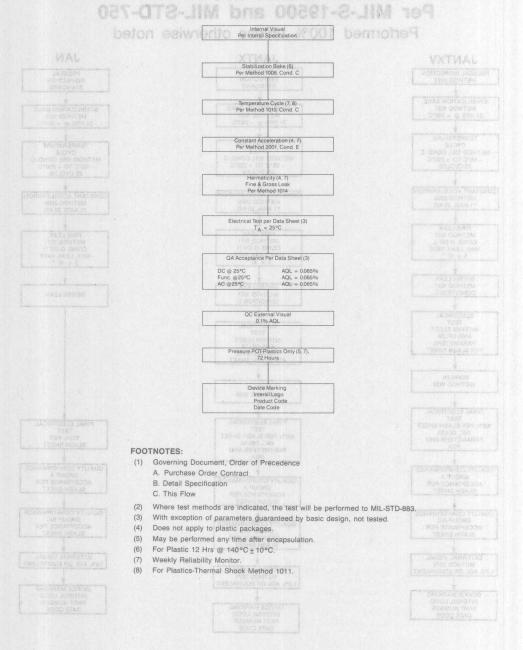
#### APPLIES TO IC'S ANY HYBRIDS AND TRANSISTORS







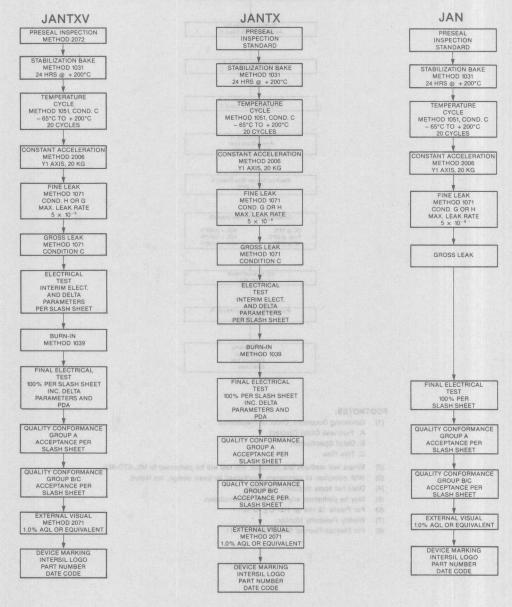
## Standard Product (1, 2) Performed 100% Unless Otherwise Noted APPLIES TO IC'S AND HYBRIDS AND TRANSISTORS





# High-Reliability/Military Products Discrete Products JANTXV, JANTX and JAN Per MIL-S-19500 and MIL-STD-750

Performed 100% unless otherwise noted





#### B 224 HIGH RELIABILITY PROCESSING PROCESS FLOW SELECTION GUIDE - STANDARD IC PROCESS FLOWS -

	38510 JAN	883B REV. C.	HR	BR	BI	COMMER	CIAL NOTES
ON-SHORE BUILD	Χ						
WAFER LOT TRACEABILITY	X	X					2
PRE-CAP VISUAL M2010B	X	X	X	X			
STABILIZATION BAKE	X	X	X	X	X	X	
TEMPERATURE CYCLE	X	X	X	X	S	S	3
CENTRIFUGE HERMETICITY ELECTRICAL TEST BURN-IN	X V Supple X X X X X X X X X X X X X X X X X X X	X X X	X DYNAMIC X TESTS IS	S X X	X	UOADBUB S	PROCESSES A SECONDER
ELECTRICAL TEST	X	X	X LTPD=E	X	X	X LIPPE	2 0 0 17
POST BURN-IN PDA	X	X		Decorate decouper-veneral		rational to	
D.C. ELECT. @ 3 TEMPS. A.C. ELECT. @ 25°C	ANICXOBUS	×	X			2 900000	
GROUP A SAMPLE INSPECTION	MARK X MINN	X	X	X X	X	X	
GROUP B EAC INSP. LOT	X	X	S		S	S	3
STRICT DOCUMENTATION	XHJ	X	G	enconst.		- Landing	
GROUP C & D INSPECTION	S	5	G	G			3

- NOTES:

  1. ONLY MAJOR IC PROCESSING DIFFERENCES ARE SHOWN HERE. SEE DETAIL FLOWS ON FOLLOWING PAGES FOR MORE SECIFIC DATA. CHART IS FOR HERMETIC PACKAGES. ONLY MINIMUM REQUIREMENTS ARE SHOWN. 38510 IS CLASS B.

  2. WAFER LOT TRACEABILITY MAINTAINED AND AVAILABLE AT EXTRA CHARGE FOR OTHER PRODUCTS.

  3. S = SAMPLE TEST ON REGULAR BASIS.

  X = PERFORMED 100%. G = GENERIC DATA.

  4. INTERSIL ALSO OFFERS "SPECIALS" TO SPECIFIC CUSTOMER SCD'S. SPECIALS ARE AVAILABLE WITH ANY OF THE ABOVE

- PROCESSING PLUS SEM, PIND, ETC.

#### HIGH RELIABILITY PROCESSING PROCESS FLOW SELECTION GUIDE - STANDARD TRANSISTOR PROCESS FLOWS -

ON-SHORE BUILD	JANTXV	JANTX	JAN	BI	COMMERCIAL	NOTES
INSPECTION LOT TRACEABILITY	x	×				2
PRE-CAP VISUAL	X	X	X			
STABILIZATION BAKE	X	X	X	X	X	
TEMPERATURE CYCLE	X	X	X	S	S	3
CENTRIFUGE	X	X		S	S	
HERMETICITY	X	X	X	S	S	
ELECTRICAL TEST	XX	X		X		
BURN-IN	X	X		X		
ELECTRICAL TEST	X	X				
POST BURN-IN PDA	X	X				
D.C. ELECT. @ 25°C	X	X	X	X	X	
A.C. ELECT. @ 25°C	Y Y Y Y Y	X	SUGGOODS 3	X	X	i Audikoeua I
GROUP A	тос оситаХ	X	SOX DONTEN	X	X	arek domina 1
GROUP B EACH INSP. LOT	X BOND	X	YT SAMEOUS	G	G	3 14
STRICT DOCUMENTATION	ar = QeT X	X	X = Gairi			
GROUP C INSPECTION	S	S	S			

- NOTES:

  1. ONLY MAJOR TRANSISTOR PROCESSING DIFFERENCES ARE SHOWN HERE. SEE DETAIL FLOWS ON FOLLOWING PAGES FOR MORE SPECIFIC DATA: CHART IS FOR HERMETIC PACKAGES. ONLY MINIMUM REQUIREMENTS ARE SHOWN.

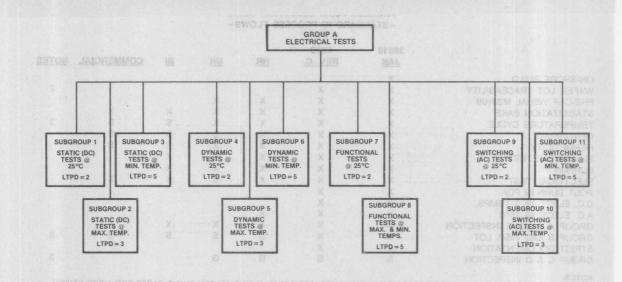
  2. WAFER LOT TRACEABILITY MAINTAINED AND AVAILABLE AT EXTRA CHARGE FOR OTHER PRODUCTS.

  3. S = SAMPLE TEST ON REGULAR BASIS.

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  4. INTERSIL ALSO OFFERS "SPECIALS" TO SPECIFIC CUSTOMER SCD'S. SPECIALS ARE AVAILABLE WITH ANY OF THE ABOVE

- PROCESSING PLUS SEM, PIND, ETC.

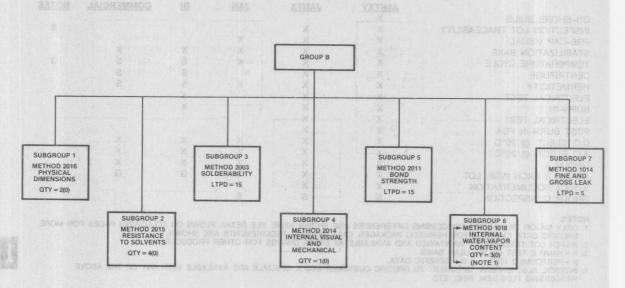


Notes:

1. The specific parameters to be included for tests in each subgroup shall be specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.

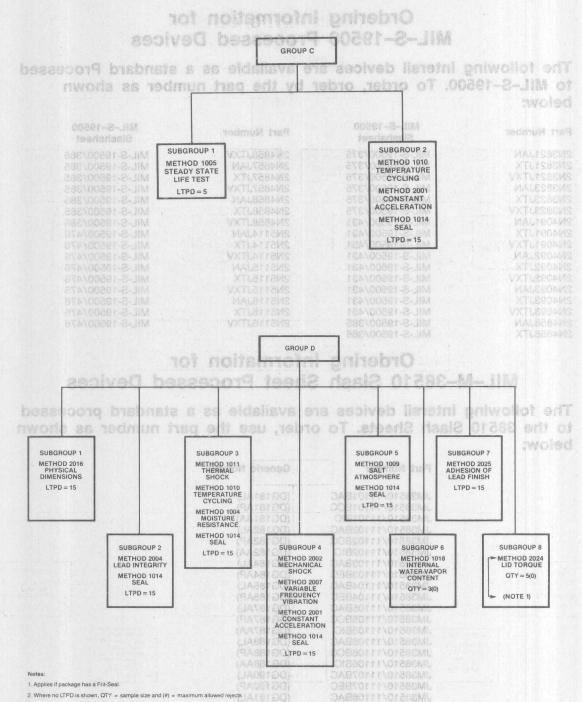
2. A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.

3. Maximum accept number is 2.



- Notes:

  1. Required only if package contains a desiccant.
- 2. Where no LTPD is shown, QTY = sample size and (#) = maximum allowed rejects.



## Ordering Information for MIL-S-19500 Processed Devices

The following Intersil devices are available as a standard Processed to MIL-S-19500. To order, order by the part number as shown below:

Part Number	MIL-S-19500 Slashsheet	Part Number	MIL-S-19500 Slashsheet
2N3821JAN	MIL-S-19500/375	2N4856JTXV	MIL-S-19500/385
2N3821JTX	MIL-S-19500/375	2N4857JAN	MIL-S-19500/385
2N3821JTXV	MIL-S-19500/375	2N4857JTX	MIL-S-19500/385
2N3823JAN	MIL-S-19500/375	2N4857JTXV	MIL-S-19500/385
2N3823JTX	MIL-S-19500/375	2N4858JAN	MIL-S-19500/385
2N3823JTXV	MIL-S-19500/375	2N4858JTX	MIL-S-19500/385
2N4091JAN	MIL-S-19500/431	2N4858JTXV	MIL-S-19500/385
2N4091JTX	MIL-S-19500/431	2N5114JAN	MIL-S-19500/476
2N4091JTXV	MIL-S-19500/431	2N5114JTX	MIL-S-19500/476
2N4092JAN	MIL-S-19500/431	2N5114JTXV	MIL-S-19500/476
2N4092JTX	MIL-S-19500/431	2N5115JAN	MIL-S-19500/476
2N4092JTXV	MIL-S-19500/431	2N5115JTX	MIL-S-19500/476
2N4093JAN	MIL-S-19500/431	2N5115JTXV	MIL-S-19500/476
2N4093JTX	MIL-S-19500/431	2N5116JAN	MIL-S-19500/476
2N4093JTXV	MIL-S-19500/431	2N5116JTX	MIL-S-19500/476
2N4856JAN	MIL-S-19500/385	2N5116JTXV	MIL-S-19500/476
2N4856JTX	MIL-S-19500/385		

## Ordering Information for MIL-M-38510 Slash Sheet Processed Devices

The following Intersil devices are available as a standard processed to the 38510 Slash Sheets. To order, use the part number as shown below:

Part Number	Generic Number
JM38510/11101BAC	(DG181AL)
JM38510/11101BCC JM38510/11101BIC	(DG181AP) (DG181AA)
JM38510/11102BAC	(DG182AL)
JM38510/11102BCC	(DG182AP)
JM38510/11102BIC	(DG182AA)
JM38510/11103BAC	(DG184AL)
JM38510/11103BEC	(DG184AP)
JM38510/11104BAC JM38510/11104BEC	(DG185AL) (DG185AP)
JM38510/11105BAC	(DG187AL)
JM38510/11105BCC	(DG187AP)
JM38510/11105BIC	(DG187AA)
JM38510/11106BAC	(DG188AL)
JM38510/11106BCC	(DG188AP)
JM38510/11106BIC	(DG188AA)
JM38510/11107BAC JM38510/11107BEC	(DG190AL) (DG190AP)
JM38510/11107BEC	(DG190AF)
JM38510/11108BEC	(DG191AP)
JM38510/12704BVC	(AD7541TD)

# Ordering Information for DESC Drawing Processed Devices

The following Intersil devices are available as a standard processed to the DESC Drawings. To order, use the part number as shown below:

tensing and istantancing				
Part Number	Generic Number	Part Number	Generic Number	
DESC77052-01EB DESC77052-01EX DESC77053-01EX DESC77053-01EX DESC81006-01AC DESC81006-01AX DESC81006-01EB DESC81006-01EX DESC81006-02AX DESC81006-02AX DESC81006-02EB DESC81006-02EB DESC81006-02EX DESC81006-02IC DESC81006-03AC DESC81006-03AC DESC81006-03AC DESC81006-03AX DESC81006-03AX DESC81006-03AX DESC81006-03AX DESC81006-03AX DESC81006-04AC DESC81006-04AC DESC81006-04AC DESC81006-04EB DESC81006-04EB DESC81006-04EB	(IH6108MJE) (IH6108MJE) (IH6108MJE) (DG201AK) (DG201AK) (IH5040MFD) (IH5040MFD) (IH5040MJE) (IH5041MFD) (IH5041MFD) (IH5041MJE) (IH5041MJE) (IH5041MTW) (IH5041MTW) (IH5042MFD) (IH5042MFD) (IH5042MFD) (IH5043MFD) (IH5043MFD) (IH5043MFD) (IH5043MFD) (IH5043MFD) (IH5043MFD) (IH5043MFD) (IH5043MJE)	DESC81006-07EX DESC81006-08AC DESC81006-08AX DESC81006-08EB DESC81006-08EX	(IH5044MFD) (IH5044MFD) (IH5044MJE) (IH5044MJE) (IH5045MFD) (IH5045MFD) (IH5045MJE) (IH5046MFD) (IH5046MFD) (IH5046MFD) (IH5046MJE) (IH5046MJE) (IH5047MFD) (IH5047MFD) (IH5047MFD) (IH5047MJE)	
DESC81006-04EX	(IHOU43IVIJE)		the manufacture of the 1921 civilia	

ACCELERATED BURN-IN — Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150°C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA — Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE — Technique used to define manufacturing and test processes at time of order placement. Baselining usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs.

**BURN-IN** — A screening operation. Devices are subjected to high temperature (typically 125°C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

class s and b integrated circuits — These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-STD-883. Classes, S and B are sometimes referred to as "Levels S and B." The Classes cover:

**CLASS S**—For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.

**CLASS B** — For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap visual, etc.

**CORRECTIVE ACTION** — Those actions which a given supplier (or user) agrees to perform so that a detected problem does not reoccur.

**DESC** — Defense Electronic Supply Center, located in Dayton, Ohio.

**DESC LINE CERTIFICATION** — The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

**DPA** — Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

**GENERIC DATA** — Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order.

**GROUP A** — Sample electrical test which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

**GROUP B** — For Integrated Circuits, Package-Related Environmental Tests are performed for Class B Products per MIL-STD-883, Method 5005 (For Revision Products) or per the "HR" program. For Class S, Group B includes Additional Processing, including steady state life test.

For Diodes and Transistors, both environmental and life test are performed per MIL-S-19500.

**GROUP C** — For Class B or "HR" program I.C.'s, Die-Related Tests are performed. Not required for Class S I.C.'s. Group G includes life testing temperature cycling and constant acceleration per MIL-M-38510. For diodes transistors, Group C includes both environmental and life tests per MIL-S-19500

**GROUP D** — Additional Package-Related Environmental Test for I.C.'s for Class B or Class S products or per the "HR" program.

JAN — "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX — A JAN-qualified diode or transistor which has been subjected to additional screening and burn-in tests. MIL-S-19500 only.

JAN TXV — A JAN-qualified diode or transistor which, in additional to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits. MIL-S-19500 only.

LTPD-Lot Tolerance Percent Defective is a sampling plan measurement criteria.

MIL-M-38510 — The general military specification for integrated circuits.

M38510/XXX — Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-S-19500 — The general military specifications for diodes and transistors.

MIL-S-19500/XXX — Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 — Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

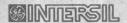
MIL-STD-883 — Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, hermeticity, storage life, etc.

**NPFC** — Naval Publications and Forms Center, Philadelphia Printing and distribution source for military specifications.

NON-STANDARD PARTS — In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL — Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

#### HIGH RELIABILITY PROCESSING



**OPERATING LIFE TEST**—Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA — Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA — Percent Defective Allowable. Criteria sometimes applied to burn-in screening. MIL-STD-883 and MIL-M-38510 typically require either a 5% or 10% PDA. A 10% PDA means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

**PDS** — Parameter Drift Screening. Measures the changes (Δs) in electrical parameters through burn-in. Common for Class S devices.

PIND — Particle Impact Noise Detection. This is an audio screening test to locate and eliminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY — The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL — A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY — Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABILITY — Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours) or MTBF (mean time between failure in hours). MTBF is the reciprocal of Failure Rate.

QPL — Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist for MIL-M-38510:

PART II QPL — This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided after 90 days whenever any one supplier is granted a PART I QPL.

PART I QPL — A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QUALIFYING ACTIVITY — Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING — Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D per MIL-STD-883. For diodes and transistors, this usually means testing to Groups A, B and C per MIL-STD-750.

QUALITY CONFORMANCE TESTING — These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

RADC — Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA - Same as variable data.

**REWORK PROVISION** — For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), re-marking, and cleaning.

**SCREENING** — Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc.

**SEM INSPECTION** — Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects.

**SERIALIZATION** — The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs — Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

**SOURCE INSPECTION** — Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can typically occur at one or more points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection.

**TRACEABILITY** — A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA — Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.

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#### PART NUMBERING SYSTEM



#### **Examples of Intersil Part Numbers**

BASIC	ELECTRICAL OPTION	TEMP	PKG	PIN	ORDER #
ICH8500	HS UAING TH	C	MGO.	V	ICH8500ACTV
ICL8038	Debuic 1.01c	C	P	D	ICL8038CCPD
IH5040	TIS SONAD GILL	M	D	E	IH5040MDE

## ON ALL INTERSIL IC PART NUMBERS. THE LAST THREE LETTERS ARE TEMPERATURE, PACKAGE, AND NUMBER OF PINS, RESPECTIVELY.

DACKAGE.	η Αο''	TO	7 0	TIOZ 3 Vo clinit man			
		TO-237 Plastic flat-pack					
IS USING THE							
	D			om OVRER OU BOOM ual-in-line Fashor			
	10-75	Small	TO-	8			
ibraep eut sum	dxF L	Ceran	nic fl	8 at-pack			
H8510 family b	Ol jen	TO-66	110	at-pack soupinnost			
		16 ni	16	x.7 pin spacing)			
	DISHNO	he	rmet	ic hybrid din			
	J	Cerdi	) diis	al-in-line			
	K	TO-3	Dissi	Explains the ope			
	ylagu	Lead	ess.	ceramic and to to to			
	Pb	Plasti	dua	al-in-line babulant			
	S	TO-52	o in				
anmedworp epa	dioy a	TO-5	type				
	des rev	(also	TO-7	'8, TO-99, TO-100)			
	100	TO-72	type	e 8, TO-71)			
		(also	TO-1	8, TO-71)			
	V	TO-39					
	Z	TO-92					
	/W	Wafer	u me				
NUMBER OF PINS:	A	8	P	Acres Power Cook			
NUMBER OF PINS:	A B C	8 10 12	P Q R	Age and ranging to the control of th			
NUMBER OF PINS:	A B C	8 10 12	P Q R	20			
NUMBER OF PINS:	A B C D	8 10 12 14	P Q R S	Age and ranging to the control of th			
NUMBER OF PINS:	A B C D E	8 10 12 14 16	P Q R S T	20 Haddadada 33 KUO 3HT 000A			
NUMBER OF PINS:	A B C D E F	8 10 12 14 16 22	PQRSTU	20 2 18 1 2 2 18 1 3 2 1 3 1 4 3 1 4 3 1 4 3 1 4 3 1 4 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 8 2 3 1 6 5 3 1 6 6 1 6 1 6			
NUMBER OF PINS:	A B C D E F G	8 10 12 14 16 22 24	PQRSTUV	20 2 3 4 6 7 8 (0.200" pin circle, isolated case)			
NUMBER OF PINS:	A B C D E F G	8 10 12 14 16 22 24	PQRSTUV	20 2 3 4 6 7 8 (0.200" pin circle, isolated case)			
NUMBER OF PINS: CITY OF PINS:	A B C D E F G H L	8 10 12 14 16 22 24 42 28	P QRSTUV W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle.			
NUMBER OF PINS: OF PI	A BCDEFG H.	8 10 12 14 16 22 24 42 28	P QRSTUV W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle, isolated case)			
NUMBER OF PINS: OF PI	A BCDEFG H J	8 10 12 14 16 22 24 42 28	P QRSTUV W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle, isolated case)			
NUMBER OF PINS: OF PI	A BCDEFG H J	8 10 12 14 16 22 24 42 28	P QRSTUV W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle, isolated case)			
ATRUM AND AND AND AND AND AND AND AND AND AND	A BCDEFG HI JK	8 10 12 14 16 22 24 42 28 32 35	P QRSTUV W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle, isolated case) 8 (0.200" pin circle, case to pin 4)			
NUMBER OF PINS:  GLA TUSTIC  GLASSION  GLASSIO	A BCDEFG HI JK L	8 10 12 14 16 22 24 42 28 32 35	P Q R S T U V W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle, isolated case) 8 (0.200" pin circle, case to pin 4)			
TRUT A/D STRING TO STRING	A BCDEFG HI JK LM	8 10 12 14 16 22 24 42 28 32 35 40 48	P Q R S T U V W	20 2 3 4 6 7 8 (0.200" pin circle, isolated case) 10 (0.230" pin circle, isolated case) 8 (0.200" pin circle, case to pin 4)			

#### APPLICATION NOTE SUMMARY

releys: Describes CMOS, hybrid (FET + driver), U-	
types. Application information included.	
ground" analog switches and provides suggested applications.	
logentilog amplifier, sample and hold discuit,	
	KODY
EVERYTHING YOU ALWAYS WANTED TO KNOW	
regarding the use of the 8038.	
DESIGN FOR A BATTERY OPERATED	
Describes the differences between integrating	
and a note on multiplexed data systems.	
	AG17
CONVENTERS	
An analysis of proper design techniques using D/A	
A 12 DIGIT PANEL METER DEMONSTRATION	AG19

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#### APPLICATION NOTE SUMMARY

The following are brief descriptions of current Intersil Application notes.

A003 UNDERSTANDING AND APPLYING THE ANALOG SWITCH Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET + driver), J-FET "virtual ground" and J-FET "positive signal" types. Application information included.

A004 IH5009 LOW COST ANALOG SWITCH SERIES Compares the members of the IH5009 "virtual ground" analog switches and provides suggested

applications.

A005 THE 8007 — A HIGH PERFORMANCE FET INPUT OP AMP Compares the 8007 with the 741, which is pin compatible and suggests applications such as logantilog amplifier, sample and hold circuit. photometer, peak detector, etc.

A007 USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER Describes in detail the operation of the 8048 logarithmetic amplifier, and its counterpart, the 8049 antilog amp.

A011 A PRECISION FOUR QUADRANT MULTIPLIER -THE 8013 Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication. division, and square root applications.

A013 EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038 This note includes 17 of the most asked questions regarding the use of the 8038.

A015 DESIGN FOR A BATTERY OPERATED FREQUENCY COUNTER Describes a low cost battery operated frequency/ period counter using the 7207A and 7208. Includes specifications, schematics, PC layout, etc.

A016 SELECTING A/D CONVERTERS Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.

A017 THE INTEGRATING A/D CONVERTER Provides an explanation of integrating A/D converters, together with a detailed error analysis.

A018 DO'S AND DONT'S OF APPLYING A/D CONVERTERS An analysis of proper design techniques using D/A converters.

A019 41/2 DIGIT PANEL METER DEMONSTRATION/ INSTRUMENTATION BOARDS Describes two typical PC board layouts using the 8052A/7103A 41/2 digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.

A020 A COOKBOOK APPROACH TO HIGH SPEED DATA ACQUISITION AND MICROPROCESSOR INTERFACING

Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.

A021 POWER D/A CONVERTERS USING THE ICH 8510 Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc. Also see A026.

A022 A NEW J-FET STRUCTURE - THE VARAFET Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built-in.

A023 LOW COST DIGITAL PANEL METER DESIGNS Provides a detailed explanation of the 7106 and 7107 31/2 digit panel meter IC's, and describes two of the evaluation kits available from Intersil.

A026 DC SERVO MOTOR SYSTEMS USING THE ICH8510 This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.

A027 POWER SUPPLY DESIGN USING THE ICL8211

AND ICL8212

Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.

A028 BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a ±41/2 digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.

A029 POWER OF AMP HEAT SINK KIT Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.

A030 THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS Describes in detail the operation of the 7104. Includes in digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.

A031 COIL DRIVE ALARM DESIGN CONSIDERATIONS Explains the procedure used when using watch circuits to drive piezoelectric transducers.

A032 UNDERSTANDING THE AUTO-ZERO AND COMMON MODE PERFORMANCE OF THE ICL7106/7107/7109 FAMILY Explains in detail the operation of the ICL7106/7/9 family of A/D Converters.

A046 BUILDING A BATTERY OPERATED AUTO RANGING DVM WITH THE ICL7106 Explains principles of auto ranging, problems and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.

A047 GAMES PEOPLE PLAY WITH A/D CONVERTERS Describes 25 different integrating A/D converter applications. Input circuits, conversion modifications,



- display and microprocessor interfaces are shown in detail.
- A050 USING THE IT500 FAMILY TO IMPROVE THE INPUT BIAS CURRENT OF BIFET OP AMPS A brief description of a preamplifier for BIFET OP
- A051 PRINCIPLES AND APPLICATIONS OF THE ICL7660 CMOS VOLTAGE CONVERTER Describes internal operation of the ICL7660. Includes a wide range of possible applications.
- A052 TIPS FOR USING SINGLE CHIP 31/2 DIGIT A/D CONVERTERS Answers frequently asked questions regarding the operation of 31/2 digit single chip A/D converters. Included are sections on power supplies, displays,
- A053 THE ICL7650 A NEW ERA IN GLITCH-FREE CHOPPER STABILIZER AMPLIFIERS A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.
- A054 DISPLAY DRIVER FAMILY COMBINES CONVENIENCE OF USE WITH MICROPROCESSOR INTERFACABILITY Compares and describes the various display drivers. Includes design examples for 7 segment, Alphanumeric, and bargraph systems.
  - AVOIDING PROBLEMS IN CMOS MEMORY **OPERATION** Discusses input overvoltage and SCR latchup and the multiple address access problem in CMOS timing and component selection.

#### ORDERING INFORMATION



#### and to notistago lametre and to not Device Family Prefixes

Device Family Prefixes

AD — Analog Devices Alternate Source
D — Driver/Level Translator IC
Sense polyacidade de de la company d

#### Electrical Option/Variation of Basic Device Type Designators

These designators are datasheet dependent, and are not always used. [30,43] hereas things and greened a second sec

#### one quito and single chip A/D converters. Stephenous CNA girls single si

SOMO ni meldoto associa seeroba el chi Commercial: 0°C to +70°C avalgaio selloquis ravion no anotoes era babuloni

—Industrial: Either – 25°C to +85°C or – 40°C to +85°C 10d 39 kg 11191 00 1100 1101 1119 (Specified on Datasheet)

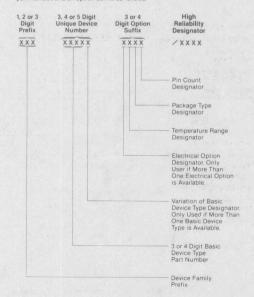
- Military: - 55°C to + 125°C

#### **Package Type Designators**

\_TO-237 -TO-237
-Small Outline IC (SOIC)
-TO-220
-Ceramic Dual-In-Line
-Small TO-8
-Ceramic Flat Pack
-TO-66 - Ceramic Flat Pack
- To-66
- 16 Pin (.6 x. 7 Pin Spacing)
Hermetic Hybrid Dip
- CERDIP Dual-In Line
- To-30
- Pestic Dual-In-Line
- To-57
- To-5 Type
- (Also TO-78, TO-99, TO-100)
- TO-72 Type
- (Also TO-78, TO-71)
- TO-39
- TO-39
- TO-39
- TO-92
- Wafer
- Dice /W /D

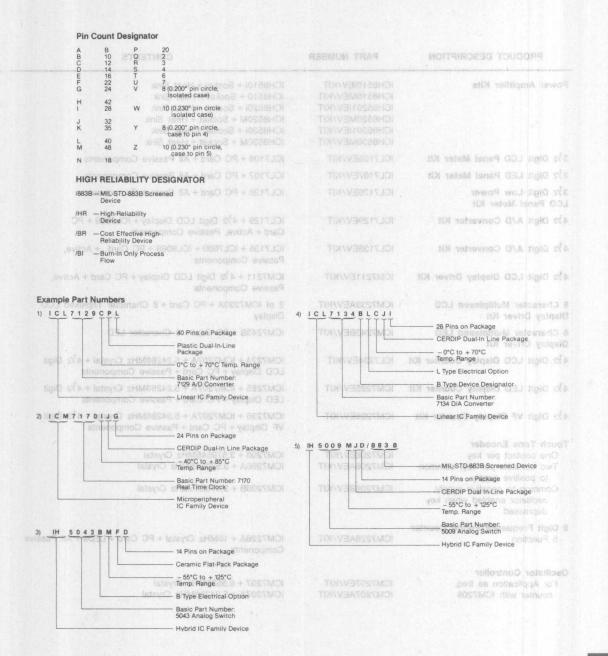
#### -Dice Part Numbering System

All Intersil IC part numbers consist of a device family prefix, a basic numeric part number, and an option suffix, as follows:



#### ORDERING INFORMATION



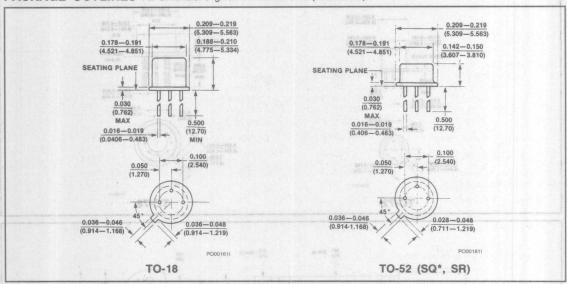


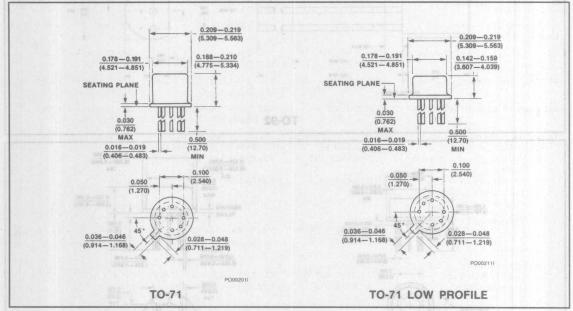
### **EVALUATION KITS**

### MOTTAMPOTM SINTERSIL

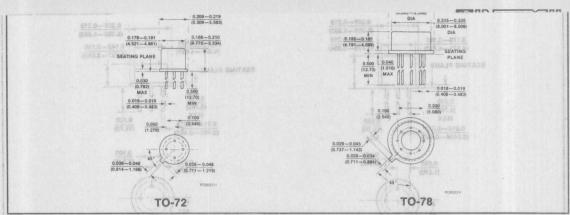
		Pin Count Designator		
PRODUCT DESCRIPTION	PART NUMBER	CONTENTS		
Power Amplifier Kits	ICH8510IEV/KIT ICH8510MEV/KIT ICH85201IEV/KIT ICH8520MEV/KIT ICH85301IEV/KIT ICH8530MEV/KIT	ICH8510i + Socket + Heat Sink ICH8510 + Socket + Heat Sink ICH8520i + Socket + Heat Sink ICH8520M + Socket + Heat Sink ICH8530i + Socket + Heat Sink ICH8530M + Socket + Heat Sink		
3½ Digit LCD Panel Meter Kit	ICL7106EV/KIT	ICL7106 + PC Card + All Passive Components		
31/2 Digit LED Panel Meter Kit	ICL7107EV/KIT	ICL7107 + PC Card + All Passive Components		
3½ Digit Low Power LCD Panel Meter Kit	ICL7126EV/KIT	ICL7126 + PC Card + All Passive Components		
4½ Digit A/D Converter Kit	ICL7129EV/KIT	ICL7129 + 4½ Digit LCD Display + ICL8069 + PC Card + Active, Passive Components		
4½ Digit A/D Converter Kit	ICL7135EV/KIT	ICL7135 + ICL7660 + ICL8069 + PC Card + Active, Passive Components		
4½ Digit LCD Display Driver Kit	ICM7211EV/KIT	ICM7211 + 4½ Digit LCD Display + PC Card + Active, Passive Components		
8 Character Multiplexed LCD Display Driver Kit	ICM7233AEV/KIT	2 of ICM7233A + PC Card + 8 Character Triplexed LCD Display		
8 Character Multiplexed LED Display Driver Kit	ICM7243BEV/KIT	ICM7243B + PC Card + 8 Character LED		
4½ Digit LCD Display Counter Kit	ICL7224EV/KIT	ICM7224 + ICM7207A + 5.24288MHz Crystal + 4 <sup>1</sup> / <sub>2</sub> Digit LCD Display + PC Card + Passive Components		
4½ Digit LED Display Counter Kit	ICM7225EV/KIT	ICM7225 + ICM7207A + 5.24288MHz Crystal + 4½ Digit LED Display + PC Card + Passive Components		
4½ Digit VF Display Counter Kit	ICM7236EV/KIT	ICM7236 + ICM7207A + 5.24288MHz Crystal + 4½ Digit VF Display + PC Card + Passive Components		
Touch Tone Encoder  One contact per key, Two contacts per key, common to positive supply	ICM7206EV/KIT ICM7206AEV/KIT	ICM7206 + 3.579545MHz Crystal ICM7206A + 3.579545MHz Crystal		
Common to negative supply, oscillator enabled when key depressed	ICM7206BEV/KIT	ICM7206B + 3:579545MHz Crystal		
8 Digit Frequency/Period Counter		GRADENES HER		
5 Function Several Visual Control of Several Contro	ICM7226AEV/KIT	ICM7226A + 10MHz Crystal + PC Card + LEDs + All Passiv Components		
Oscillator Controller		Ceramic Flat-Pack Pockage		
For Application as freq. counter with ICM7208	ICM7207EV/KIT ICM7207AEV/KIT	ICM7207 + 6.5536MHz Crystal ICM7207A + 5.24288MHz Crystal		

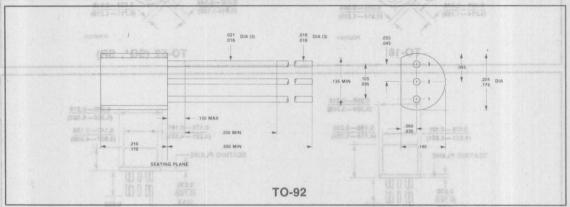


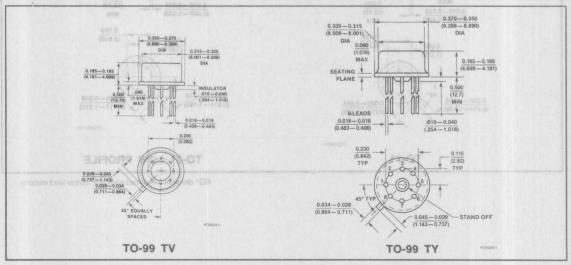




SQ\* denotes a two lead package; center lead missing.



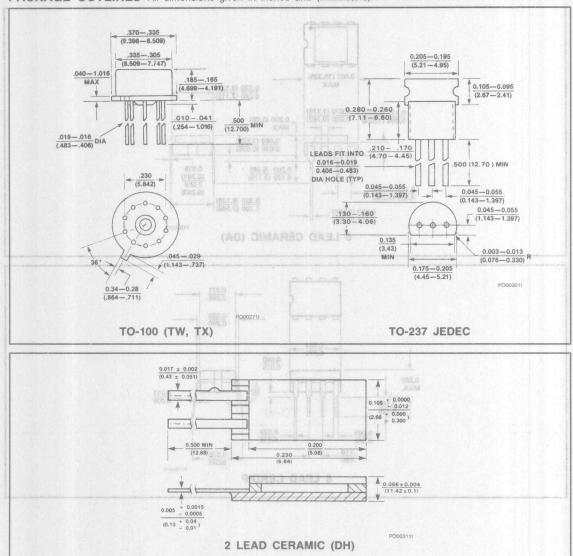




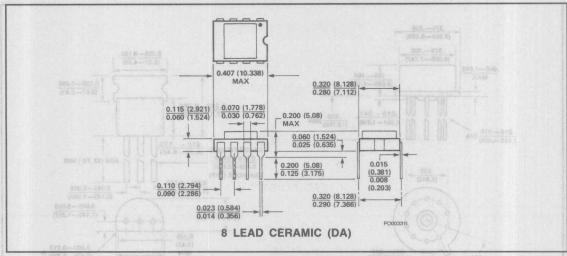


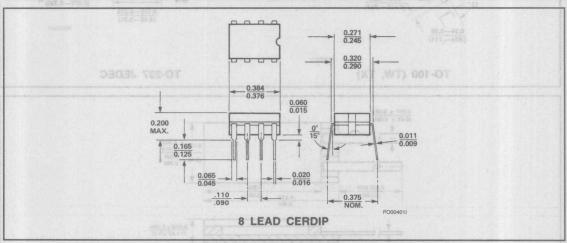


#### PACKAGE OUTLINES All dimensions given in inches and (millimeters). Particular and (millimeters).

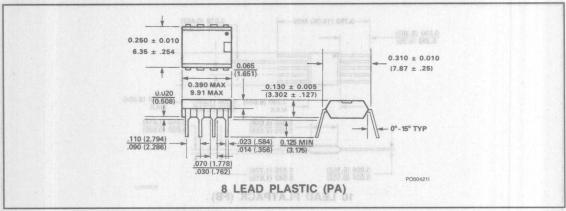


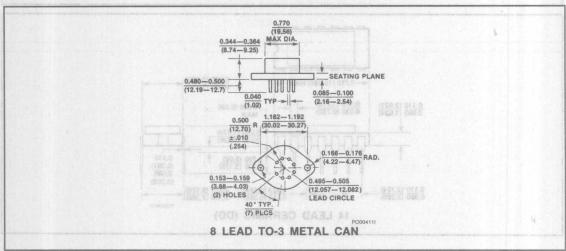


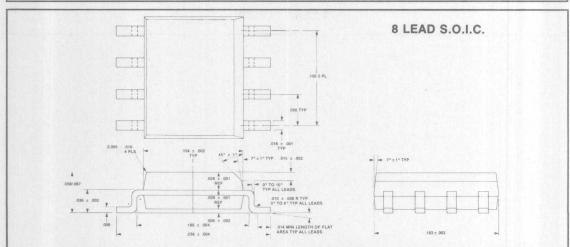








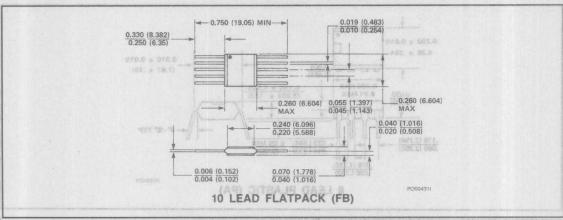


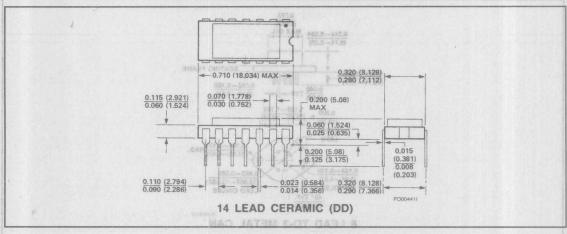


**WINTERSIL** 

#### PACKAGE OUTLINES All dimensions given in inches and (millimeters). Claramin NA 83ML/TUO 30ANOA9

8 LEAD S.O.I.C.

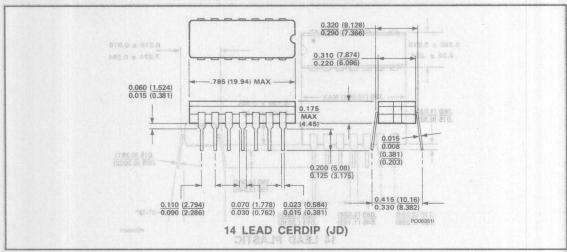


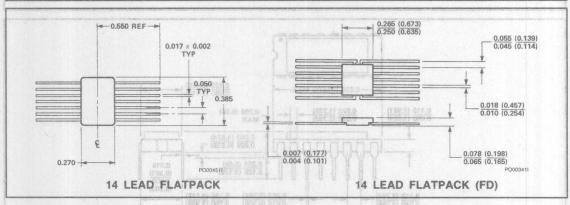




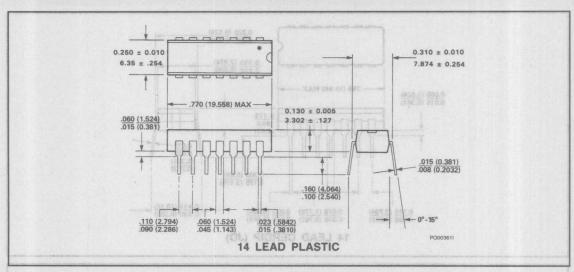


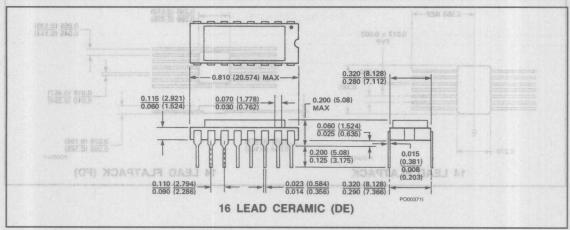
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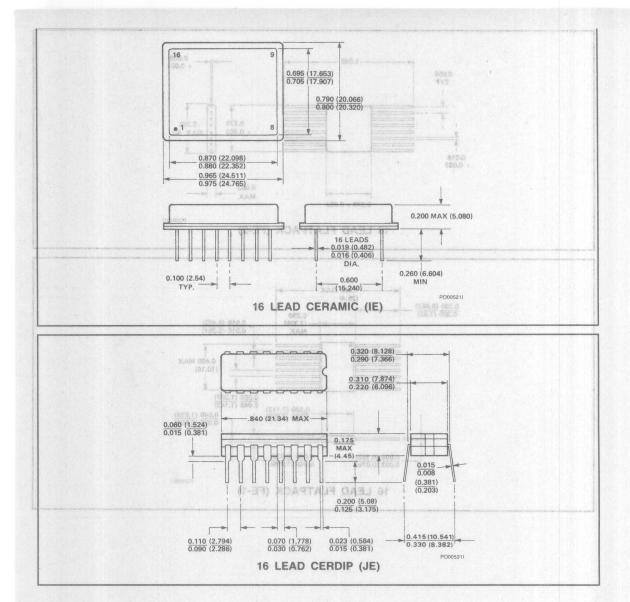




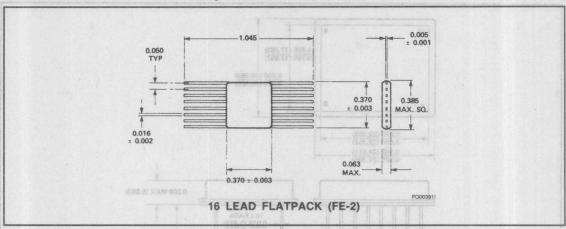
16 LEAD CERAMIC (DE)

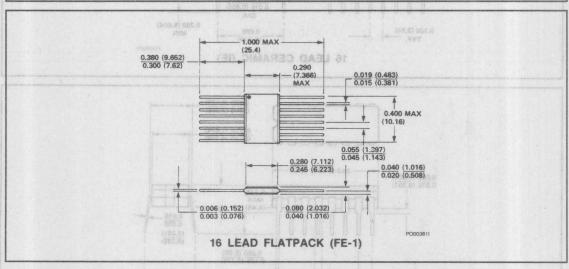


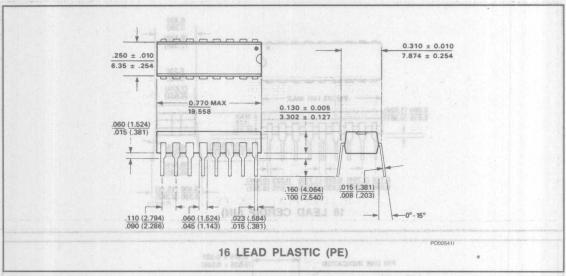


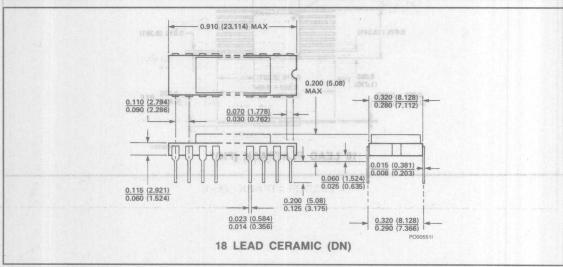






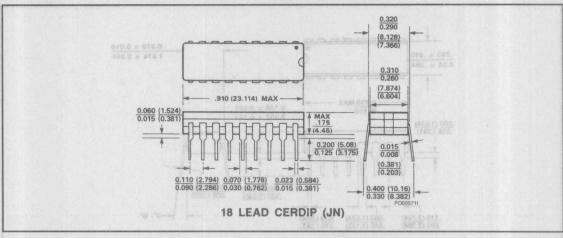


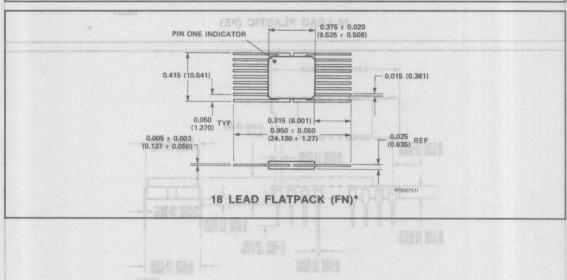


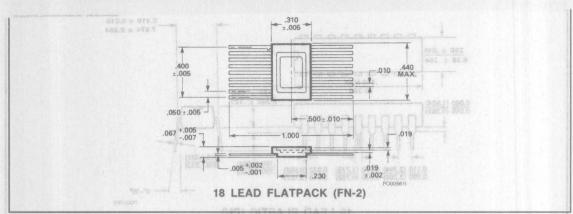


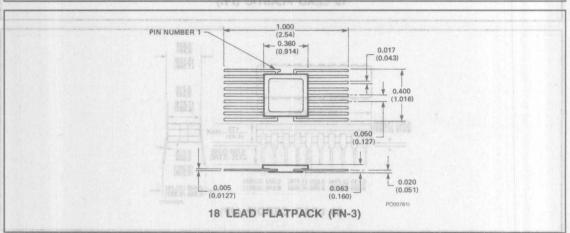


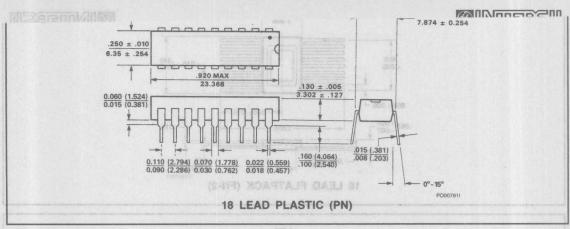


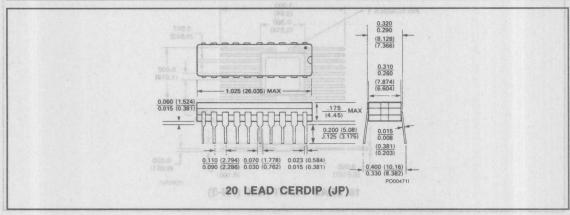




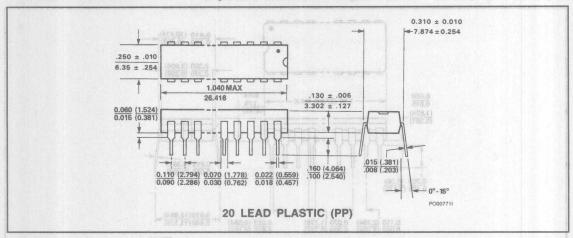


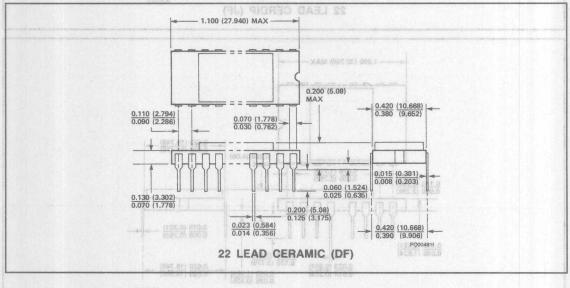








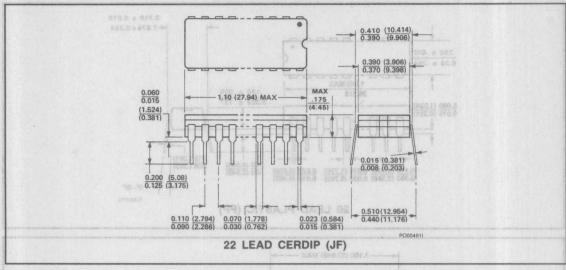


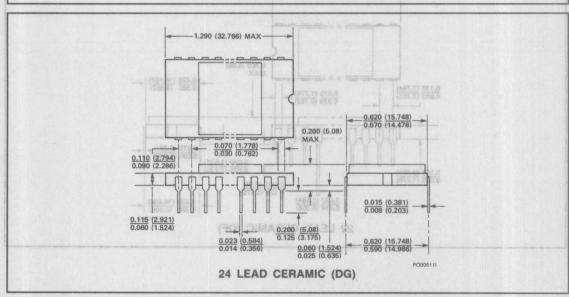


24 LEAD CERAMIC (DG)

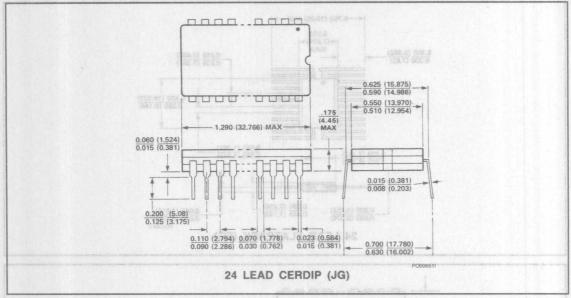


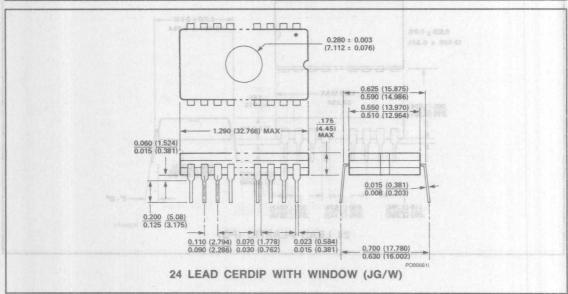


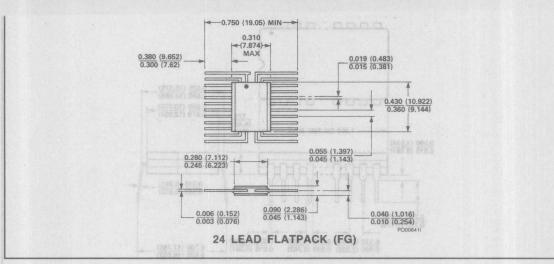


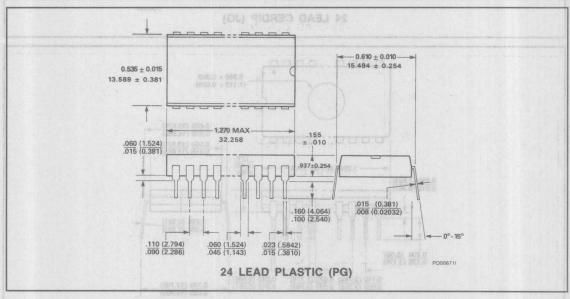














#### PACKAGE OUTLINES All dimensions given in inches and (millimeters). Managed IIA 83/MUTUO 38/AMOAS

